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74LVC2G3157

Dual 10 Ω single-pole double-throw analog switch

Rev. 2 — 15 December 2016

Product data sheet

1. General description

The 74LVC2G3157 is a dual low-ohmic single-pole double-throw analog switch suitable for use as an analog or digital 2:1 multiplexer/demultiplexer. Each switch has a digital select input (nS), two independent inputs/outputs (nY0 and nY1) and a common input/output (nZ).

Schmitt trigger action at the select inputs makes the circuit tolerant of slower input rise and fall times across the entire V_{CC} range from 1.65 V to 5.5 V.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- Very low ON resistance:
 - ◆ 10.4 Ω (typical) at $V_{CC} = 2.7$ V
 - ◆ 7.8 Ω (typical) at $V_{CC} = 3.3$ V
 - ◆ 6.2 Ω (typical) at $V_{CC} = 5$ V
- Switch current capability of 32 mA
- Break-before-make switching
- High noise immunity
- CMOS low power consumption
- TTL interface compatibility at 3.3 V
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- ESD protection:
 - ◆ HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2 kV
 - ◆ MM JESD22-A115-C exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Select input accepts voltages up to 5.5 V
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC2G3157DP	-40 °C to +125 °C	TSSOP10	plastic thin shrink small outline package; 10 leads; body width 3 mm	SOT552-1
74LVC2G3157GM	-40 °C to +125 °C	XQFN10	plastic extremely thin quad flat package; no leads; 10 terminals; body 2 × 1.55 × 0.5 mm	SOT1049-3

4. Marking

Table 2. Marking codes

Type number	Marking code ^[1]
74LVC2G3157DP	YJ
74LVC2G3157GM	YJ

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

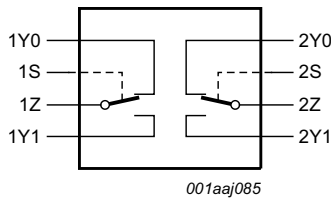


Fig 1. Logic symbol

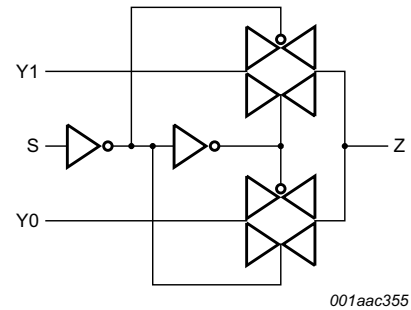


Fig 2. Logic diagram (one switch)

6. Pinning information

6.1 Pinning

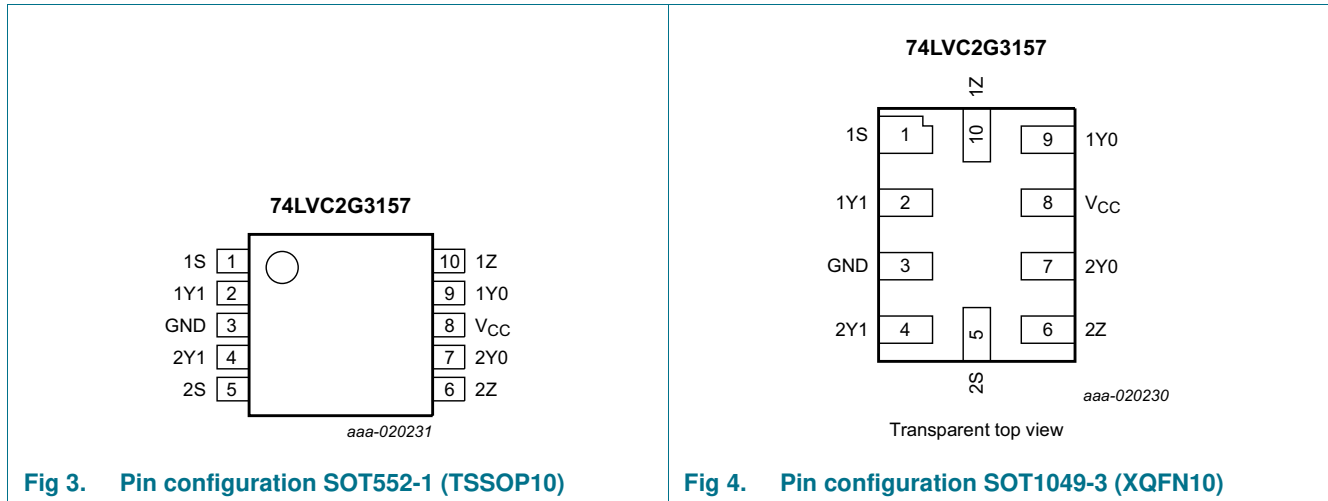


Fig 3. Pin configuration SOT552-1 (TSSOP10)

Fig 4. Pin configuration SOT1049-3 (XQFN10)

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
1S	1	select input
1Y1	2	independent input or output
GND	3	ground (0 V)
2Y1	4	independent input or output
2S	5	select input
2Z	6	common output or input
2Y0	7	independent input or output
V _{CC}	8	supply voltage
1Y0	9	independent input or output
1Z	10	common output or input

7. Functional description

Table 4. Function table^[1]

Input nS	Channel on
L	nY0
H	nY1

[1] H = HIGH voltage level; L = LOW voltage level.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
V_I	input voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < -0.5$ V	-50	-	mA
I_{SK}	switch clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	± 50	mA
V_{SW}	switch voltage	enable and disable mode	-0.5	$V_{CC} + 0.5$	V
I_{SW}	switch current	$V_{SW} > -0.5$ V or $V_{SW} < V_{CC} + 0.5$ V	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	$^{\circ}$ C
P_{tot}	total power dissipation	$T_{amb} = -40$ $^{\circ}$ C to +125 $^{\circ}$ C	-	250	mW

- [1] The minimum input voltage rating may be exceeded if the input current rating is observed.
 [2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.
 [3] For TSSOP10 package: above 55 $^{\circ}$ C the value of P_{tot} derates linearly with 2.5 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_{SW}	switch voltage	enable and disable mode	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+125	$^{\circ}$ C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	-	-	20	ns/V
		$V_{CC} = 2.7$ V to 5.5 V	-	-	10	ns/V

- [1] To avoid sinking GND current from terminal Z when switch current flows in terminal Yn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no GND current will flow from terminal Yn. In this case, there is no limit for the voltage drop across the switch.
 [2] Applies to control signal levels.

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65V _{CC}	-	-	0.65V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 3 V to 3.6 V	2.0	-	-	2.0	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7V _{CC}	-	-	0.7V _{CC}	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35V _{CC}	-	0.35V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 3 V to 3.6 V	-	-	0.8	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3V _{CC}	-	0.3V _{CC}	V
I _I	input leakage current	pin nS; V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V ^[2]	-	±0.1	±1	-	±1	μA
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 5.5 V; see Figure 5 ^[2]	-	±0.1	±0.2	-	±0.5	μA
I _{S(ON)}	ON-state leakage current	V _{CC} = 5.5 V; see Figure 6 ^[2]	-	±0.1	±1	-	±2	μA
I _{CC}	supply current	V _I = 5.5 V or GND; V _{SW} = GND or V _{CC} ; V _{CC} = 1.65 V to 5.5 V ^[2]	-	0.1	4	-	4	μA
ΔI _{CC}	additional supply current	pin nS; V _I = V _{CC} - 0.6 V; V _{CC} = 5.5 V; V _{SW} = GND or V _{CC} ^[2]	-	5	500	-	500	μA
C _I	input capacitance		-	2.5	-	-	-	pF
C _{S(OFF)}	OFF-state capacitance		-	6.0	-	-	-	pF
C _{S(ON)}	ON-state capacitance		-	18	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

[2] These typical values are measured at V_{CC} = 3.3 V

10.1 Test circuits

$V_I = V_{CC}$ or GND and $V_O =$ GND or V_{CC} .

Fig 5. Test circuit for measuring OFF-state leakage current

$V_I = V_{CC}$ or GND and $V_O =$ open circuit.

Fig 6. Test circuit for measuring ON-state leakage current

10.2 ON resistance

Table 8. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground 0 V); for graphs see [Figure 8](#) to [Figure 13](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
R _{ON(peak)}	ON resistance (peak)	$V_I =$ GND to V_{CC} ; see Figure 7						
		$I_{SW} = 4$ mA; $V_{CC} = 1.65$ V to 1.95 V	-	34.0	130	-	195	Ω
		$I_{SW} = 8$ mA; $V_{CC} = 2.3$ V to 2.7 V	-	12.0	30	-	45	Ω
		$I_{SW} = 12$ mA; $V_{CC} = 2.7$ V	-	10.4	25	-	38	Ω
		$I_{SW} = 24$ mA; $V_{CC} = 3.0$ V to 3.6 V	-	7.8	20	-	30	Ω
		$I_{SW} = 32$ mA; $V_{CC} = 4.5$ V to 5.5 V	-	6.2	15	-	23	Ω
R _{ON(rail)}	ON resistance (rail)	$V_I =$ GND; see Figure 7						
		$I_{SW} = 4$ mA; $V_{CC} = 1.65$ V to 1.95 V	-	8.2	18	-	27	Ω
		$I_{SW} = 8$ mA; $V_{CC} = 2.3$ V to 2.7 V	-	7.1	16	-	24	Ω
		$I_{SW} = 12$ mA; $V_{CC} = 2.7$ V	-	6.9	14	-	21	Ω
		$I_{SW} = 24$ mA; $V_{CC} = 3.0$ V to 3.6 V	-	6.5	12	-	18	Ω
		$I_{SW} = 32$ mA; $V_{CC} = 4.5$ V to 5.5 V	-	5.8	10	-	15	Ω
		$V_I = V_{CC}$; see Figure 7						
		$I_{SW} = 4$ mA; $V_{CC} = 1.65$ V to 1.95 V	-	10.4	30	-	45	Ω
		$I_{SW} = 8$ mA; $V_{CC} = 2.3$ V to 2.7 V	-	7.6	20	-	30	Ω
		$I_{SW} = 12$ mA; $V_{CC} = 2.7$ V	-	7.0	18	-	27	Ω
		$I_{SW} = 24$ mA; $V_{CC} = 3.0$ V to 3.6 V	-	6.1	15	-	23	Ω
		$I_{SW} = 32$ mA; $V_{CC} = 4.5$ V to 5.5 V	-	4.9	10	-	15	Ω

Table 8. ON resistance ...continued

At recommended operating conditions; voltages are referenced to GND (ground 0 V); for graphs see [Figure 8](#) to [Figure 13](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
R _{ON(flat)}	ON resistance (flatness)	V _I = GND to V _{CC} ^[2]						
		I _{SW} = 4 mA; V _{CC} = 1.65 V to 1.95 V	-	26.0	-	-	-	Ω
		I _{SW} = 8 mA; V _{CC} = 2.3 V to 2.7 V	-	5.0	-	-	-	Ω
		I _{SW} = 12 mA; V _{CC} = 2.7 V	-	3.5	-	-	-	Ω
		I _{SW} = 24 mA; V _{CC} = 3.0 V to 3.6 V	-	2.0	-	-	-	Ω
		I _{SW} = 32 mA; V _{CC} = 4.5 V to 5.5 V	-	1.5	-	-	-	Ω

[1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.

[2] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V_{CC} and temperature.

10.3 ON resistance test circuit and graphs

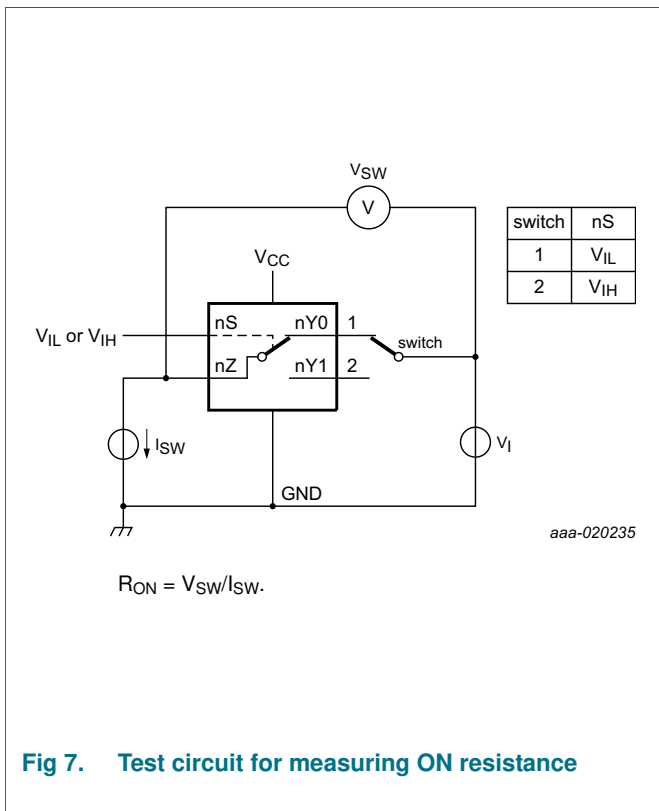
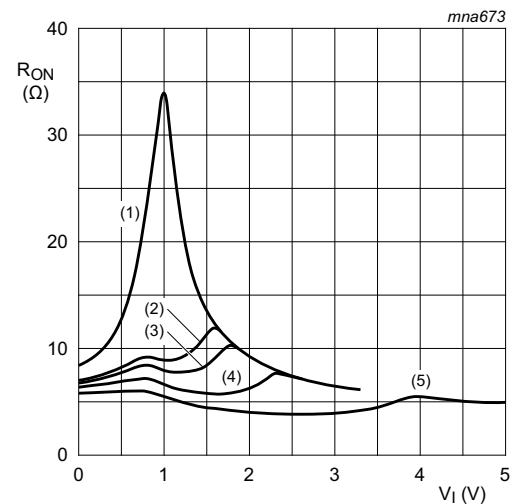
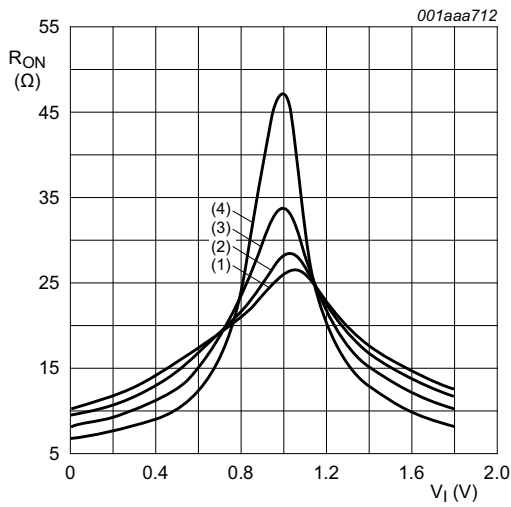


Fig 7. Test circuit for measuring ON resistance



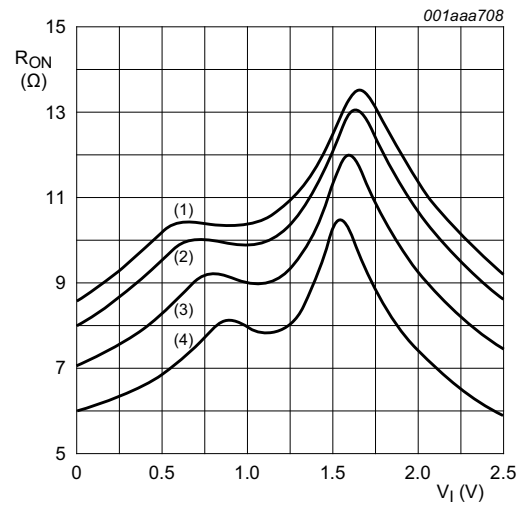
- (1) V_{CC} = 1.8 V.
- (2) V_{CC} = 2.5 V.
- (3) V_{CC} = 2.7 V.
- (4) V_{CC} = 3.3 V.
- (5) V_{CC} = 5.0 V.

Fig 8. Typical ON resistance as a function of input voltage; T_{amb} = 25 °C



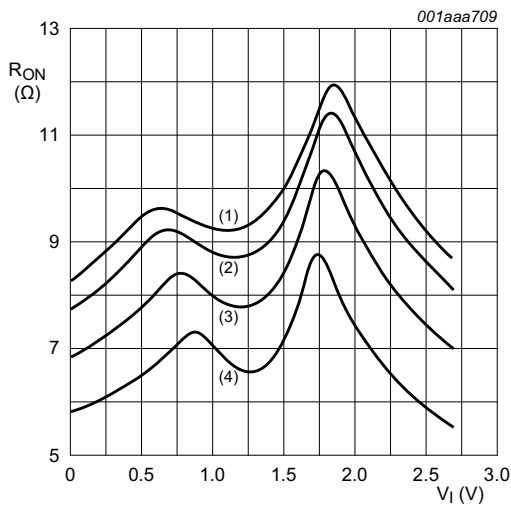
- (1) $T_{amb} = 125\text{ °C.}$
- (2) $T_{amb} = 85\text{ °C.}$
- (3) $T_{amb} = 25\text{ °C.}$
- (4) $T_{amb} = -40\text{ °C.}$

Fig 9. ON resistance as a function of input voltage;
 $V_{CC} = 1.8\text{ V}$



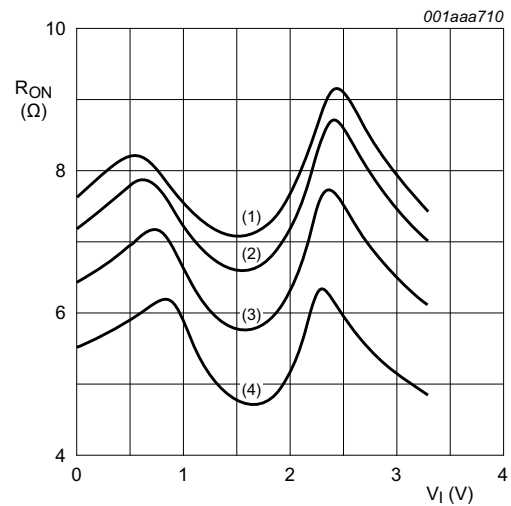
- (1) $T_{amb} = 125\text{ °C.}$
- (2) $T_{amb} = 85\text{ °C.}$
- (3) $T_{amb} = 25\text{ °C.}$
- (4) $T_{amb} = -40\text{ °C.}$

Fig 10. ON resistance as a function of input voltage;
 $V_{CC} = 2.5\text{ V}$



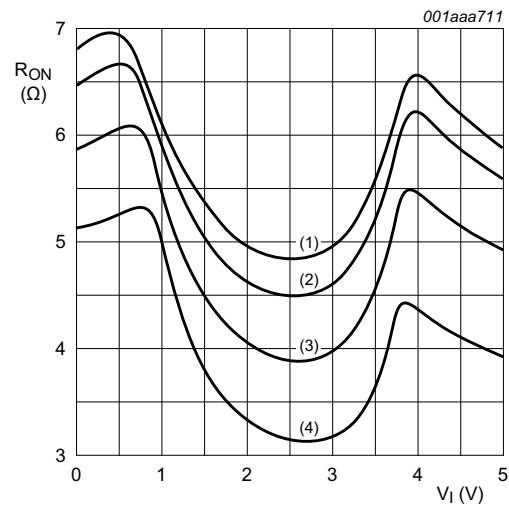
- (1) $T_{amb} = 125\text{ °C.}$
- (2) $T_{amb} = 85\text{ °C.}$
- (3) $T_{amb} = 25\text{ °C.}$
- (4) $T_{amb} = -40\text{ °C.}$

Fig 11. ON resistance as a function of input voltage;
 $V_{CC} = 2.7\text{ V}$



- (1) $T_{amb} = 125\text{ °C.}$
- (2) $T_{amb} = 85\text{ °C.}$
- (3) $T_{amb} = 25\text{ °C.}$
- (4) $T_{amb} = -40\text{ °C.}$

Fig 12. ON resistance as a function of input voltage;
 $V_{CC} = 3.3\text{ V}$



- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}$.
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}$.
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}$.
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}$.

Fig 13. ON resistance as a function of input voltage; $V_{CC} = 5.0\text{ V}$

11. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 17](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t_{pd}	propagation delay	nYn to nZ or nZ to nYn; see Figure 14 ^{[2][3]}						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	-	-	2	-	3.0	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	-	1.2	-	2.0	ns
		$V_{CC} = 2.7 \text{ V}$	-	-	1.0	-	1.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	-	0.8	-	1.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	0.6	-	1.0	ns
t_{en}	enable time	nS to nYn; see Figure 15 ^[4]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1	8.7	24	1	26.5	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1	5.3	14	1	15.5	ns
		$V_{CC} = 2.7 \text{ V}$	1	4.9	14	1	15.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	0.5	4	7.6	0.5	8.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	0.5	3	5.7	0.5	6.6	ns
t_{dis}	disable time	nS to nYn; see Figure 15 ^[5]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	2.5	6	13	2.5	14.5	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	2	4.4	7.5	2	8.5	ns
		$V_{CC} = 2.7 \text{ V}$	1.5	4.2	7.5	1.5	8.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.5	3.6	5.3	1.5	6	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	0.8	2.9	3.8	0.8	4.5	ns
t_{b-m}	break-before-make time	$C_L = 35 \text{ pF}$; $R_L = 50 \Omega$; see Figure 16 ^[6]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.5	-	-	0.5	-	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.5	-	-	0.5	-	ns
		$V_{CC} = 2.7 \text{ V}$	0.5	-	-	0.5	-	ns
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	0.5	-	-	0.5	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	0.5	-	-	0.5	-	ns

[1] Typical values are measured at $T_{amb} = 25 \text{ °C}$ and nominal V_{CC} .

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

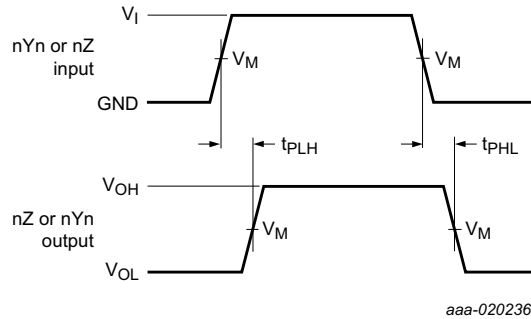
[3] Propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified capacitance when driven by an ideal voltage source (zero output impedance).

[4] t_{en} is the same as t_{PZH} and t_{PZL} .

[5] t_{dis} is the same as t_{PLZ} and t_{PHZ} .

[6] Break-before-make specified by design.

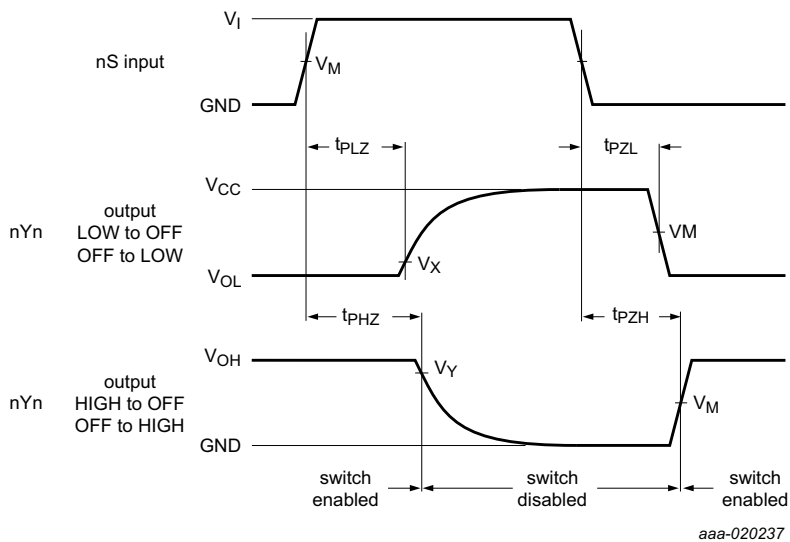
11.1 Waveforms and test circuits



Measurement points are given in [Table 10](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 14. Input (nY or nZ) to output (nZ or nY) propagation delays



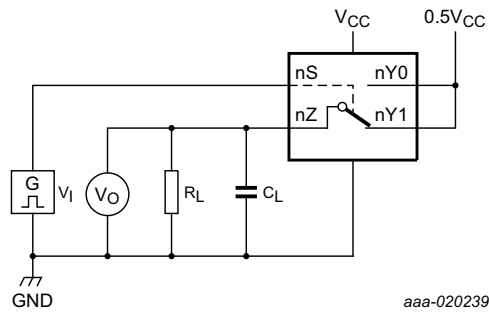
Measurement points are given in [Table 10](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

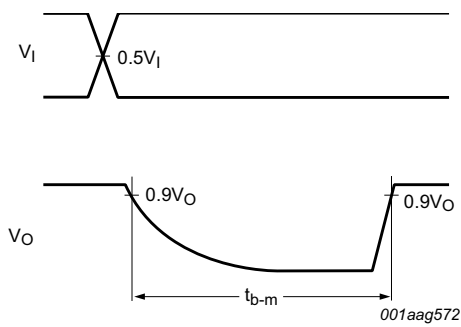
Fig 15. Enable and disable times

Table 10. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.65 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$

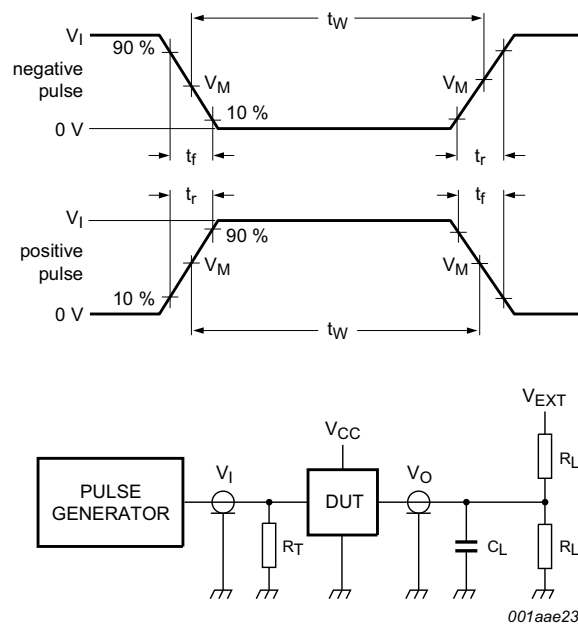


a. Test circuit



b. Input and output measurement points

Fig 16. Test circuit for measuring break-before-make timing



Test data is given in [Table 11](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

Fig 17. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	50 pF	500 Ω	open	GND	$2V_{CC}$
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	50 pF	500 Ω	open	GND	$2V_{CC}$
2.7 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2V_{CC}$
3 V to 3.6 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2V_{CC}$
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2V_{CC}$

11.2 Additional dynamic characteristics

Table 12. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	$f_i = 600\text{ Hz to }20\text{ kHz}; R_L = 600\text{ }\Omega; C_L = 50\text{ pF}; V_i = 0.5\text{ V (p-p)}$; see Figure 18				
		$V_{CC} = 1.65\text{ V}$	-	0.260	-	%
		$V_{CC} = 2.3\text{ V}$	-	0.078	-	%
		$V_{CC} = 3.0\text{ V}$	-	0.078	-	%
$f_{(-3\text{dB})}$	-3 dB frequency response	$R_L = 50\text{ }\Omega$; see Figure 19				
		$V_{CC} = 1.65\text{ V}$	-	200	-	MHz
		$V_{CC} = 2.3\text{ V}$	-	300	-	MHz
		$V_{CC} = 3.0\text{ V}$	-	300	-	MHz
α_{iso}	isolation (OFF-state)	$R_L = 50\text{ }\Omega; C_L = 5\text{ pF}; f_i = 10\text{ MHz}$; see Figure 20				
		$V_{CC} = 1.65\text{ V}$	-	-42	-	dB
		$V_{CC} = 2.3\text{ V}$	-	-42	-	dB
		$V_{CC} = 3.0\text{ V}$	-	-40	-	dB
Xtalk	crosstalk	between switches; $f_i = 10\text{ MHz}$; see Figure 21				
		$V_{CC} = 1.65\text{ V}$	-	-54	-	dB
		$V_{CC} = 2.3\text{ V}$	-	-54	-	dB
		$V_{CC} = 3.0\text{ V}$	-	-54	-	dB
Q_{inj}	charge injection	$C_L = 0.1\text{ nF}; V_{gen} = 0\text{ V}; R_{gen} = 0\text{ }\Omega; f_i = 1\text{ MHz}; R_L = 1\text{ M}\Omega$; see Figure 22				
		$V_{CC} = 1.8\text{ V}$	-	3.3	-	pC
		$V_{CC} = 2.5\text{ V}$	-	4.1	-	pC
		$V_{CC} = 3.3\text{ V}$	-	5.0	-	pC
		$V_{CC} = 4.5\text{ V}$	-	6.4	-	pC
	$V_{CC} = 5.5\text{ V}$	-	7.5	-	pC	

11.3 Test circuits

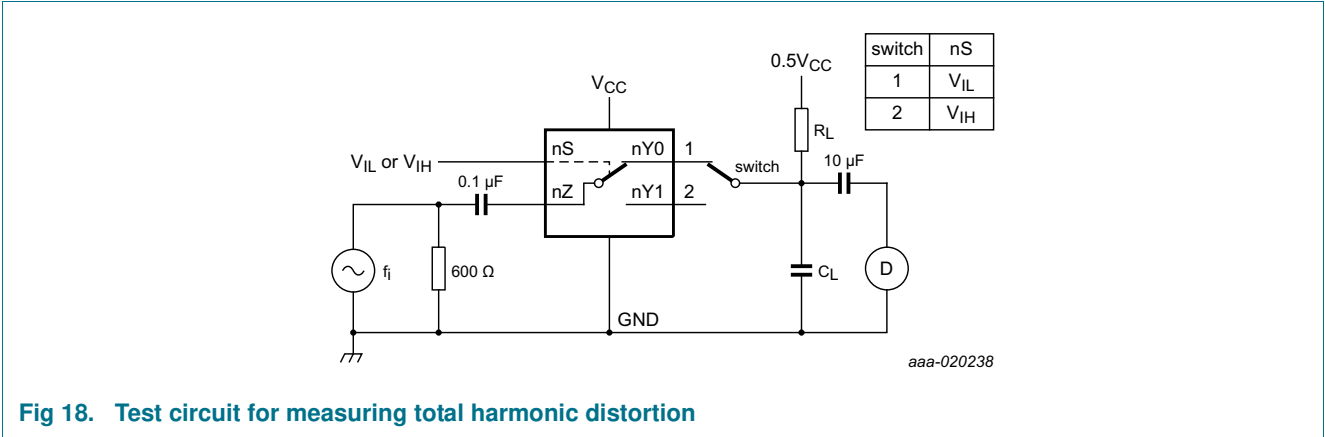
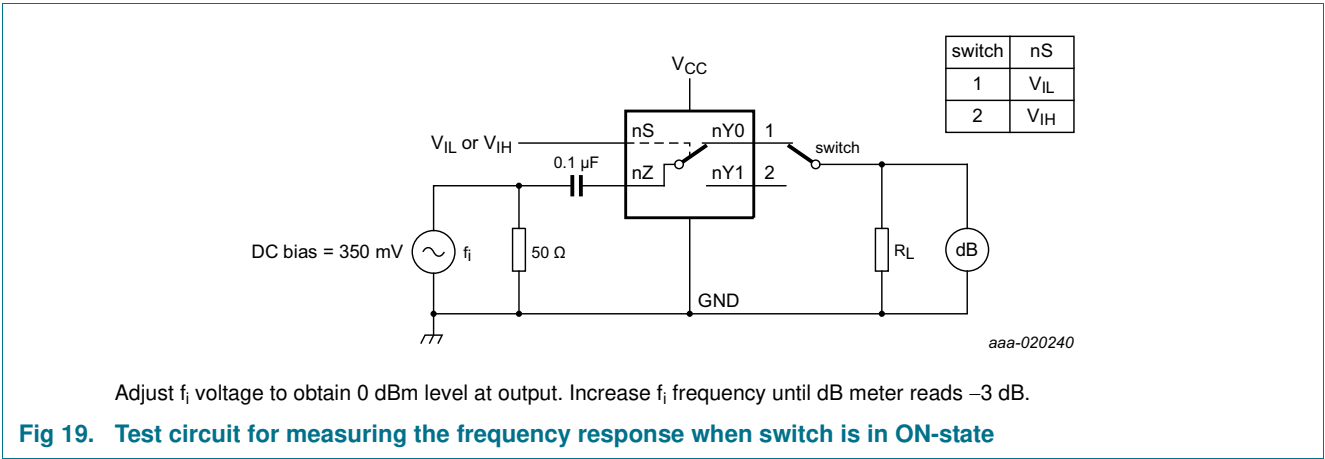
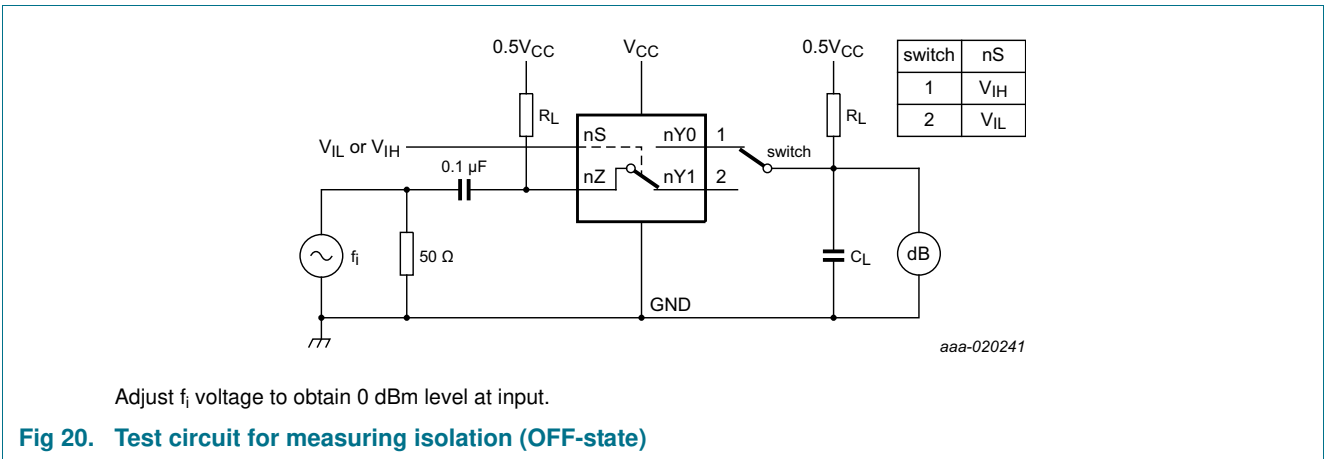


Fig 18. Test circuit for measuring total harmonic distortion



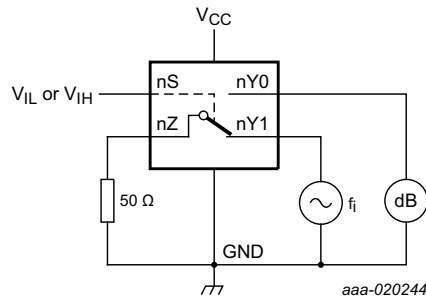
Adjust f_i voltage to obtain 0 dBm level at output. Increase f_i frequency until dB meter reads -3 dB.

Fig 19. Test circuit for measuring the frequency response when switch is in ON-state



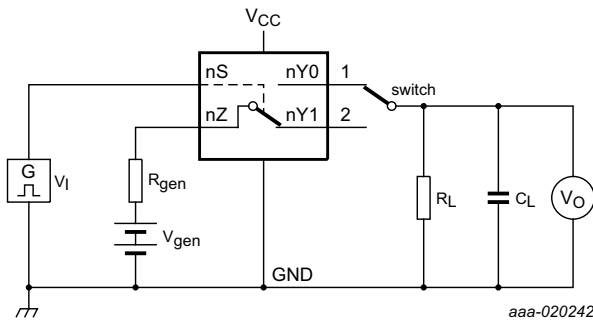
Adjust f_i voltage to obtain 0 dBm level at input.

Fig 20. Test circuit for measuring isolation (OFF-state)

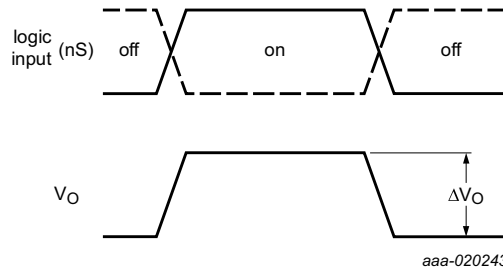


Adjust f_i voltage to obtain 0 dBm level at input.

Fig 21. Test circuit for measuring crosstalk



a. Test circuit



b. Input and output pulse definitions

$$Q_{inj} = \Delta V_O \times C_L$$

ΔV_O = output voltage variation.

R_{gen} = generator resistance.

V_{gen} = generator voltage.

Fig 22. Test circuit for measuring charge injection

12. Package outline

TSSOP10: plastic thin shrink small outline package; 10 leads; body width 3 mm

SOT552-1

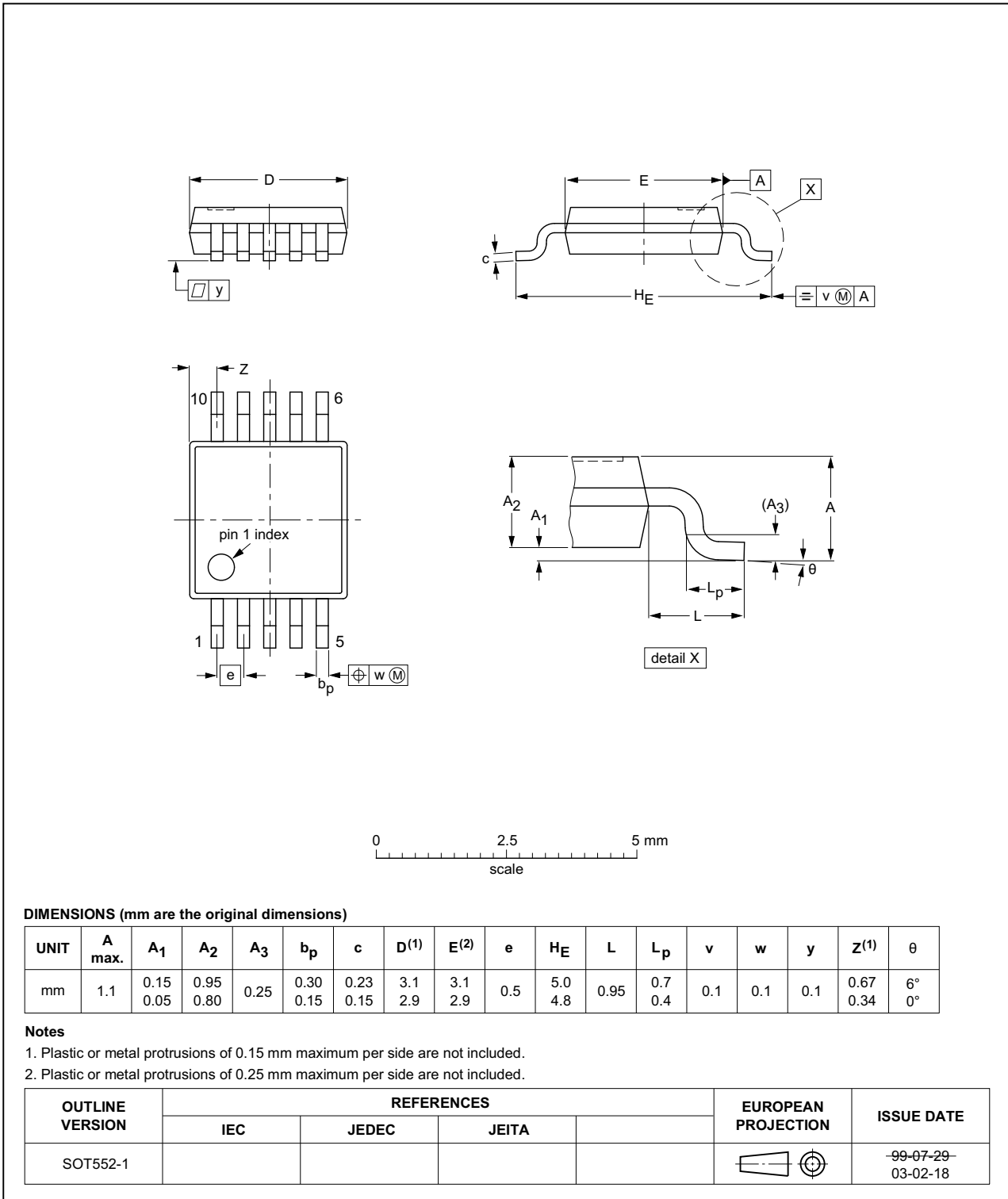


Fig 23. Package outline SOT552-1 (TSSOP10)

XQFN10: plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.55 x 2.00 x 0.50 mm

SOT1049-3

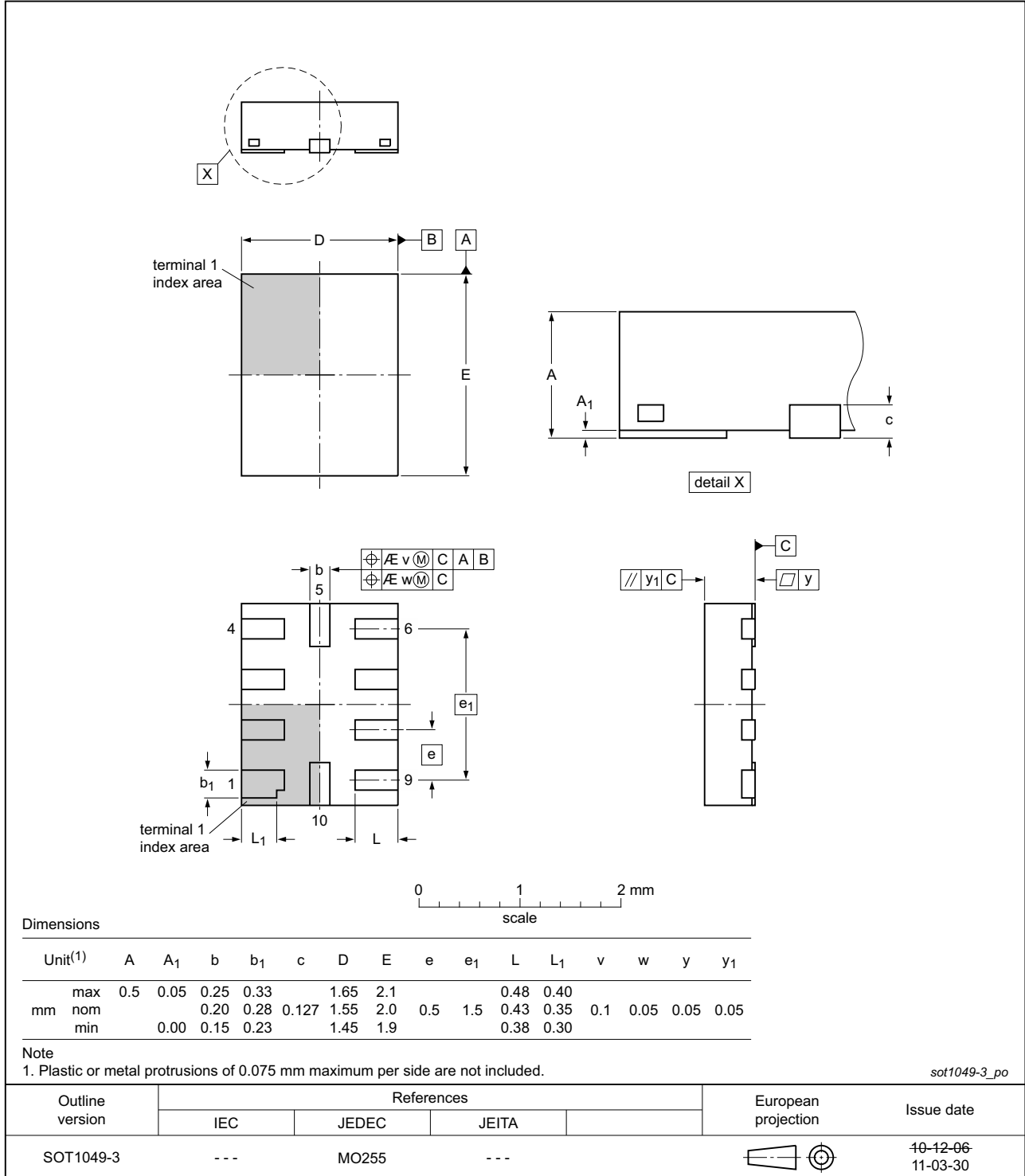


Fig 24. Package outline SOT1049-3 (XQFN10)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC2G3157 v.2	20161215	Product data sheet	-	74LVC2G3157 v.1
Modifications:	• Table 7 : The maximum limits for leakage current and supply current have changed.			
74LVC2G3157 v.1	20151214	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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17. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
4	Marking	2
5	Functional diagram	2
6	Pinning information	3
6.1	Pinning	3
6.2	Pin description	3
7	Functional description	3
8	Limiting values	4
9	Recommended operating conditions	4
10	Static characteristics	5
10.1	Test circuits	6
10.2	ON resistance	6
10.3	ON resistance test circuit and graphs	7
11	Dynamic characteristics	10
11.1	Waveforms and test circuits	11
11.2	Additional dynamic characteristics	14
11.3	Test circuits	15
12	Package outline	17
13	Abbreviations	19
14	Revision history	19
15	Legal information	20
15.1	Data sheet status	20
15.2	Definitions	20
15.3	Disclaimers	20
15.4	Trademarks	21
16	Contact information	21
17	Contents	22