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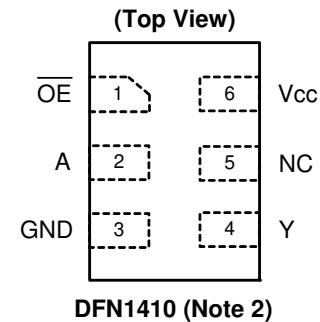
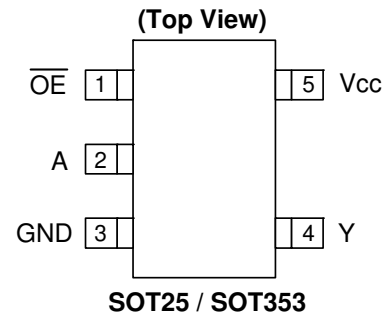
### Description

The 74LVCE1G125 is a single non-inverting buffer/bus driver with a 3-state output. The output enters a high impedance state when a HIGH-level is applied to the output enable (OE) pin. The device is designed for operation with a power supply range of 1.4V to 5.5V. The inputs are tolerant to 5.5V allowing this device to be used in a mixed voltage environment. The device is fully specified for partial power down applications using I<sub>OFF</sub>. The I<sub>OFF</sub> circuitry disables the output preventing damaging current backflow when the device is powered down.

### Features

- Extended Supply Voltage Range from 1.4 to 5.5V
- Switching speed characterized for operation at 1.5V
- Offers 30% speed improvement over LVC at 1.8V.
- ± 24mA Output Drive at 3.3V
- CMOS low power consumption
- IOFF Supports Partial-Power-Down Mode Operation
- Inputs accept up to 5.5V
- ESD Protection Tested per JESD 22
  - Exceeds 200-V Machine Model (A115-A)
  - Exceeds 2000-V Human Body Model (A114-A)
- Latch-Up Exceeds 100mA per JESD 78, Class II
- Range of Package Options
- Direct Interface with TTL Levels
- SOT25, SOT353 and DFN1410: Assembled with “Green” Molding Compound (no Br, Sb)
- Lead Free Finish/ RoHS Compliant (Note 1)

### Pin Assignments



### Applications

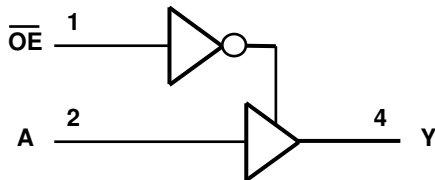
- Voltage Level Shifting
- Bus Driver / Repeater
- Power Down Signal Isolation
- General Purpose Logic
- Wide array of products such as.
  - PCs, networking, notebooks, netbooks, PDAs
  - Computer peripherals, hard drives, CD/DVD ROM
  - TV, DVD, DVR, set top box
  - Cell Phones, Personal Navigation / GPS
  - MP3 players ,Cameras, Video Recorders

Notes: 1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied. Please visit our website at [http://www.diodes.com/products/lead\\_free.html](http://www.diodes.com/products/lead_free.html).  
 2. Pin 2 and pin 5 of the DFN1410 package are internally connected.

**Pin Descriptions**

Pin Name	Description
$\overline{OE}$	Output Enable (active low)
A	Data Input
GND	Ground
Y	Data Output
Vcc	Supply Voltage

**Logic Diagram**



**Function Table**

Inputs		Output
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

### Absolute Maximum Ratings (Note 3)

Symbol	Description	Rating	Unit
ESD HBM	Human Body Model ESD Protection	2	KV
ESD MM	Machine Model ESD Protection	200	V
$V_{CC}$	Supply Voltage Range	-0.5 to 6.5	V
$V_I$	Input Voltage Range	-0.5 to 6.5	V
$V_o$	Voltage applied to output in high impedance or $I_{OFF}$ state	-0.5 to 6.5	V
$V_o$	Voltage applied to output in high or low state	-0.3 to $V_{CC} + 0.5$	V
$I_{IK}$	Input Clamp Current $V_I < 0$	-50	mA
$I_{OK}$	Output Clamp Current	-50	mA
$I_o$	Continuous output current	$\pm 50$	mA
	Continuous current through Vdd or GND	$\pm 100$	mA
$T_J$	Operating Junction Temperature	-40 to 150	$^{\circ}C$
$T_{STG}$	Storage Temperature	-65 to 150	$^{\circ}C$

Note: 3. Stresses beyond the absolute maximum may result in immediate failure or reduced reliability. These are stress values and device operation should be within recommend values.

### Recommended Operating Conditions (Note 4)

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	Operating Voltage	Operating	1.4	5.5	V
		Data retention only	1.2		V
V <sub>IH</sub>	High-level Input Voltage	V <sub>CC</sub> = 1.4 V to 1.95 V	0.65 X V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
		V <sub>CC</sub> = 3 V to 3.6 V	2		
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 X V <sub>CC</sub>		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.4 V to 1.95 V		0.35 X V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	
		V <sub>CC</sub> = 3 V to 3.6 V		0.8	
		V <sub>CC</sub> = 4.5 V to 5.5 V		0.3 X V <sub>CC</sub>	
V <sub>I</sub>	Input Voltage	0	5.5	V	
V <sub>O</sub>	Output Voltage	0	V <sub>CC</sub>	V	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> =1.4 V		-3	mA
		V <sub>CC</sub> = 1.65 V		-4	
		V <sub>CC</sub> = 2.3 V		-8	
		V <sub>CC</sub> = 3 V		-16	
		V <sub>CC</sub> = 4.5 V		-24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> =1.4 V		3	mA
		V <sub>CC</sub> = 1.65 V		4	
		V <sub>CC</sub> = 2.3 V		8	
		V <sub>CC</sub> = 3 V		16	
		V <sub>CC</sub> = 4.5 V		24	
Δt/ΔV	Input transition rise or fall rate	V <sub>CC</sub> = 1.4 to 3V		20	ns/V
		V <sub>CC</sub> = 3.3 V ± 0.3 V		10	
		V <sub>CC</sub> = 5 V ± 0.5 V		5	
T <sub>A</sub>	Operating free-air temperature	-40	85	°C	

Note: 4. Unused inputs should be held at V<sub>CC</sub> or Ground.

### Electrical Characteristics (All typical values are at $V_{CC} = 3.3V$ , $T_A = 25^\circ C$ )

Over recommended free-air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	Vcc	Min	Typ.	Max	Unit
$V_{OH}$	High Level Output Voltage	$I_{OH} = -100\mu A$	1.4 V to 5.5V	$V_{CC} - 0.1$			V
		$I_{OH} = -3mA$	1.4 V	1.05			
		$I_{OH} = -4mA$	1.65 V	1.2			
		$I_{OH} = -8mA$	2.3V	1.9			
		$I_{OH} = -16mA$	3 V	2.4			
		$I_{OH} = -24mA$		2.3			
		$I_{OH} = -32mA$	4.5 V	3.8			
$V_{OL}$	High-level Input Voltage	$I_{OL} = 100\mu A$	1.4 V to 5.5V			0.1	V
		$I_{OL} = 3mA$	1.4V			.4	
		$I_{OL} = 4mA$	1.65 V			0.45	
		$I_{OL} = 8mA$	2.3V			0.3	
		$I_{OL} = 16mA$	3 V			0.4	
		$I_{OL} = 24mA$				0.55	
		$I_{OL} = 32mA$	4.5			0.55	
$I_I$	Input Current	$V_I = 5.5 V$ or GND	0 to 5.5 V			$\pm 5$	$\mu A$
$I_{OFF}$	Power Down Leakage Current	$V_I$ or $V_O = 5.5V$	0			$\pm 10$	$\mu A$
$I_{OZ}$	Z State Leakage Current	$V_O = 0$ to 5.5V	3.6V			10	$\mu A$
$I_{CC}$	Supply Current	$V_I = 5.5V$ of GND $I_O = 0$	1.4 V to 5.5V			10	$\mu A$
$\Delta I_{CC}$	Additional Supply Current	One input at $V_{CC} - 0.6 V$ Other inputs at $V_{CC}$ or GND	3 V to 5.5V			500	$\mu A$
$C_i$	Input Capacitance	$V_i = V_{CC} -$ or GND	3.3		3.5		pF
$\theta_{JA}$	Thermal Resistance Junction-to-Ambient	SOT25	(Note 5)		204		$^\circ C/W$
		SOT353	(Note 5)		371		
		DFN1410	(Note 5)		430		
$\theta_{JC}$	Thermal Resistance Junction-to-Case	SOT25	(Note 5)		52		$^\circ C/W$
		SOT353	(Note 5)		143		
		DFN1410	(Note 5)		190		

Note: 5. Test condition for SOT25, SOT353 and DFN1410: Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

### Switching Characteristics

Over recommended free-air temperature range, CL = 15pF (see Figure 1)

Parameter	From (Input)	TO (OUTPUT)	Vcc = 1.5 V ± 0.1V		Vcc = 1.8 V ± 0.15V		Vcc = 2.5 V ± 0.2V		Vcc = 3.3 V ± 0.3V		Vcc = 5 V ± 0.5V		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>pd</sub>	A	Y	1.9	6.9	1.3	4.8	0.5	3.6	0.4	3	0.4	3	ns

Over recommended free-air temperature range, CL = 30 or 50pF as noted (see Figure 2)

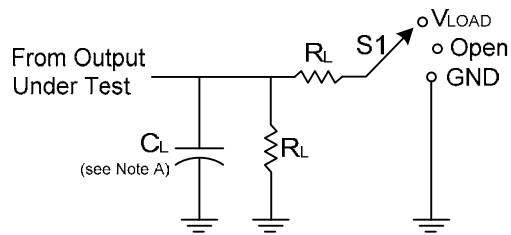
Parameter	From (Input)	TO (OUTPUT)	Vcc = 1.5 V ± 0.1V		Vcc = 1.8 V ± 0.15V		Vcc = 2.5 V ± 0.2V		Vcc = 3.3 V ± 0.3V		Vcc = 5 V ± 0.5V		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>pd</sub>	A	Y	2.8	9	1.9	6.3	0.9	4.4	0.8	3.6	0.9	3.6	ns
t <sub>en</sub>	$\overline{\text{OE}}$	Y	3.3	10.1	2.3	7	1.2	5.2	0.8	4.3	0.9	4.5	
t <sub>dis</sub>	$\overline{\text{OE}}$	Y	1.3	9.2	0.9	6.4	0.8	4	0.8	4.1	0.9	3.7	

### Operating Characteristics

T<sub>A</sub> = 25 °C

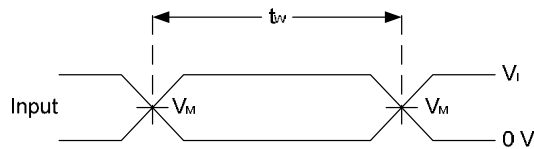
Parameter			Test Conditions	Vcc = 1.5 V	Vcc = 1.8 V	Vcc = 2.5 V	Vcc = 3.3 V	Vcc = 5 V	Unit
				TYP	TYP	TYP	TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance	Outputs enabled	f = 10 MHz	20	20	20	21	22	pF
		Outputs disabled		2	2	2	2	4	

**Parameter Measurement Information**

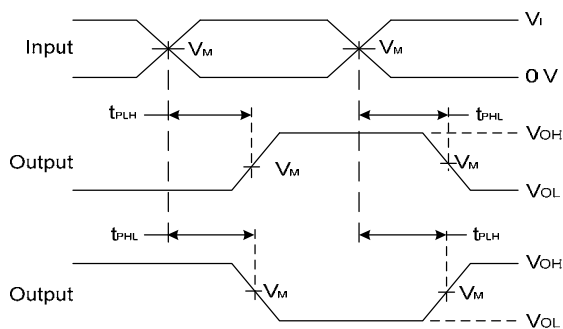


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{load}$
$t_{PHZ}/t_{PZH}$	GND

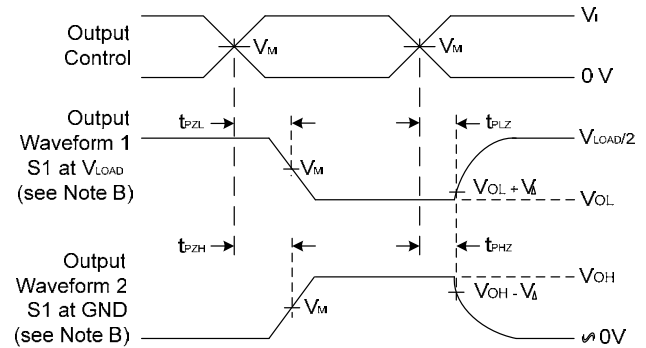
$V_{CC}$	Inputs		$V_M$	$C_L$	$R_L$
	$V_I$	$t_r/t_f$			
$1.5V \pm 0.1V$	$V_{CC}$	$\leq 2ns$	$V_{CC}/2$	15pF	1M $\Omega$
$1.8V \pm 0.15V$	$V_{CC}$	$\leq 2ns$	$V_{CC}/2$	15pF	1M $\Omega$
$2.5V \pm 0.2V$	$V_{CC}$	$\leq 2ns$	$V_{CC}/2$	15pF	1M $\Omega$
$3.3V \pm 0.3V$	3V	$\leq 2.5ns$	1.5V	15pF	1M $\Omega$
$5V \pm 0.5V$	$V_{CC}$	$\leq 2.5ns$	$V_{CC}/2$	15pF	1M $\Omega$



**Voltage Waveform Pulse Duration**



**Voltage Waveform Propagation Delay Times Inverting and Non Inverting Outputs**



**Voltage Waveform Enable and Disable Times Low and High Level Enabling**

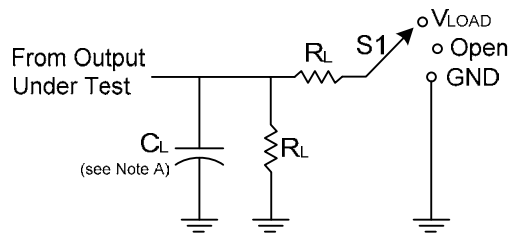
- Notes:
- A. Includes test lead and test apparatus capacitance.
  - B. All pulses are supplied at pulse repetition rate  $\leq 10$  MHz.
  - C. Inputs are measured separately one transition per measurement.
  - D.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - E.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{EN}$ .
  - F.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{PD}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

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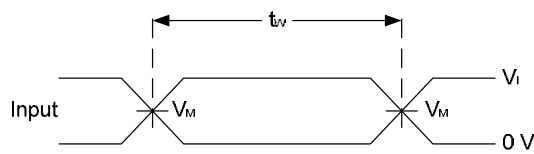


### Parameter Measurement Information (Continued)

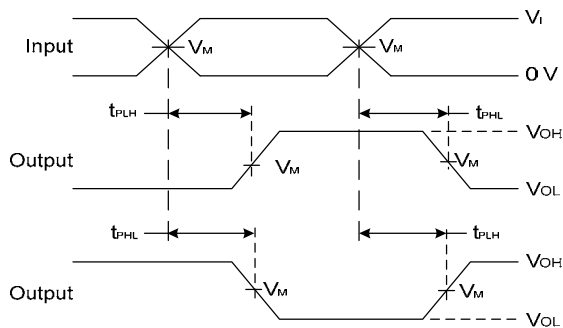


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	Vload
$t_{PHZ}/t_{PZH}$	GND

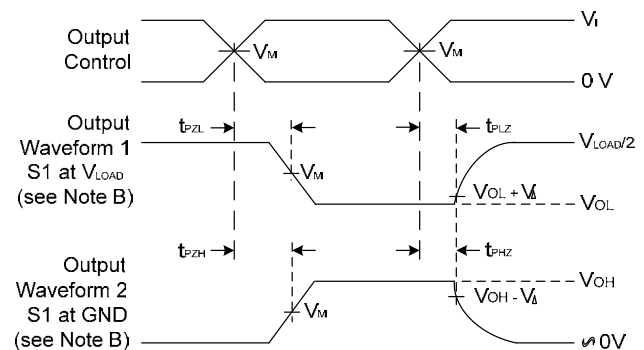
Vcc	Inputs		VM	CL	RL
	VI	tr/td			
1.5V±0.1V	VCC	≤2ns	VCC/2	30pF	1KΩ
1.8V±0.15V	VCC	≤2ns	VCC/2	30pF	1KΩ
2.5V±0.2V	VCC	≤2ns	VCC/2	30pF	500Ω
3.3V±0.3V	3V	≤2.5ns	1.5V	50pF	500Ω
5V±0.5V	VCC	≤2.5ns	VCC/2	50pF	500Ω



#### Voltage Waveform Pulse Duration



#### Voltage Waveform Propagation Delay Times Inverting and Non Inverting Outputs

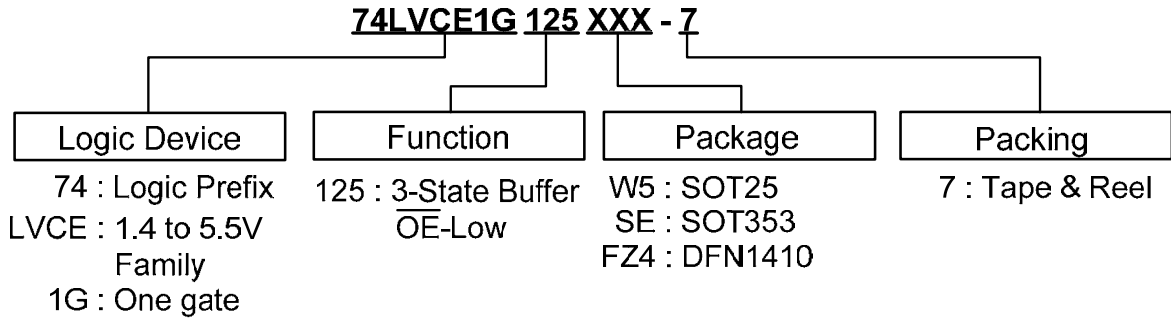


#### Voltage Waveform Enable and Disable Times Low and High Level Enabling

- Notes:
- A. Includes test lead and test apparatus capacitance.
  - B. All pulses are supplied at pulse repetition rate ≤ 10 MHz.
  - C. Inputs are measured separately one transition per measurement.
  - D.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - E.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{EN0}$ .
  - F.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{PD}$ .

Figure 2. Load Circuit and Voltage Waveforms

### Ordering Information



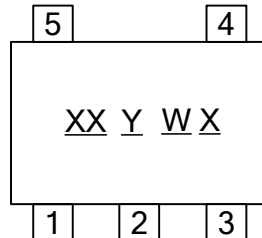
Device	Package Code	Packaging (Note 5)	7" Tape and Reel	
			Quantity	Part Number Suffix
74LVCE1G125W5-7	W6	SOT25	3000/Tape & Reel	-7
74LVCE1G125SE-7	SE	SOT353	3000/Tape & Reel	-7
74LVCE1G125FZ4-7	FZ4	DFN1410	5000/Tape & Reel	-7

Note: 6. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at <http://www.diodes.com/datasheets/ap02001.pdf>.

### Marking Information

#### (1) SOT25 and SOT353

(Top View)

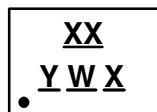


XX : Identification code  
Y : Year 0~9  
W : Week : A~Z : 1~26 week;  
a~z : 27~52 week; z represents  
52 and 53 week  
X : A~Z : Internal code

Part Number	Package	Identification Code
74LVCE1G125W5	SOT25	PY
74LVCE1G125SE	SOT353	PY

#### (2) DFN1410

(Top View)

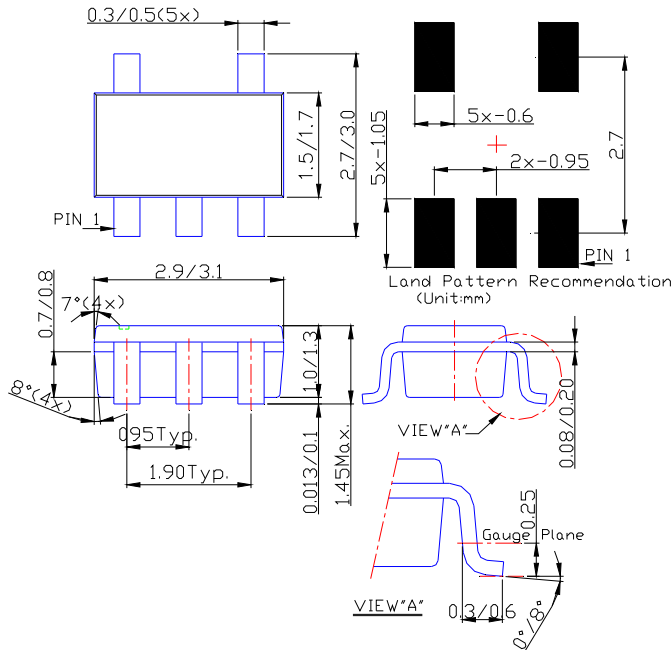


XX : Identification Code  
Y : Year : 0~9  
W : Week : A~Z : 1~26 week;  
a~z : 27~52 week; z represents  
52 and 53 week  
X : A~Z : Internal code

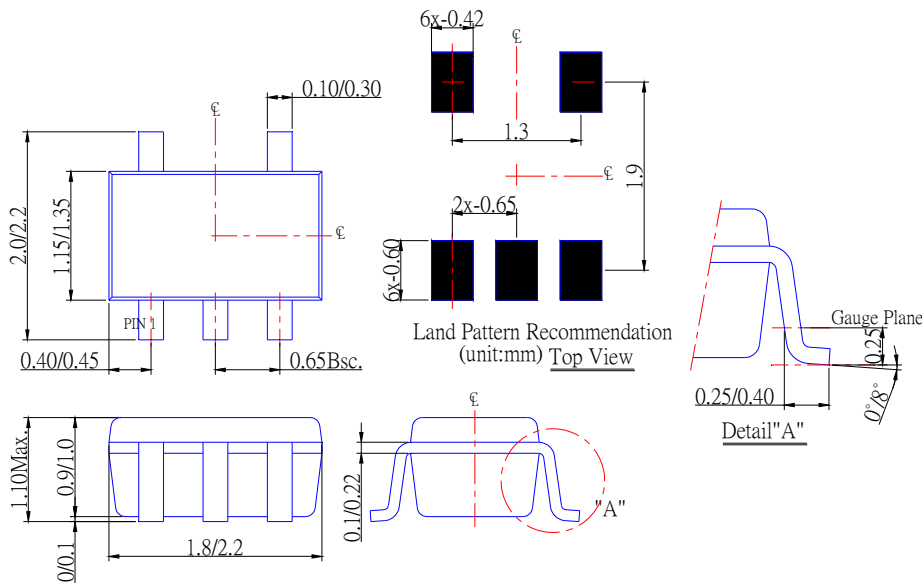
Part Number	Package	Identification Code
74LVCE1G125FZ4	DFN1410	PY

**Package Outline Dimensions (All Dimensions in mm)**

**(1) Package Type: SOT25**



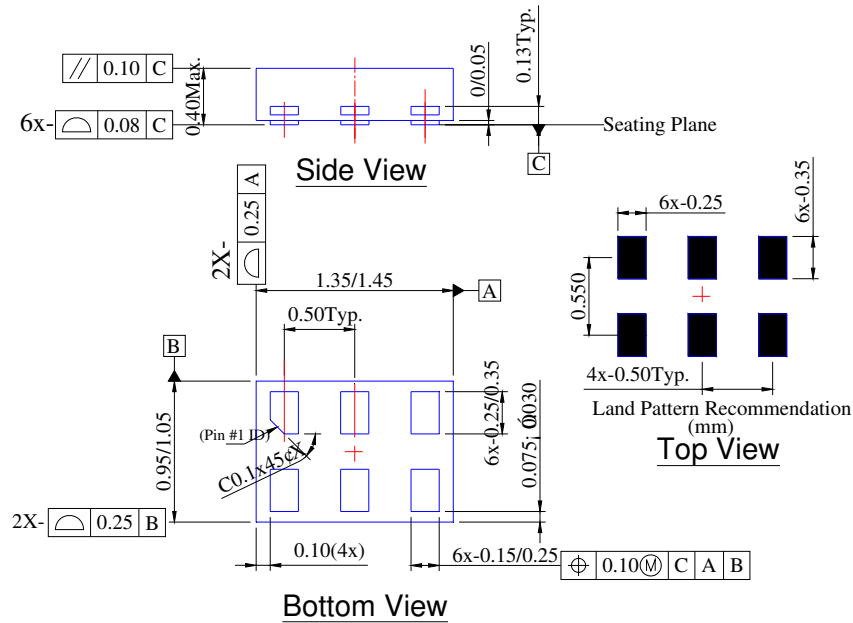
**(2) Package Type: SOT353**



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**Package Outline Dimensions (All Dimensions in mm)**

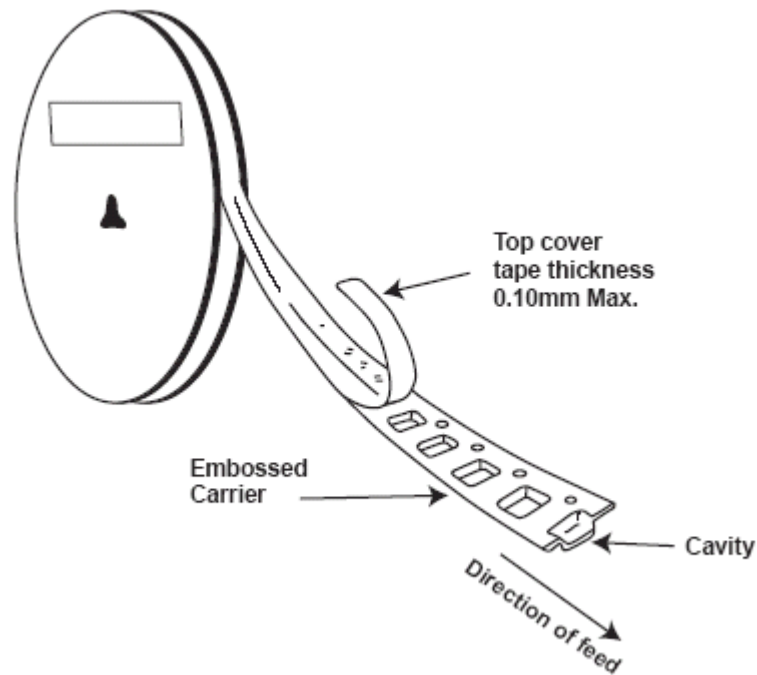
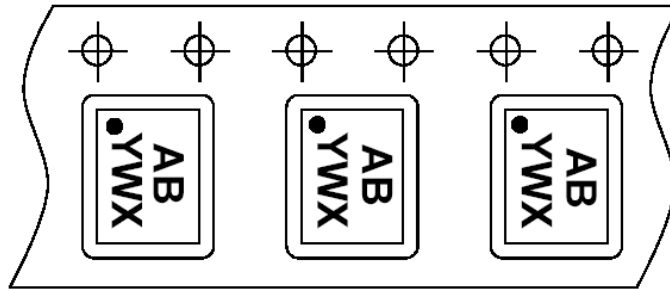
(3) Package Type: DFN1410



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**Taping Orientation (Note 7)**

For DFN1410



Note: 7. The taping orientation of the other package type can be found on our website at <http://www.diodes.com/datasheets/ap02007.pdf>

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