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# 74LVT16245B; 74LVTH16245B

3.3 V 16-bit transceiver; 3-state

Rev. 10 — 1 March 2012

Product data sheet

## 1. General description

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The 74LVT16245B; 74LVTH16245B is a high-performance BiCMOS product designed for  $V_{CC}$  operation at 3.3 V.

This device is a 16-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an output enable input ( $\overline{nOE}$ ) for easy cascading and a direction input ( $nDIR$ ) for direction control.

## 2. Features and benefits

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- 16-bit bidirectional bus interface
- 3-state buffers
- Output capability: +64 mA and -32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- Latch-up protection:
  - ◆ JESD78B Class II exceeds 500 mA
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V

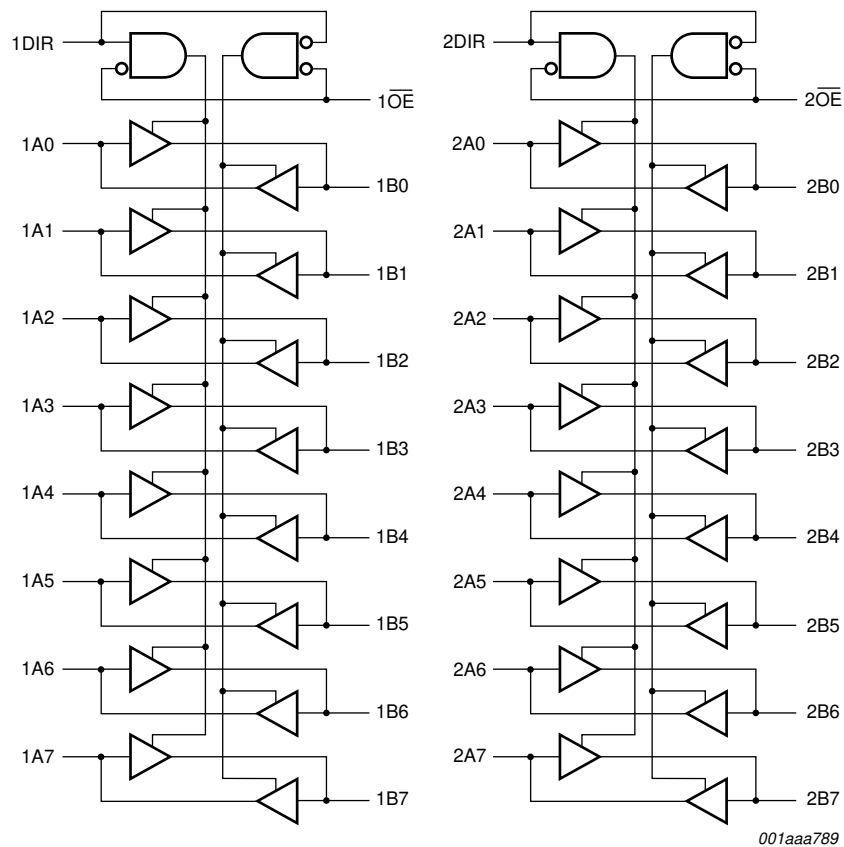


## 3. Ordering information

Table 1. Ordering information

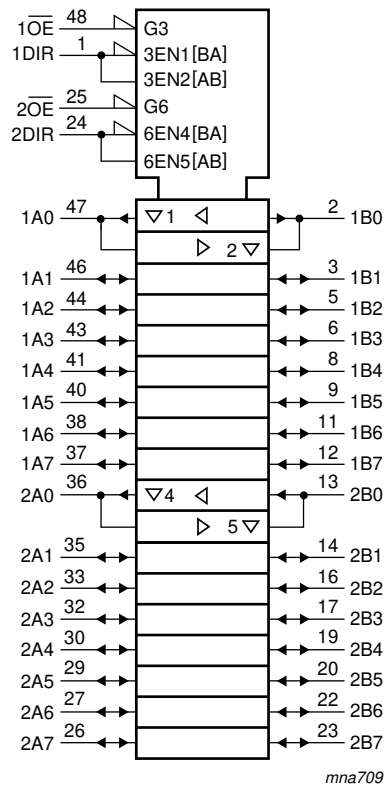
| Type number                       | Package           |         |   | Version   |
|-----------------------------------|-------------------|---------|---|-----------|
|                                   | Temperature range | Name    | Description   |           |
| 74LVT16245BDL<br>74LVTH16245BDL   | -40 °C to +85 °C  | SSOP48  | plastic shrink small outline package; 48 leads;<br>body width 7.5 mm  | SOT370-1  |
| 74LVT16245BDGG<br>74LVTH16245BDGG | -40 °C to +85 °C  | TSSOP48 | plastic thin shrink small outline package; 48 leads;<br>body width 6.1 mm   | SOT362-1  |
| 74LVT16245BEV                     | -40 °C to +85 °C  | VFPGA56 | plastic very thin fine-pitch ball grid array package;<br>56 balls; body 4.5 × 7 × 0.65 mm                               | SOT702-1  |
| 74LVT16245BBX<br>74LVTH16245BBX   | -40 °C to +125 °C | HXQFN60 | plastic compatible thermal enhanced extremely<br>thin quad flat package; no leads; 60 terminals;<br>body 4 × 6 × 0.5 mm | SOT1134-2 |

## 4. Functional diagram



Pin numbers are shown for SSOP48 and TSSOP48 packages only.

Fig 1. Logic symbol



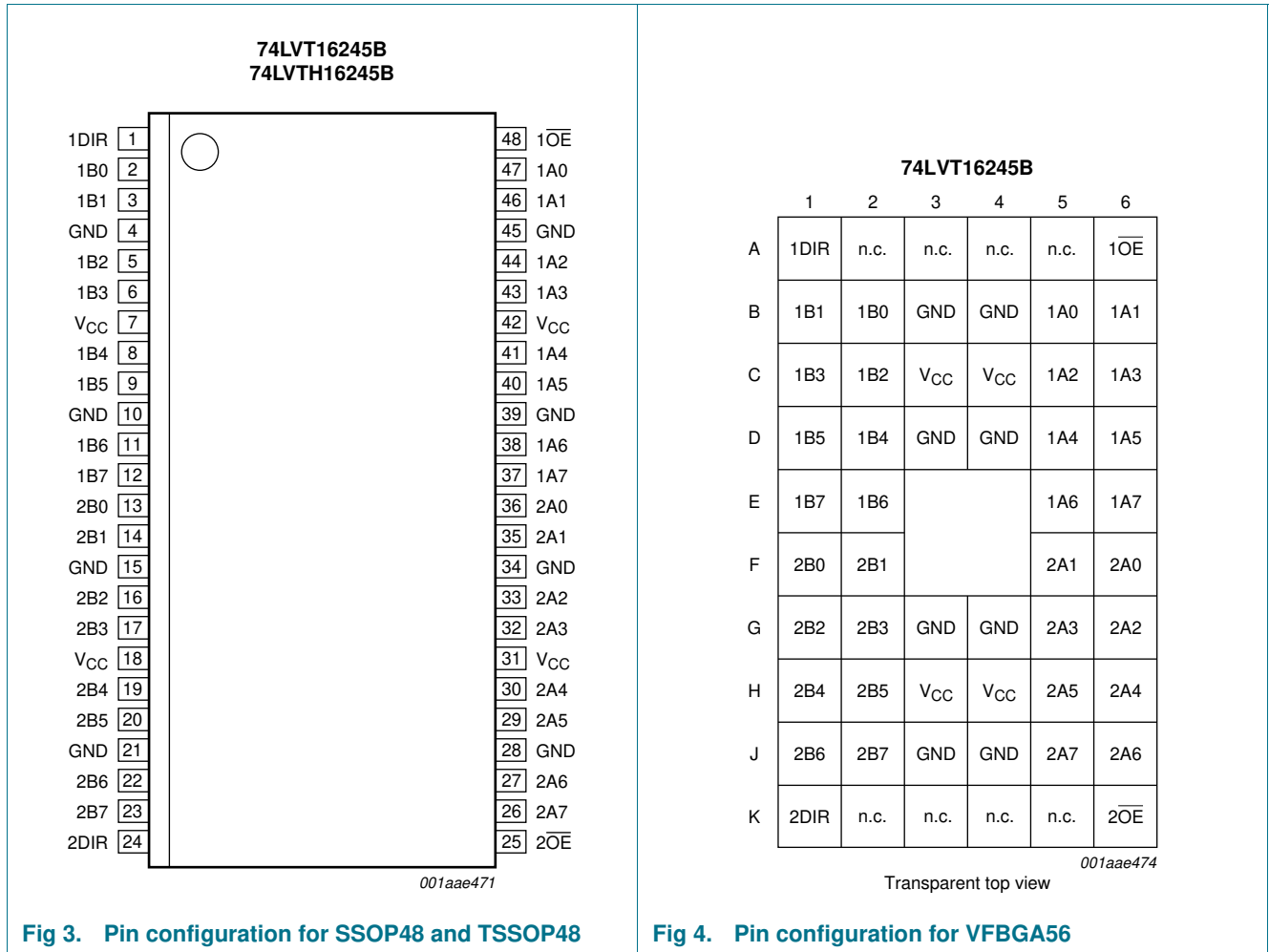
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Pin numbers are shown for SSOP48 and TSSOP48 packages only.

**Fig 2. IEC logic symbol**

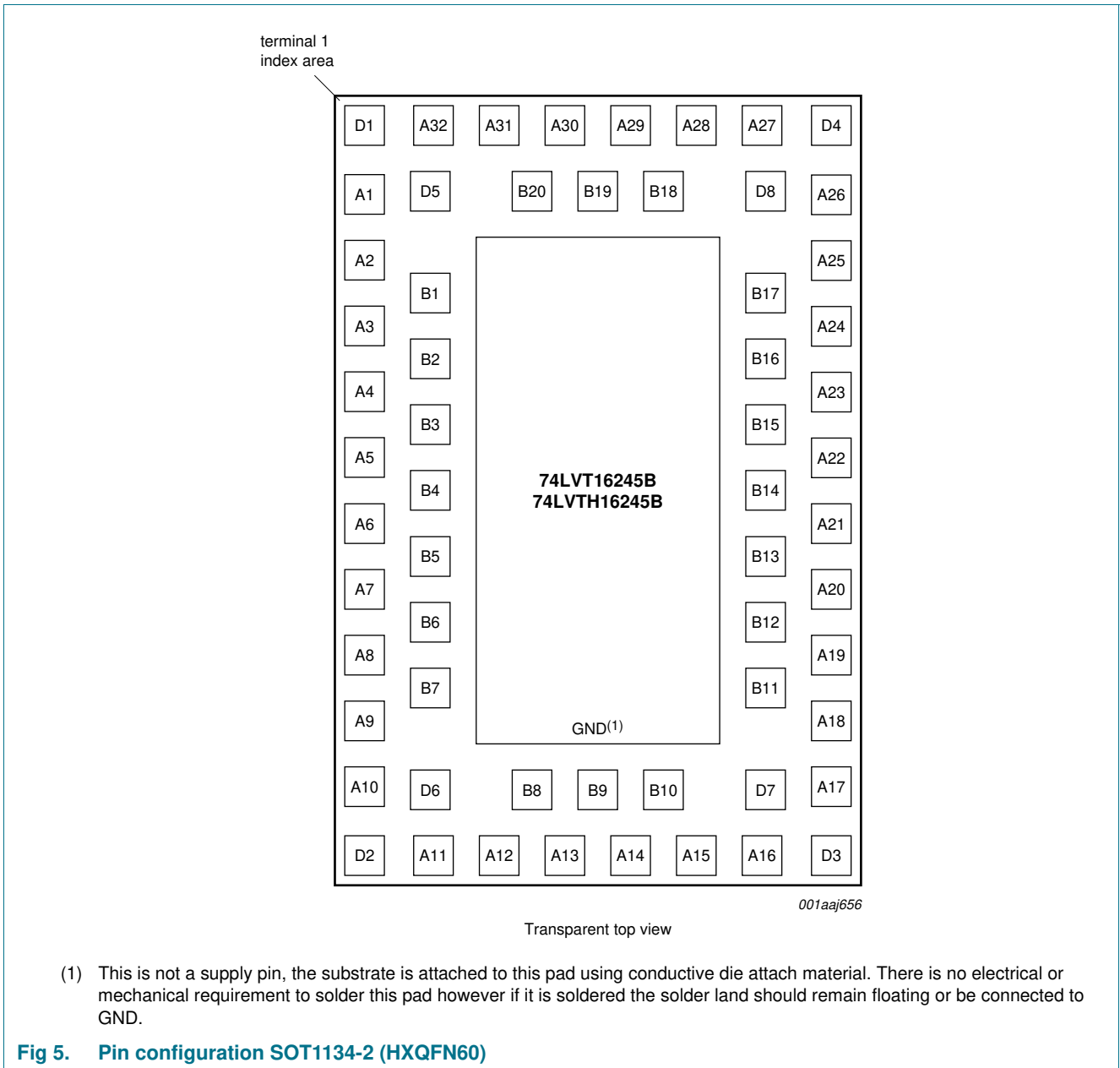
## 5. Pinning information

### 5.1 Pinning



**Fig 3. Pin configuration for SSOP48 and TSSOP48**

**Fig 4. Pin configuration for VFBGA56**



## 5.2 Pin description

Table 2. Pin description

| Symbol          | Pin                            |                                |  | Description                      |
|-----------------|--------------------------------|--------------------------------|--|----------------------------------|
|                 | SOT370-1 and SOT362-1          | SOT702-1                       | SOT1134-2  |                                  |
| 1DIR, 2DIR      | 1, 24                          | A1, K1                         | A30, A13   | direction control input          |
| 1B0 to 1B7      | 2, 3, 5, 6, 8, 9, 11, 12       | B2, B1, C2, C1, D2, D1, E2, E1 | B20, A31, D5, D1, A2, B2, B3, A5                     | data input/output                |
| 2B0 to 2B7      | 13, 14, 16, 17, 19, 20, 22, 23 | F1, F2, G1, G2, H1, H2, J1, J2 | A6, B5, B6, A9, D2, D6, A12, B8                      | data input/output                |
| GND             | 4, 10, 15, 21, 28, 34, 39, 45  | B3, D3, G3, J3, J4, G4, D4, B4 | A32, A3, A8, A11, A16, A19, A24, A27                 | ground (0 V)                     |
| V <sub>CC</sub> | 7, 18, 31, 42                  | C3, H3, H4, C4                 | A1, A10, A17, A26                                    | supply voltage                   |
| 1OE, 2OE        | 48, 25                         | A6, K6                         | A29, A14   | output enable input (active LOW) |
| 2A0 to 2A7      | 36, 35, 33, 32, 30, 29, 27, 26 | F6, F5, G6, G5, H6, H5, J6, J5 | A21, B13, B12, A18, D3, D7, A15, B10                 | data input/output                |
| 1A0 to 1A7      | 47, 46, 44, 43, 41, 40, 38, 37 | B5, B6, C5, C6, D5, D6, E5, E6 | B18, A28, D8, D4, A25, B16, B15, A22                 | data input/output                |
| n.c.            | -                              | A2, A3, A4, A5, K2, K3, K4, K5 | A4, A7, A20, A23, B1, B4, B7, B9, B11, B14, B17, B19 | not connected                    |

## 6. Functional description

### 6.1 Function table

Table 3. Function table [1]

| Control |      | Input/output     |                  |
|---------|------|------------------|------------------|
| nOE     | nDIR | nAn              | nBn              |
| L       | L    | output nAn = nBn | input            |
| L       | H    | input            | output nBn = nAn |
| H       | X    | Z                | Z                |

[1] H = HIGH voltage level;  
 L = LOW voltage level;  
 X = don't care;  
 Z = high-impedance OFF-state.



## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol           | Parameter               | Conditions                           | Min      | Max  | Unit |
|------------------|-------------------------|--------------------------------------|----------|------|------|
| V <sub>CC</sub>  | supply voltage          |                                      | -0.5     | +4.6 | V    |
| V <sub>I</sub>   | input voltage           |                                      | [1] -0.5 | +7.0 | V    |
| V <sub>O</sub>   | output voltage          | output in OFF-state or HIGH-state    | [1] -0.5 | +7.0 | V    |
| I <sub>IK</sub>  | input clamping current  | V <sub>I</sub> < 0 V                 | -50      | -    | mA   |
| I <sub>OK</sub>  | output clamping current | V <sub>O</sub> < 0 V                 | -50      | -    | mA   |
| I <sub>O</sub>   | output current          | output in LOW-state                  | -        | 128  | mA   |
|                  |                         | output in HIGH-state                 | -64      | -    | mA   |
| T <sub>stg</sub> | storage temperature     |                                      | -65      | +150 | °C   |
| T <sub>j</sub>   | junction temperature    |                                      | [2] -    | 150  | °C   |
| P <sub>tot</sub> | total power dissipation | T <sub>amb</sub> = -40 °C to +85 °C; |          |      |      |
|                  |                         | (T)SSOP48 package                    | [3] -    | 500  | mW   |
|                  |                         | VFBGA56 package                      | [4] -    | 1000 | mW   |
|                  |                         | HXQFN60 package                      | [4] -    | 1000 | mW   |

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

[3] Above 60 °C the value of P<sub>tot</sub> derates linearly with 5.5 mW/K.

[4] Above 70 °C the value of P<sub>tot</sub> derates linearly with 1.8 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol           | Parameter                           | Conditions   | Min | Typ | Max | Unit |
|------------------|-------------------------------------|--|-----|-----|-----|------|
| V <sub>CC</sub>  | supply voltage                      |  | 2.7 | -   | 3.6 | V    |
| V <sub>I</sub>   | input voltage                       |  | 0   | -   | 5.5 | V    |
| V <sub>IH</sub>  | HIGH-level input voltage            |  | 2.0 | -   | -   | V    |
| V <sub>IL</sub>  | LOW-level input voltage             |  | -   | -   | 0.8 | V    |
| I <sub>OH</sub>  | HIGH-level output current           |  | -32 | -   | -   | mA   |
| I <sub>OL</sub>  | LOW-level output current            | none   | -   | -   | 32  | mA   |
|                  |                                     | current duty cycle ≤ 50 %;<br>f <sub>i</sub> ≥ 1 kHz | -   | -   | 64  | mA   |
| T <sub>amb</sub> | ambient temperature                 | in free-air  | -40 | -   | +85 | °C   |
| Δt/ΔV            | input transition rise and fall rate | outputs enabled                                      | -   | -   | 10  | ns/V |

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol  | Parameter                          | Conditions   | Min                   | Typ             | Max  | Unit |
|---|------------------------------------|--|-----------------------|-----------------|------|------|
| <b>T<sub>amb</sub> = -40 °C to +85 °C<sup>[1]</sup></b> |                                    |  |                       |                 |      |      |
| V <sub>IK</sub>   | input clamping voltage             | V <sub>CC</sub> = 2.7 V; I <sub>IK</sub> = -18 mA  | -1.2                  | -0.85           | -    | V    |
| V <sub>OH</sub>   | HIGH-level output voltage          | I <sub>OH</sub> = -100 μA; V <sub>CC</sub> = 2.7 V to 3.6 V  | V <sub>CC</sub> - 0.2 | V <sub>CC</sub> | -    | V    |
|   |                                    | I <sub>OH</sub> = -8 mA; V <sub>CC</sub> = 2.7 V   | 2.4                   | 2.5             | -    | V    |
|   |                                    | I <sub>OH</sub> = -32 mA; V <sub>CC</sub> = 3.0 V  | 2.0                   | 2.3             | -    | V    |
| V <sub>OL</sub>   | LOW-level output voltage           | V <sub>CC</sub> = 2.7 V  |                       |                 |      |      |
|   |                                    | I <sub>OL</sub> = 100 μA   | -                     | 0.07            | 0.2  | V    |
|   |                                    | I <sub>OL</sub> = 24 mA  | -                     | 0.3             | 0.5  | V    |
|   |                                    | V <sub>CC</sub> = 3.0 V  |                       |                 |      |      |
|   |                                    | I <sub>OL</sub> = 16 mA  | -                     | 0.25            | 0.4  | V    |
|   |                                    | I <sub>OL</sub> = 32 mA  | -                     | 0.3             | 0.5  | V    |
| I <sub>I</sub>  | input leakage current              | control pins   |                       |                 |      |      |
|   |                                    | V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND   | -                     | 0.1             | ±1   | μA   |
|   |                                    | V <sub>CC</sub> = 0 V or 3.6 V; V <sub>I</sub> = 5.5 V   | -                     | 0.1             | 10   | μA   |
|   |                                    | input/output data pins; V <sub>CC</sub> = 3.6 V  | <sup>[2]</sup>        |                 |      |      |
|   |                                    | V <sub>I</sub> = 5.5 V   | -                     | 0.1             | 20   | μA   |
|   |                                    | V <sub>I</sub> = V <sub>CC</sub>   | -                     | 0.5             | 10   | μA   |
| I <sub>OFF</sub>  | power-off leakage current          | V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 0 V to 4.5 V   | -                     | 0.1             | ±100 | μA   |
|   |                                    | V <sub>CC</sub> = 3 V; V <sub>I</sub> = 0.8 V  | <sup>[3]</sup> 75     | 135             | -    | μA   |
| I <sub>BHL</sub>  | bus hold LOW current               | V <sub>CC</sub> = 3 V; V <sub>I</sub> = 0.8 V  | <sup>[3]</sup> 75     | 135             | -    | μA   |
| I <sub>BHH</sub>  | bus hold HIGH current              | V <sub>CC</sub> = 3 V; V <sub>I</sub> = 2.0 V  | -                     | -135            | -75  | μA   |
| I <sub>BHLO</sub>                                       | bus hold LOW overdrive current     | nAn input; V <sub>I</sub> = 0 V to 3.6 V; V <sub>CC</sub> = 3.6 V  | 500                   | -               | -    | μA   |
| I <sub>BHHO</sub>                                       | bus hold HIGH overdrive current    | nAn input; V <sub>I</sub> = 0 V to 3.6 V; V <sub>CC</sub> = 3.6 V  | -                     | -               | -500 | μA   |
| I <sub>LO</sub>   | output leakage current             | output in HIGH-state when V <sub>O</sub> > V <sub>CC</sub> ; V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 3.0 V   | -                     | 75              | 125  | μA   |
| I <sub>O(pu/pd)</sub>                                   | power-up/power-down output current | V <sub>CC</sub> ≤ 1.2 V; V <sub>O</sub> = 0.5 V to V <sub>CC</sub> ; V <sub>I</sub> = GND or V <sub>CC</sub> ; n $\overline{\text{OE}}$ = don't care | <sup>[4]</sup> -      | 40              | ±100 | μA   |
| I <sub>CC</sub>   | supply current                     | V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = GND or V <sub>CC</sub> ; I <sub>O</sub> = 0 A  |                       |                 |      |      |
|   |                                    | outputs HIGH   | -                     | 0.07            | 0.12 | mA   |
|   |                                    | outputs LOW  | -                     | 4.7             | 6.0  | mA   |
|   |                                    | outputs disabled   | <sup>[5]</sup> -      | 0.07            | 0.12 | mA   |
| ΔI <sub>CC</sub>  | additional supply current          | per input pin; V <sub>CC</sub> = 3.0 V to 3.6 V; one input at V <sub>CC</sub> - 0.6 V, other inputs at V <sub>CC</sub> or GND                        | <sup>[6]</sup> -      | 0.1             | 0.2  | mA   |
| C <sub>I</sub>  | input capacitance                  | pins nDIR and n $\overline{\text{OE}}$ , V <sub>O</sub> = 0 V or 3.0 V   | -                     | 3               | -    | pF   |

**Table 6. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol        | Parameter                          | Conditions   | Min | Typ | Max | Unit |
|---------------|------------------------------------|--|-----|-----|-----|------|
| $C_{iO(off)}$ | off-state input/output capacitance | pins nAn and nBn, outputs disabled;<br>$V_O = GND$ or $V_{CC}$ | -   | 9   | -   | pF   |

[1] Typical values are measured at  $V_{CC} = 3.3$  V and at  $T_{amb} = 25$  °C.[2] Unused pins at  $V_{CC}$  or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any  $V_{CC}$  between 0 V and 1.2 V with a transition time of up to 10 ms. From  $V_{CC} = 1.2$  V to  $V_{CC} = 3.3$  V  $\pm$  0.3 V a transition time of 100  $\mu$ s is permitted. This parameter is valid for  $T_{amb} = 25$  °C only.[5]  $I_{CC}$  is measured with outputs pulled to  $V_{CC}$  or GND.[6] This is the increase in supply current for each input at the specified voltage level other than  $V_{CC}$  or GND.

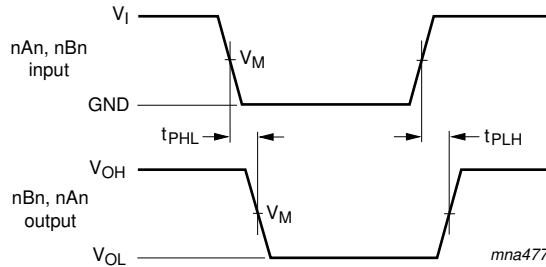
## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#).

| Symbol  | Parameter                           | Conditions   | Min | Typ <sup>[1]</sup> | Max | Unit |
|---|-------------------------------------|--|-----|--------------------|-----|------|
| <b><math>T_{amb} = -40</math> °C to <math>+85</math> °C</b> |                                     |  |     |                    |     |      |
| $t_{PLH}$   | LOW to HIGH propagation delay       | nAn to nBn or nBn to nAn;<br>see <a href="#">Figure 6</a>    |     |                    |     |      |
|   |                                     | $V_{CC} = 2.7$ V   | -   | -                  | 3.5 | ns   |
|   |                                     | $V_{CC} = 3.0$ V to 3.6 V                                    | 1.0 | 1.9                | 3.3 | ns   |
| $t_{PHL}$   | HIGH to LOW propagation delay       | nAn to nBn or nBn to nAn;<br>see <a href="#">Figure 6</a>    |     |                    |     |      |
|   |                                     | $V_{CC} = 2.7$ V   | -   | -                  | 3.5 | ns   |
|   |                                     | $V_{CC} = 3.0$ V to 3.6 V                                    | 1.0 | 1.7                | 3.3 | ns   |
| $t_{PZH}$   | OFF-state to HIGH propagation delay | $\overline{nOE}$ to nAn or nBn; see <a href="#">Figure 7</a> |     |                    |     |      |
|   |                                     | $V_{CC} = 2.7$ V   | -   | -                  | 5.3 | ns   |
|   |                                     | $V_{CC} = 3.0$ V to 3.6 V                                    | 1.0 | 2.8                | 4.5 | ns   |
| $t_{PZL}$   | OFF-state to LOW propagation delay  | $\overline{nOE}$ to nAn or nBn; see <a href="#">Figure 7</a> |     |                    |     |      |
|   |                                     | $V_{CC} = 2.7$ V   | -   | -                  | 5.1 | ns   |
|   |                                     | $V_{CC} = 3.0$ V to 3.6 V                                    | 1.0 | 2.8                | 4.1 | ns   |
| $t_{PHZ}$   | HIGH to OFF-state propagation delay | $\overline{nOE}$ to nAn or nBn; see <a href="#">Figure 7</a> |     |                    |     |      |
|   |                                     | $V_{CC} = 2.7$ V   | -   | -                  | 5.7 | ns   |
|   |                                     | $V_{CC} = 3.0$ V to 3.6 V                                    | 1.5 | 3.2                | 5.1 | ns   |
| $t_{PLZ}$   | LOW to OFF-state propagation delay  | $\overline{nOE}$ to nAn or nBn; see <a href="#">Figure 7</a> |     |                    |     |      |
|   |                                     | $V_{CC} = 2.7$ V   | -   | -                  | 4.6 | ns   |
|   |                                     | $V_{CC} = 3.0$ V to 3.6 V                                    | 1.5 | 3.0                | 4.6 | ns   |

[1] All typical values are at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C.

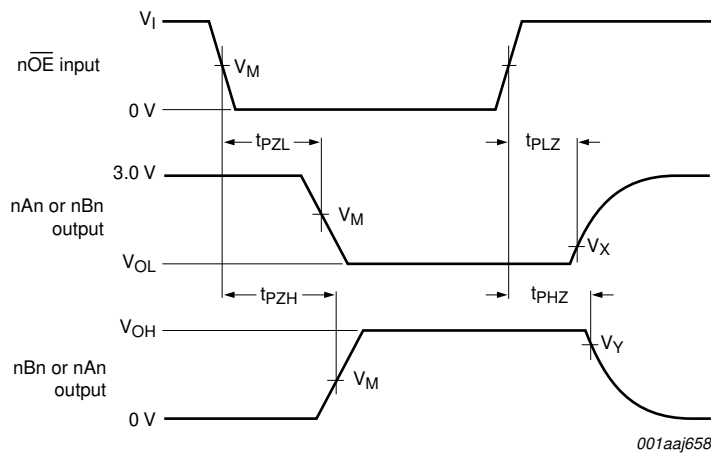
11. Waveforms



Measurements points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 6. Propagation delay input (nAn, nBn) to output (nBn, nAn)**



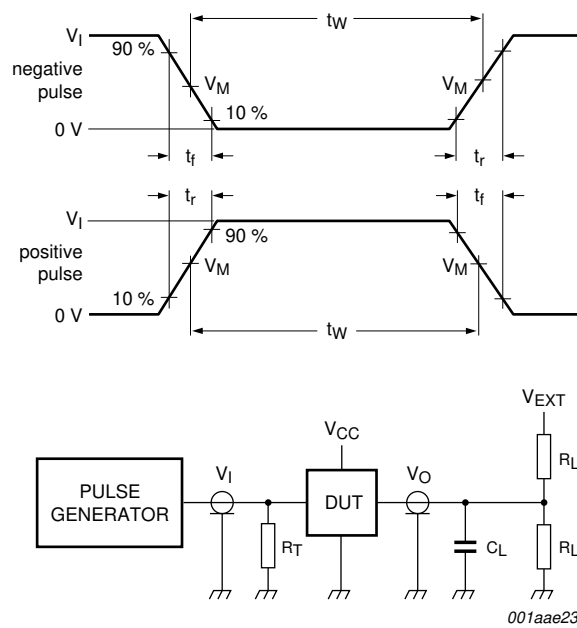
Measurements points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 7. 3-state output enable and disable times**

**Table 8. Measurement points**

| Input | Output |                  |                  |
|-------|--------|------------------|------------------|
| $V_M$ | $V_M$  | $V_X$            | $V_Y$            |
| 1.5 V | 1.5 V  | $V_{OL} + 0.3 V$ | $V_{OH} - 0.3 V$ |



Test data is given in [Table 9](#).

Definitions test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig 8. Test circuit for measuring switching times**

**Table 9. Test data**

| Input |               |        |               | Load  |              | $V_{EXT}$          |                    |                    |
|-------|---------------|--------|---------------|-------|--------------|--------------------|--------------------|--------------------|
| $V_I$ | $f_i$         | $t_W$  | $t_r, t_f$    | $C_L$ | $R_L$        | $t_{PHZ}, t_{PZH}$ | $t_{PLZ}, t_{PZL}$ | $t_{PLH}, t_{PHL}$ |
| 2.7 V | $\leq 10$ MHz | 500 ns | $\leq 2.5$ ns | 50 pF | 500 $\Omega$ | GND                | 6 V                | open               |

12. Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1

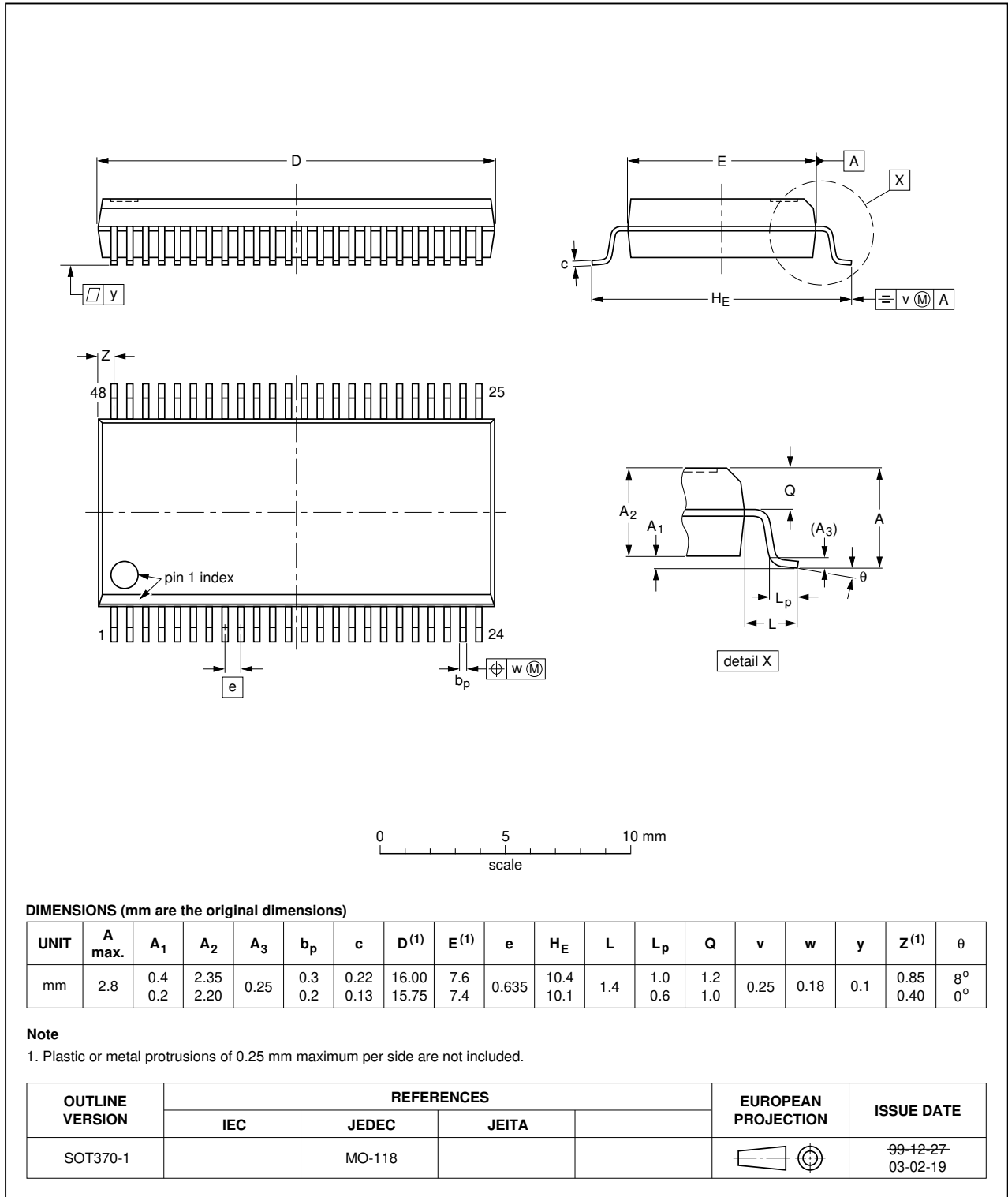


Fig 9. Package outline SOT370-1 (SSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

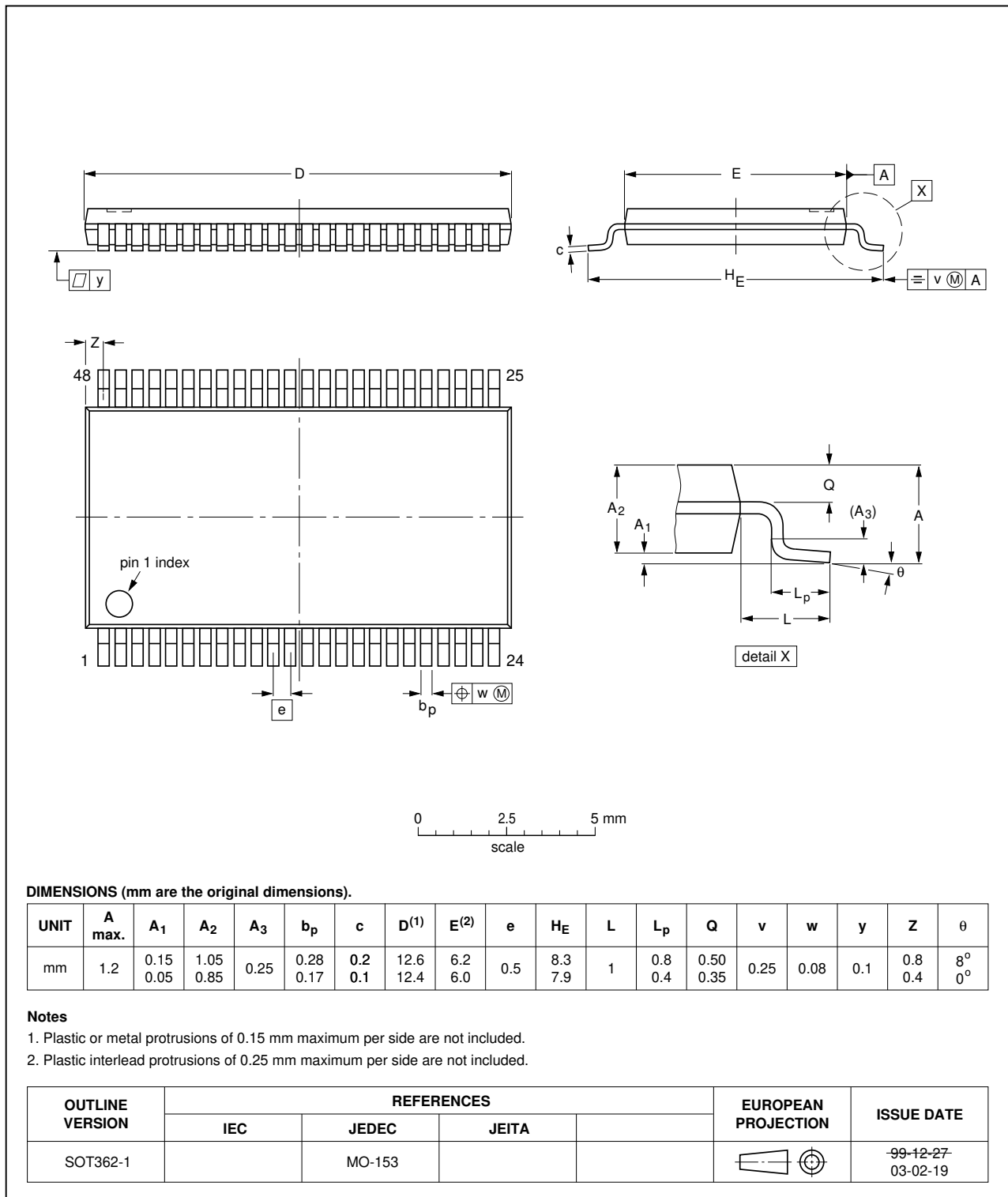


Fig 10. Package outline SOT362-1 (TSSOP48)

VFBGA56: plastic very thin fine-pitch ball grid array package; 56 balls; body 4.5 x 7 x 0.65 mm

SOT702-1

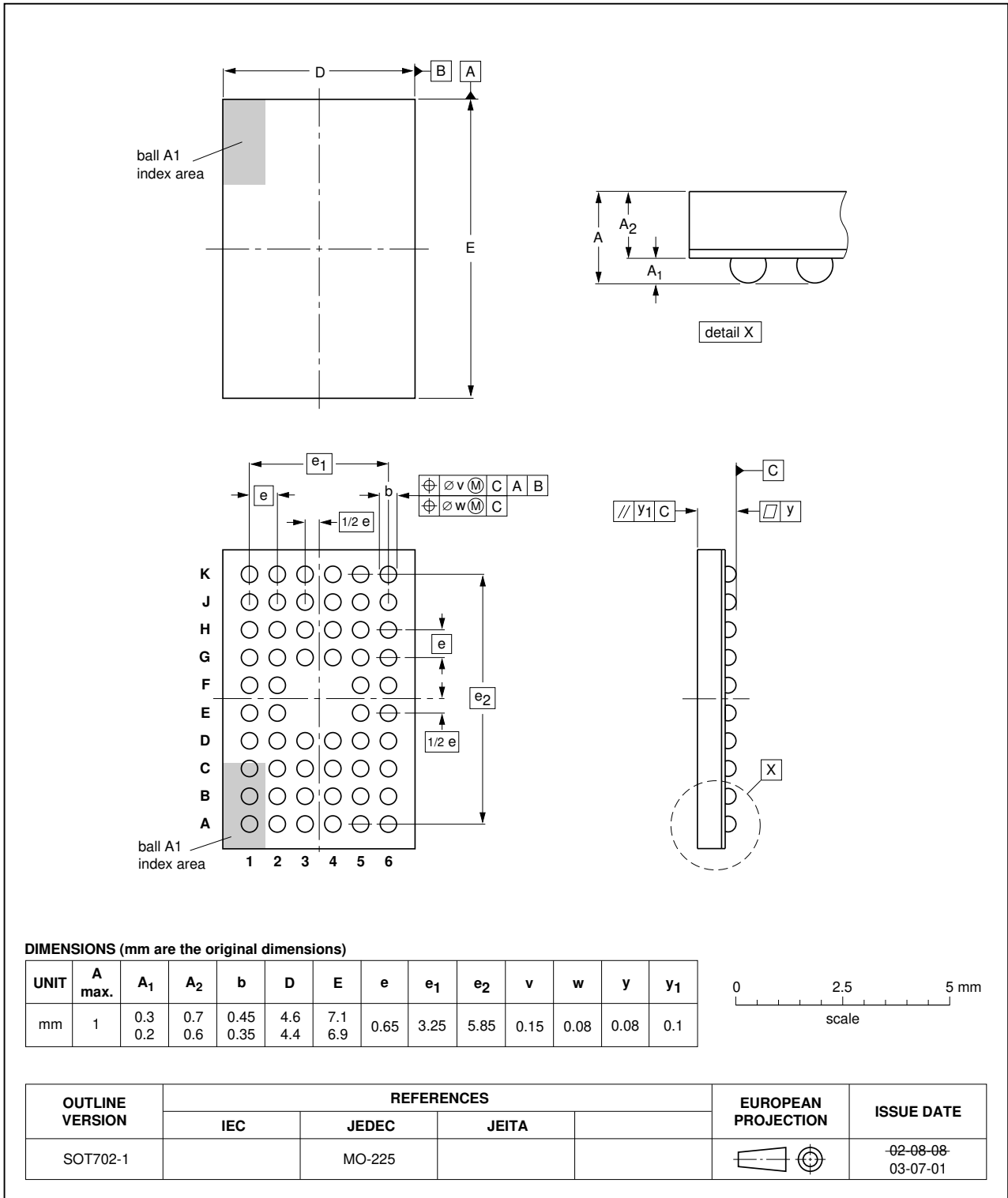
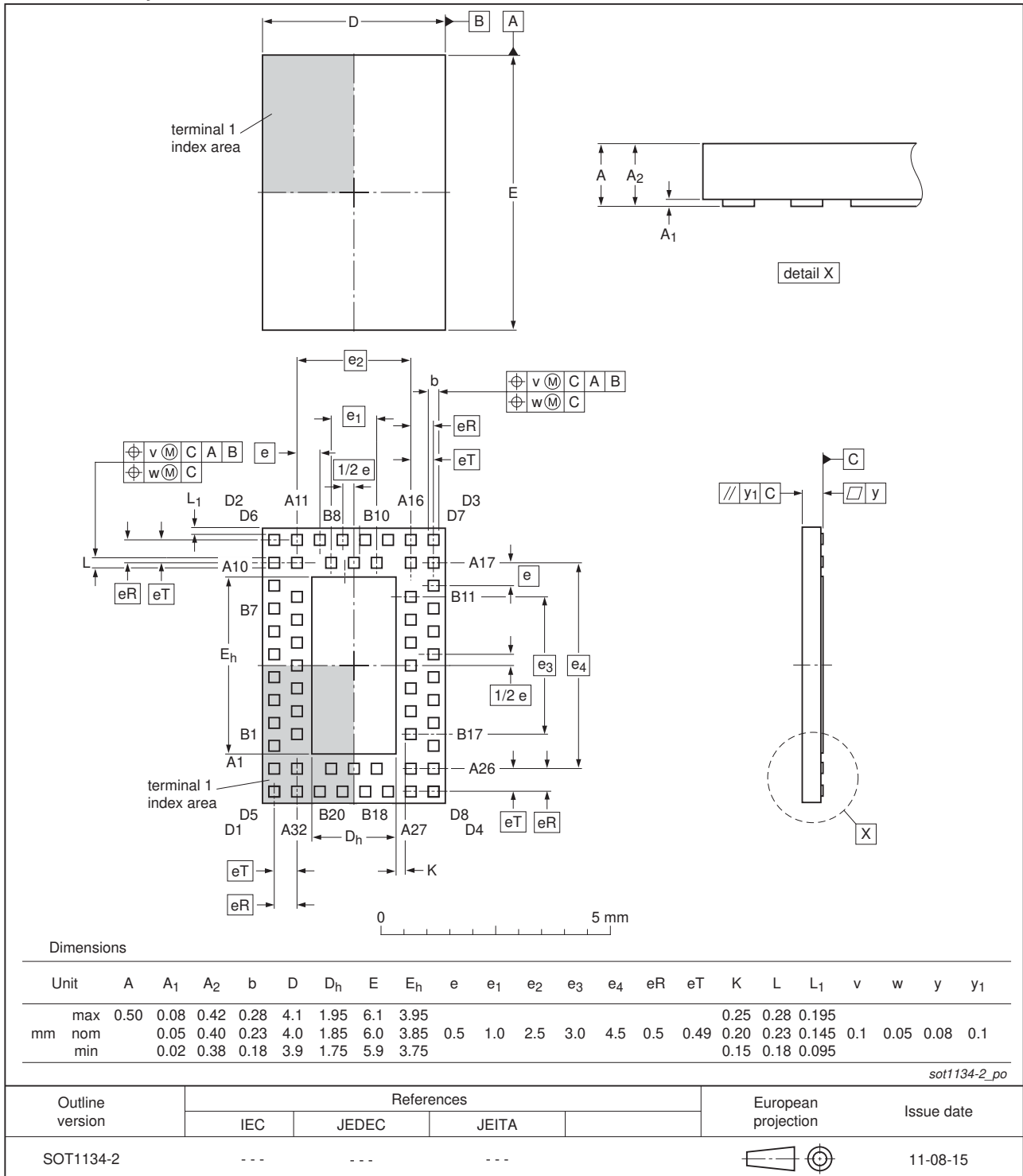


Fig 11. Package outline SOT702-1 (VFBGA56)



**HXQFN60: plastic compatible thermal enhanced extremely thin quad flat package; no leads; 60 terminals; body 4 x 6 x 0.5 mm**

SOT1134-2



**Fig 12. Package outline SOT1134-2 (HXQFN60)**

## 13. Abbreviations

Table 10. Abbreviations

| Acronym | Description                                     |
|---------|---|
| BICMOS  | Bipolar Complementary Metal Oxide Semiconductor |
| DUT     | Device Under Test                               |
| ESD     | ElectroStatic Discharge                         |
| HBM     | Human Body Model                                |
| MM      | Machine Model                                   |
| TTL     | Transistor-Transistor Logic                     |

## 14. Revision history

Table 11. Revision history

| Document ID           | Release date  | Data sheet status     | Change notice | Supersedes           |
|-----------------------|---|-----------------------|---------------|----------------------|
| 74LVT_LVTH16245B v.10 | 20120301  | Product data sheet    | -             | 74LVT_LVTH16245B v.9 |
| Modifications:        | <ul style="list-style-type: none"> <li>For type number 74LVT16245BBX and 74LVTH16245BBX the sot code has changed to SOT1134-2.</li> </ul> |                       |               |                      |
| 74LVT_LVTH16245B v.9  | 20111122  | Product data sheet    | -             | 74LVT_LVTH16245B v.8 |
| Modifications:        | <ul style="list-style-type: none"> <li>Legal pages updated.</li> </ul>  |                       |               |                      |
| 74LVT_LVTH16245B v.8  | 20110617  | Product data sheet    | -             | 74LVT_LVTH16245B v.7 |
| 74LVT_LVTH16245B v.7  | 20100329  | Product data sheet    | -             | 74LVT_LVTH16245B v.6 |
| 74LVT_LVTH16245B v.6  | 20090409  | Product data sheet    | -             | 74LVT_LVTH16245B v.5 |
| 74LVT_LVTH16245B v.5  | 20090312  | Product data sheet    | -             | 74LVT_LVTH16245B v.4 |
| 74LVT_LVTH16245B v.4  | 20060323  | Product data sheet    | -             | 74LVT16245B v.3      |
| 74LVT16245B v.3       | 20021031  | Product data sheet    | -             | 74LVT16245B v.2      |
| 74LVT16245B v.2       | 19980219  | Product specification | -             | 74LVT16245B v.1      |
| 74LVT16245B v.1       | 19940523  | Product specification | -             | -                    |

## 15. Legal information

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| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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