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FAIRCHILD SEMICONDUCTOR™

January 2000
Revised October 2001

74LVT16543 • 74LVTH16543 Low Voltage 16-Bit Registered Transceiver with 3-STATE Outputs

General Description

The LVT16543 and LVTH16543 16-bit transceivers contain two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. Each byte has separate control inputs, which can be shorted together for full 16-bit operation.

The LVTH16543 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These transceivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16543 and LVTH16543 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining low power dissipation.

Features

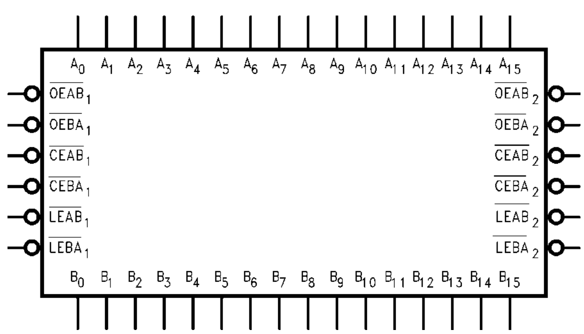
- Input and output interface capability to systems at 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH16543)
- Also available without bushold feature (74LVT16543)
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Functionally compatible with the 74 series 16543
- Latch-up conforms to JEDEC JED78
- ESD performance:
  Human-body model > 2000V
  Machine model > 200V
  Charged-device model > 1000V

Ordering Code:

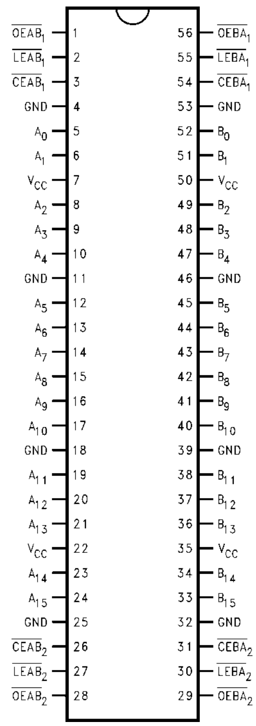
Order Number	Package Number	Package Description
74LVT16543MEA (Preliminary)	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LVT16543MTD (Preliminary)	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
74LVTH16543MEA	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LVTH16543MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{OEAB}_n$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}_n$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}_n$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}_n$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}_n$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}_n$	B-to-A Latch Enable Input (Active LOW)
A_0–A_{15}	A-to-B Data Inputs or
	B-to-A 3-STATE Outputs
B_0–B_{15}	B-to-A Data Inputs or
	A-to-B 3-STATE Outputs

Functional Description

The LVT16543 and LVTH16543 contain two sets of D-type latches, with separate input and output controls for each. For data flow from A to B, for example, the A to B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from the A Port or take data from the B Port as indicated in the Data I/O Control Table. With $\overline{CEAB}$ LOW, a low signal on ($\overline{LEAB}$) input makes the A to B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ line puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the B output buffers are active and reflect the data present on the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$. Each byte has separate control inputs, allowing the device to be used as two 8-bit transceivers or as one 16-bit transceiver.

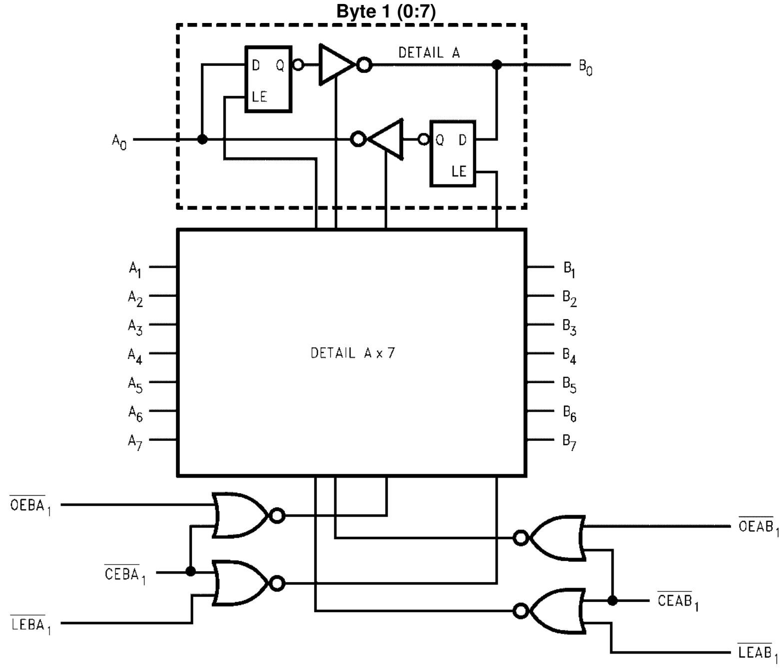
Data I/O Control Table

Inputs			Latch Status (Byte n)	Output Buffers (Byte n)
$\overline{CEAB}_n$	$\overline{LEAB}_n$	$\overline{OEAB}_n$		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}_n$, $\overline{LEBA}_n$ and $\overline{OEBA}_n$

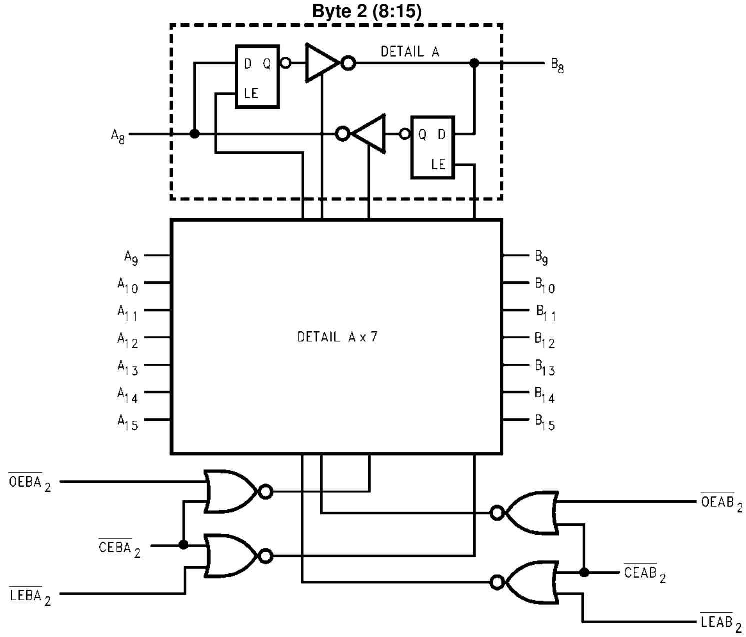
Logic Diagrams

Byte 1 (0:7)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Byte 2 (8:15)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +4.6		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in 3-STATE	V
		−0.5 to +7.0	Output in HIGH or LOW State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
I_O	DC Output Current	64	$V_O > V_{CC}$ Output at HIGH State	mA
		128	$V_O > V_{CC}$ Output at LOW State	
I_{CC}	DC Supply Current per Supply Pin	±64		mA
I_{GND}	DC Ground Current per Ground Pin	±128		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	3.6	V
V_I	Input Voltage	0	5.5	V
I_{OH}	HIGH-Level Output Current		−32	mA
I_{OL}	LOW-Level Output Current		64	
T_A	Free-Air Operating Temperature	−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V	0	10	ns/V

Note 1: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 2: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics

Symbol	Parameter		V_{CC} (V)	$T_A = -40°C$ to $+85°C$ Min	Max	Units	Conditions
V_{IK}	Input Clamp Diode Voltage		2.7		−1.2	V	$I_I = -18$ mA
V_{IH}	Input HIGH Voltage		2.7–3.6	2.0		V	$V_O \leq 0.1V$ or
V_{IL}	Input LOW Voltage		2.7–3.6		0.8		$V_O \geq V_{CC} - 0.1V$
V_{OH}	Output HIGH Voltage		2.7–3.6	$V_{CC} - 0.2$		V	$I_{OH} = -100$ µA
			2.7	2.4		V	$I_{OH} = -8$ mA
			3.0	2.0		V	$I_{OH} = -32$ mA
V_{OL}	Output LOW Voltage		2.7		0.2	V	$I_{OL} = 100$ µA
			2.7		0.5	V	$I_{OL} = 24$ mA
			3.0		0.4	V	$I_{OL} = 16$ mA
			3.0		0.5	V	$I_{OL} = 32$ mA
			3.0		0.55	V	$I_{OL} = 64$ mA
$I_{I(HOLD)}$ (Note 3)	Bushold Input Minimum Drive		3.0	75		µA	$V_I = 0.8V$
				−75		µA	$V_I = 2.0V$
$I_{I(OD)}$ (Note 3)	Bushold Input Over-Drive Current to Change State		3.0	500		µA	(Note 4)
				−500		µA	(Note 5)
I_I	Input Current		3.6		10	µA	$V_I = 5.5V$
		Control Pins	3.6		±1	µA	$V_I = 0V$ or V_{CC}
		Data Pins	3.6		−5	µA	$V_I = 0V$
					1	µA	$V_I = V_{CC}$
I_{OFF}	Power Off Leakage Current		0		±100	µA	$0V \leq V_I$ or $V_O \leq 5.5V$
$I_{PU/PD}$	Power Up/Down 3-STATE Output Current		0–1.5V		±100	µA	$V_O = 0.5V$ to $3.0V$ $V_I =$ GND or V_{CC}
I_{OZL} (Note 3)	3-STATE Output Leakage Current		3.6		−5	µA	$V_O = 0.0V$
I_{OZL}	3-STATE Output Leakage Current		3.6		−5	µA	$V_O = 0.5V$
I_{OZH} (Note 3)	3-STATE Output Leakage Current		3.6		5	µA	$V_O = 3.6V$
I_{OZH}	3-STATE Output Leakage Current		3.6		5	µA	$V_O = 3.0V$
$I_{OZH}+$	3-STATE Output Leakage Current		3.6		10	µA	$V_{CC} < V_O \leq 5.5V$
I_{CCH}	Power Supply Current		3.6		0.19	mA	Outputs HIGH
I_{CCL}	Power Supply Current		3.6		5	mA	Outputs LOW
I_{CCZ}	Power Supply Current		3.6		0.19	mA	Outputs Disabled
$I_{CCZ}+$	Power Supply Current		3.6		0.19	mA	$V_{CC} \leq V_O \leq 5.5V$, Outputs Disabled
ΔI_{CC}	Increase in Power Supply Current (Note 6)		3.6		0.2	mA	One Input at $V_{CC} - 0.6V$ Other Inputs at V_{CC} or GND

Note 3: Applies to bushold versions only (74LVTH16543)

Note 4: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 5: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 6: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 7)

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$ Min	Typ	Max	Units	Conditions $C_L = 50$ pF, $R_L = 500\Omega$
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8		V	(Note 8)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		−0.8		V	(Note 8)

Note 7: Characterized in SSOP package. Guaranteed parameter, but not tested.

Note 8: Max number of outputs defined as (n). n−1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

Symbol	Parameter		$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $R_L = 500\ \Omega$: $V_{CC} = 3.3 \pm 0.3V$ Min	$V_{CC} = 3.3 \pm 0.3V$ Max	$V_{CC} = 2.7V$ Min	$V_{CC} = 2.7V$ Max	Units
t_{PLH}	Propagation Delay		1.2	4.2	1.2	4.5	ns
t_{PHL}	Data to Outputs		1.2	4.4	1.2	4.9	
t_{PLH}	Propagation Delay		1.3	4.7	1.3	5.5	ns
t_{PHL}	$\overline{LE}$ to A or B		1.3	5.1	1.3	5.8	
t_{PZH}	Output Enable Time		1.3	4.7	1.3	5.4	ns
t_{PZL}	$\overline{OE}$ to A or B		1.3	5.1	1.3	6.1	
t_{PHZ}	Output Disable Time		2.0	5.5	2.0	5.7	ns
t_{PLZ}	$\overline{OE}$ to A or B		2.0	4.9	2.0	4.9	
t_{PZH}	Output Enable Time		1.3	4.6	1.3	5.6	ns
t_{PZL}	$\overline{CE}$ to A or B		1.3	5.0	1.3	6.1	
t_{PHZ}	Output Disable Time		2.0	5.5	2.0	5.8	ns
t_{PLZ}	$\overline{CE}$ to A or B		2.0	4.9	2.0	4.9	
t_W	Pulse Duration	$\overline{LE}$ LOW	3.3		3.3		ns
t_S	Setup Time	A or B before $\overline{LE}$, Data HIGH	0.5		0.5		ns
		A or B before $\overline{LE}$, Data LOW	0.8		1.3		
		A or B before $\overline{CE}$, Data HIGH	0.5		0.0		
		A or B before $\overline{CE}$, Data LOW	0.6		1.1		
t_H	Hold Time	A or B after $\overline{LE}$, Data HIGH	1.5		0.7		ns
		A or B after $\overline{LE}$, Data LOW	1.2		1.3		
		A or B after $\overline{CE}$, Data HIGH	1.7		0.9		
		A or B after $\overline{CE}$, Data LOW	1.6		1.8		
t_{OSLH}	Output to Output Skew (Note 9)			1.0		1.0	ns
t_{OSHL}				1.0		1.0	

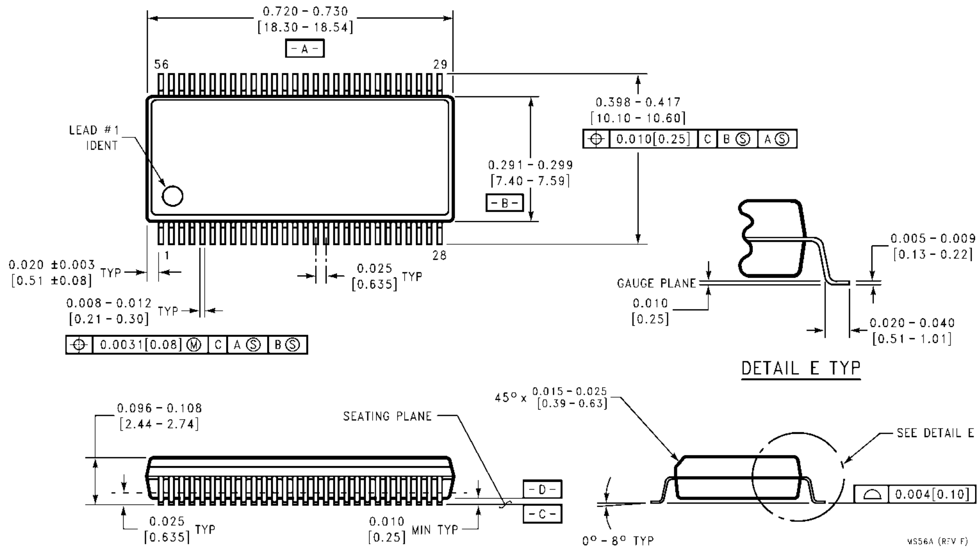
Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Capacitance (Note 10)

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = OPEN, V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	Input/Output Capacitance	V_{CC} = 3.0V, V_O = 0V or V_{CC}	8	pF

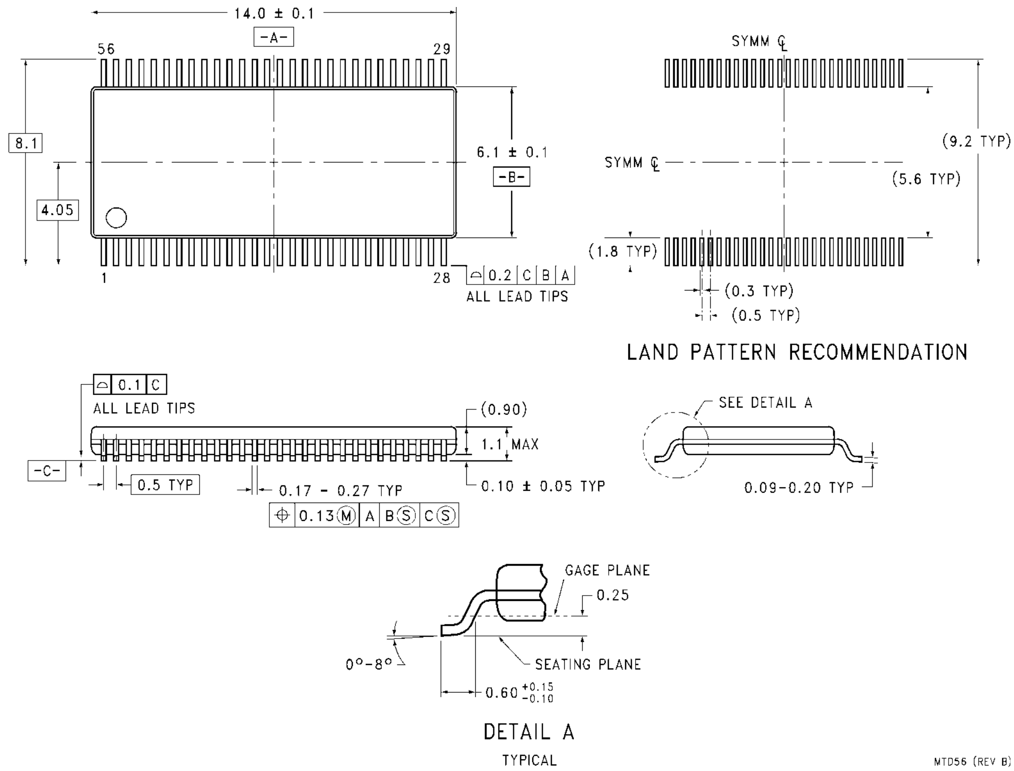
Note 10: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS56A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56