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SEMICONDUCTOR™

March 1998
Revised October 2004

# 74VCX16601

# Low Voltage 18-Bit Universal Bus Transceivers with 3.6V Tolerant Inputs and Outputs

## General Description

The VCX16601 is an 18-bit universal bus transceiver which combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH-to-LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CLKAB. When $\overline{OEAB}$ is LOW, the outputs are active. When $\overline{OEAB}$ is HIGH, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA and $\overline{CLKENBA}$.

The VCX16601 is designed for low voltage (1.4V to 3.6V) $V_{CC}$ applications with I/O capability up to 3.6V.

The VCX16601 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

## Features

- 1.4V to 3.6V $V_{CC}$ supply operation
- 3.6V tolerant inputs and outputs
- $t_{PD}$ (A to B, B to A)

  2.9 ns max for 3.0V to 3.6V $V_{CC}$
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- Static Drive ($I_{OH}/I_{OL}$)

  ±24 mA @ 3.0V $V_{CC}$
- Uses patented noise/EMI reduction circuitry
- Latchup performance exceeds 300 mA
- ESD performance:

  Human body model > 2000V

  Machine model >200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

**Note 1:** To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

## Ordering Code:

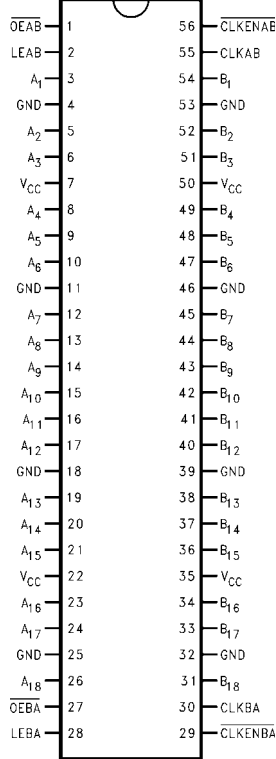| Order Number | Package Number | Package Description |
|---|---|---|
| 74VCX16601GX (Note 2) | BGA54A (Preliminary) | 54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL] |
| 74VCX16601MTD (Note 3) | MTD56 | 56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide |

**Note 2:** BGA package available in Tape and Reel only.

**Note 3:** Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
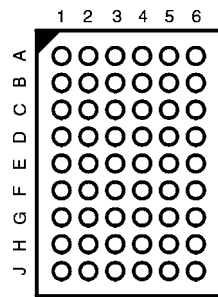
74VCX16601

## Connection Diagrams

### Pin Assignment for TSSOP

| | | | | |
|---|---|---|---|---|
| $\overline{OEAB}$ | 1 | | 56 | $\overline{CLKENAB}$ |
| LEAB | 2 | | 55 | CLKAB |
| $A_1$ | 3 | | 54 | $B_1$ |
| GND | 4 | | 53 | GND |
| $A_2$ | 5 | | 52 | $B_2$ |
| $A_3$ | 6 | | 51 | $B_3$ |
| $V_{CC}$ | 7 | | 50 | $V_{CC}$ |
| $A_4$ | 8 | | 49 | $B_4$ |
| $A_5$ | 9 | | 48 | $B_5$ |
| $A_6$ | 10 | | 47 | $B_6$ |
| GND | 11 | | 46 | GND |
| $A_7$ | 12 | | 45 | $B_7$ |
| $A_8$ | 13 | | 44 | $B_8$ |
| $A_9$ | 14 | | 43 | $B_9$ |
| $A_{10}$ | 15 | | 42 | $B_{10}$ |
| $A_{11}$ | 16 | | 41 | $B_{11}$ |
| $A_{12}$ | 17 | | 40 | $B_{12}$ |
| GND | 18 | | 39 | GND |
| $A_{13}$ | 19 | | 38 | $B_{13}$ |
| $A_{14}$ | 20 | | 37 | $B_{14}$ |
| $A_{15}$ | 21 | | 36 | $B_{15}$ |
| $V_{CC}$ | 22 | | 35 | $V_{CC}$ |
| $A_{16}$ | 23 | | 34 | $B_{16}$ |
| $A_{17}$ | 24 | | 33 | $B_{17}$ |
| GND | 25 | | 32 | GND |
| $A_{18}$ | 26 | | 31 | $B_{18}$ |
| $\overline{OEBA}$ | 27 | | 30 | CLKBA |
| LEBA | 28 | | 29 | $\overline{CLKENBA}$ |

### Pin Assignment for FBGA

**(Top Thru View)**

## Pin Descriptions

| Pin Names | Description |
|---|---|
| $\overline{OEAB}$, $\overline{OEBA}$ | Output Enable Inputs (Active LOW) |
| LEAB, LEBA | Latch Enable Inputs |
| CLKAB, CLKBA | Clock Inputs |
| $\overline{CLKENAB}$, $\overline{CLKENBA}$ | Clock Enable Inputs |
| $A_1$–$A_{18}$ | Side A Inputs or 3-STATE Outputs |
| $B_1$–$B_{18}$ | Side B Inputs or 3-STATE Outputs |

## FBGA Pin Assignments

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| **A** | $A_2$ | $A_1$ | $\overline{OEAB}$ | $\overline{CLKENAB}$ | $B_1$ | $B_2$ |
| **B** | $A_4$ | $A_3$ | LEAB | CLKAB | $B_3$ | $B_4$ |
| **C** | $A_6$ | $A_5$ | $V_{CC}$ | $V_{CC}$ | $B_5$ | $B_6$ |
| **D** | $A_8$ | $A_7$ | GND | GND | $B_7$ | $B_8$ |
| **E** | $A_{10}$ | $A_9$ | GND | GND | $B_9$ | $B_{10}$ |
| **F** | $A_{12}$ | $A_{11}$ | GND | GND | $B_{11}$ | $B_{12}$ |
| **G** | $A_{14}$ | $A_{13}$ | $V_{CC}$ | $V_{CC}$ | $B_{13}$ | $B_{14}$ |
| **H** | $A_{16}$ | $A_{15}$ | $\overline{OEBA}$ | CLKBA | $B_{15}$ | $B_{16}$ |
| **J** | $A_{17}$ | $A_{18}$ | LEBA | $\overline{CLKENBA}$ | $B_{18}$ | $B_{17}$ |

## Truth Table

(Note 4)

| Inputs | | | | | Outputs |
|---|---|---|---|---|---|
| $\overline{CLKENAB}$ | $\overline{OEAB}$ | LEAB | CLKAB | $A_n$ | $B_n$ |
| X | H | X | X | X | Z |
| X | L | H | X | L | L |
| X | L | H | X | H | H |
| H | L | L | X | X | $B_0$ (Note 5) |
| H | L | L | X | X | $B_0$ (Note 5) |
| L | L | L | ↑ | L | L |
| L | L | L | ↑ | H | H |
| L | L | L | L | X | $B_0$ (Note 5) |
| L | L | L | H | X | $B_0$ (Note 6) |

H = HIGH Voltage Level
L = LOW Voltage Level
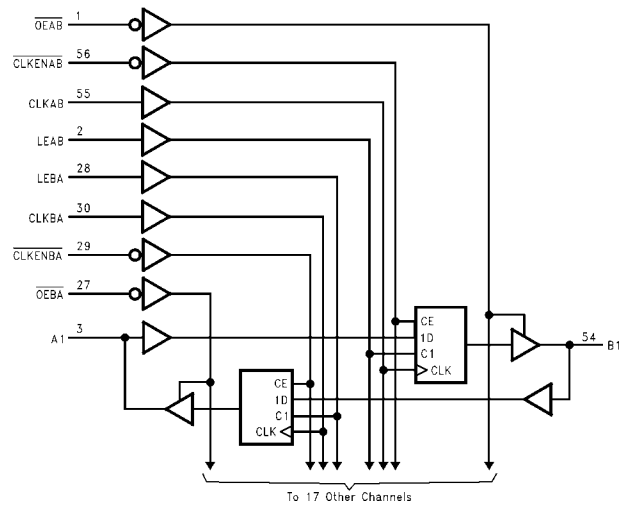X = Immaterial (HIGH or LOW, inputs may not float)
Z = High Impedance

**Note 4:** A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CLKENBA}$.

**Note 5:** Output level before the indicated steady-state input conditions were established.

**Note 6:** Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.

## Logic Diagram

| Signal | Pin |
|--------|-----|
| $\overline{OEAB}$ | 1 |
| $\overline{CLKENAB}$ | 56 |
| CLKAB | 55 |
| LEAB | 2 |
| LEBA | 28 |
| CLKBA | 30 |
| $\overline{CLKENBA}$ | 29 |
| $\overline{OEBA}$ | 27 |
| A1 | 3 |

CE
1D
C1
CLK

CE
1D
C1
CLK

54 B1

To 17 Other Channels

## Absolute Maximum Ratings(Note 7)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to +4.6V |
| DC Input Voltage ($V_I$) | −0.5V to +4.6V |
| Output Voltage ($V_O$) | |
|   Outputs 3-Stated | −0.5V to +4.6V |
|   Outputs Active (Note 8) | −0.5 to $V_{CC}$ + 0.5V |
| DC Input Diode Current ($I_{IK}$) $V_I$ < 0V | −50 mA |
| DC Output Diode Current ($I_{OK}$) | |
|   $V_O$ < 0V | −50 mA |
|   $V_O$ > $V_{CC}$ | +50 mA |
| DC Output Source/Sink Current | |
|   ($I_{OH}/I_{OL}$) | ±50 mA |
| DC $V_{CC}$ or Ground Current per | |
|   Supply Pin ($I_{CC}$ or Ground) | ±100 mA |
| Storage Temperature Range ($T_{STG}$) | −65°C to +150°C |

## Recommended Operating Conditions (Note 9)

| | |
|---|---|
| Power Supply | |
|   Operating | 1.4V to 3.6V |
| Input Voltage | −0.3V to 3.6V |
| Output Voltage ($V_O$) | |
|   Output in Active States | 0V to $V_{CC}$ |
|   Output in 3-STATE | 0.0V to 3.6V |
| Output Current in $I_{OH}/I_{OL}$ | |
|   $V_{CC}$ = 3.0V to 3.6V | ±24 mA |
|   $V_{CC}$ = 2.3V to 2.7V | ±18 mA |
|   $V_{CC}$ = 1.65V to 2.3V | ±6 mA |
|   $V_{CC}$ = 1.4V to 1.6V | ±2 mA |
| Free Air Operating Temperature ($T_A$) | −40°C to +85°C |
| Minimum Input Edge Rate ($\Delta t/\Delta V$) | |
|   $V_{IN}$ = 0.8V to 2.0V, $V_{CC}$ = 3.0V | 10 ns/V |

**Note 7:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The Recommended Operating Conditions tables will define the conditions for actual device operation.

**Note 8:** $I_O$ Absolute Maximum Rating must be observed.

**Note 9:** Floating or unused pin (inputs or I/O's) must be held HIGH or LOW.

## DC Electrical Characteristics

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | Min | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | HIGH Level Input Voltage | | 2.7 - 3.6 | 2.0 | | V |
| | | | 2.3 - 2.7 | 1.6 | | |
| | | | 1.65 - 2.3 | 0.65 x $V_{CC}$ | | |
| | | | 1.4 - 1.6 | 0.65 x $V_{CC}$ | | |
| $V_{IL}$ | LOW Level Input Voltage | | 2.7 - 3.6 | | 0.8 | V |
| | | | 2.3 - 2.7 | | 0.7 | |
| | | | 1.65 - 2.3 | | 0.35 - $V_{CC}$ | |
| | | | 1.4 - 1.6 | | 0.35 - $V_{CC}$ | |
| $V_{OH}$ | HIGH Level Output Voltage | $I_{OH}$ = −100 µA | 2.7 - 3.6 | $V_{CC}$ - 0.2 | | V |
| | | $I_{OH}$ = −12 mA | 2.7 | 2.2 | | |
| | | $I_{OH}$ = −18 mA | 3.0 | 2.4 | | |
| | | $I_{OH}$ = −24 mA | 3.0 | 2.2 | | |
| | | $I_{OH}$ = −100 µA | 2.3 - 2.7 | $V_{CC}$ - 0.2 | | |
| | | $I_{OH}$ = −6 mA | 2.3 | 2.0 | | |
| | | $I_{OH}$ = −12 mA | 2.3 | 1.8 | | |
| | | $I_{OH}$ = −18 mA | 2.3 | 1.7 | | |
| | | $I_{OH}$ = −100 µA | 1.65 - 2.3 | $V_{CC}$ - 0.2 | | |
| | | $I_{OH}$ = −6 mA | 1.65 | 1.25 | | |
| | | $I_{OH}$ = −100 µA | 1.4 - 1.6 | $V_{CC}$ - 0.2 | | |
| | | $I_{OH}$ = −2 mA | 1.4 | 1.05 | | |

## DC Electrical Characteristics (Continued)

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | Min | Max | Units |
|---|---|---|---|---|---|---|
| $V_{OL}$ | LOW Level Output Voltage | $I_{OL}$ = 100 μA | 2.7 - 3.6 | | 0.2 | |
| | | $I_{OL}$ = 12 mA | 2.7 | | 0.4 | |
| | | $I_{OL}$ = 18 mA | 3.0 | | 0.4 | |
| | | $I_{OL}$ = 24 mA | 3.0 | | 0.55 | |
| | | $I_{OL}$ = 100 μA | 2.3 - 2.7 | | 0.2 | |
| | | $I_{OL}$ = 12 mA | 2.3 | | 0.4 | V |
| | | $I_{OL}$ = 18 mA | 2.3 | | 0.6 | |
| | | $I_{OL}$ = 100 μA | 1.65 - 2.3 | | 0.2 | |
| | | $I_{OL}$ = 6 mA | 1.65 | | 0.3 | |
| | | $I_{OL}$ = 100 μA | 1.4 - 1.6 | | 0.2 | |
| | | $I_{OL}$ = 2 mA | 1.4 | | 0.35 | |
| $I_I$ | Input Leakage Current | $0V \le V_I \le 3.6V$ | 2.7 - 3.6 | | ±5.0 | μA |
| $I_{OZ}$ | 3-STATE Output Leakage | $0V \le V_O \le 3.6V$ $V_I = V_{IH}$ or $V_{IL}$ | 1.4 - 3.6 | | ±10.0 | μA |
| $I_{OFF}$ | Power Off Leakage Current | $0V \le (V_I, V_O) \le 3.6V$ | 0 | | 10.0 | μA |
| $I_{CC}$ | Quiescent Supply Current | $V_I = V_{CC}$ or GND | 1.4 - 3.6 | | 20.0 | μA |
| | | $V_{CC} \le (V_I, V_O) \le 3.6V$ (Note 10) | 1.4 - 3.6 | | ±20.0 | |
| $\Delta I_{CC}$ | Increase in $I_{CC}$ per Input | $V_{IH} = V_{CC} - 0.6V$ | 2.7 - 3.6 | | 750 | μA |

**Note 10:** Outputs disabled or 3-STATE only.

## AC Electrical Characteristics (Note 11)

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A = -40°C$ to $+85°C$ Min | Max | Units | Figure Number |
|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Clock Frequency | $C_L = 30$ pF | $3.3 \pm 0.3$ | 250 | | MHz | |
| | | | $2.5 \pm 0.2$ | 200 | | | |
| | | | $1.8 \pm 0.15$ | 100 | | | |
| | | $C_L = 15$ pF | $1.5 \pm 0.1$ | 80.0 | | | |
| $t_{PHL}$ $t_{PLH}$ | Propagation Delay Bus-to-Bus | $C_L = 30$ pF, $R_L = 500\Omega$ | $3.3 \pm 0.3$ | 0.8 | 2.9 | | Figures 1, 2 |
| | | | $2.5 \pm 0.2$ | 1.0 | 3.5 | ns | |
| | | | $1.8 \pm 0.15$ | 1.5 | 7.0 | | |
| | | $C_L = 15$ pF, $R_L = 2k\Omega$ | $1.5 \pm 0.1$ | 1.0 | 14.0 | | Figures 7, 8 |
| $t_{PHL}$ $t_{PLH}$ | Propagation Delay Clock-to-Bus | $C_L = 30$ pF, $R_L = 500\Omega$ | $3.3 \pm 0.3$ | 0.8 | 3.5 | | Figures 1, 2 |
| | | | $2.5 \pm 0.2$ | 1.0 | 4.4 | ns | |
| | | | $1.8 \pm 0.15$ | 1.5 | 8.8 | | |
| | | $C_L = 15$ pF, $R_L = 500\Omega$ | $1.5 \pm 0.1$ | 1.0 | 17.6 | | Figures 7, 8 |
| $t_{PHL}$ $t_{PLH}$ | Propagation Delay LE-to-Bus | $C_L = 30$ pF, $R_L = 500\Omega$ | $3.3 \pm 0.3$ | 0.8 | 3.5 | | Figures 1, 2 |
| | | | $2.5 \pm 0.2$ | 1.0 | 4.4 | ns | |
| | | | $1.8 \pm 0.15$ | 1.5 | 8.8 | | |
| | | $C_L = 15$ pF, $R_L = 500\Omega$ | $1.5 \pm 0.1$ | 1.0 | 17.6 | | Figures 7, 8 |
| $t_{PZL}$ $t_{PZH}$ | Output Enable Time | $C_L = 30$ pF, $R_L = 500\Omega$ | $3.3 \pm 0.3$ | 0.8 | 3.8 | | Figures 1, 3, 4 |
| | | | $2.5 \pm 0.2$ | 1.0 | 4.9 | ns | |
| | | | $1.8 \pm 0.15$ | 1.5 | 9.8 | | |
| | | $C_L = 15$ pF, $R_L = 2k\Omega$ | $1.5 \pm 0.1$ | 1.0 | 19.6 | | Figures 7, 9, 10 |
| $t_{PLZ}$ $t_{PHZ}$ | Output Disable Time | $C_L = 30$ pF, $R_L = 500\Omega$ | $3.3 \pm 0.3$ | 0.8 | 3.7 | | Figures 1, 3, 4 |
| | | | $2.5 \pm 0.2$ | 1.0 | 4.2 | ns | |
| | | | $1.8 \pm 0.15$ | 1.5 | 7.6 | | |
| | | $C_L = 15$ pF, $R_L = 2k\Omega$ | $1.5 \pm 0.1$ | 1.0 | 15.2 | | Figures 7, 9, 10 |
| $t_S$ | Setup Time | $C_L = 30$ pF, $R_L = 500\Omega$ | $3.3 \pm 0.3$ | 1.5 | | | Figure 6 |
| | | | $2.5 \pm 0.2$ | 1.5 | | ns | |
| | | | $1.8 \pm 0.15$ | 2.5 | | | |
| | | $C_L = 15$ pF, $R_L = 500\Omega$ | $1.5 \pm 0.1$ | 3.0 | | | |
| $t_H$ | Hold Time | $C_L = 30$ pF, $R_L = 500\Omega$ | $3.3 \pm 0.3$ | 1.0 | | | Figure 6 |
| | | | $2.5 \pm 0.2$ | 1.0 | | ns | |
| | | | $1.8 \pm 0.15$ | 1.0 | | | |
| | | $C_L = 15$ pF, $R_L = 500\Omega$ | $1.5 \pm 0.1$ | 2.0 | | | |
| $t_W$ | Pulse Width | $C_L = 30$ pF, $R_L = 500\Omega$ | $3.3 \pm 0.3$ | 1.5 | | | Figure 5 |
| | | | $2.5 \pm 0.2$ | 1.5 | | ns | |
| | | | $1.8 \pm 0.15$ | 4.0 | | | |
| | | $C_L = 15$ pF, $R_L = 500\Omega$ | $1.5 \pm 0.1$ | 4.0 | | | |
| $t_{OSHL}$ $t_{OSLH}$ | Output to Output Skew (Note 12) | $C_L = 30$ pF, $R_L = 500\Omega$ | $3.3 \pm 0.3$ | | 0.5 | | |
| | | | $2.5 \pm 0.2$ | | 0.5 | ns | |
| | | | $1.8 \pm 0.15$ | | 0.75 | | |
| | | $C_L = 15$ pF, $R_L = 2k\Omega$ | $1.5 \pm 0.1$ | | 1.5 | | |

**Note 11:** For $C_L = 50$pF, add approximately 300ps to the AC maximum specification.

**Note 12:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ($t_{OSHL}$) or LOW-to-HIGH ($t_{OSLH}$).

## Dynamic Switching Characteristics

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A = +25°C$ Typical | Units |
|--------|-----------|------------|--------------|------------------------|-------|
| $V_{OLP}$ | Quiet Output Dynamic Peak $V_{OL}$ | $C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$ | 1.8 | 0.25 | |
| | | | 2.5 | 0.6 | V |
| | | | 3.3 | 0.8 | |
| $V_{OLV}$ | Quiet Output Dynamic Valley $V_{OL}$ | $C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$ | 1.8 | −0.25 | |
| | | | 2.5 | −0.6 | V |
| | | | 3.3 | −0.8 | |
| $V_{OHV}$ | Quiet Output Dynamic Valley $V_{OH}$ | $C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$ | 1.8 | 1.5 | |
| | | | 2.5 | 1.9 | V |
| | | | 3.3 | 2.2 | |

## Capacitance

| Symbol | Parameter | Conditions | $T_A = +25°C$ | Units |
|--------|-----------|------------|----------------|-------|
| $C_{IN}$ | Input Capacitance | $V_I = 0V$ or $V_{CC}$ <br> $V_{CC} = 1.8V$, 2.5V, or 3.3V | 6.0 | pF |
| $C_{I/O}$ | Output Capacitance | $V_I = 0V$ or $V_{CC}$, <br> $V_{CC} = 1.8V$, 2.5V or 3.3V | 7.0 | pF |
| $C_{PD}$ | Power Dissipation Capacitance | $V_I = 0V$ or $V_{CC}$, $f = 10$ MHz <br> $V_{CC} = 1.8V$, 2.5V or 3.3V | 20.0 | pF |

# AC Loading and Waveforms (V$_{CC}$ 3.3V $\pm$ 0.3V to 1.8V $\pm$ 0.15V)
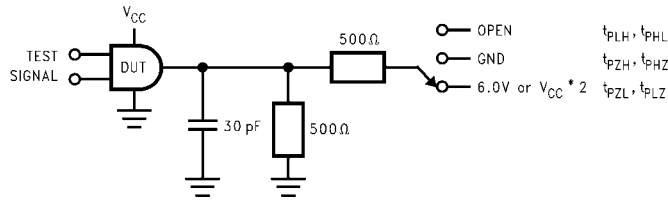


**FIGURE 1. AC Test Circuit**

| TEST | SWITCH |
|---|---|
| t$_{PLH}$, t$_{PHL}$ | Open |
| t$_{PZL}$, t$_{PLZ}$ | 6V at V$_{CC}$ = 3.3V $\pm$ 0.3V; V$_{CC}$ x 2 at V$_{CC}$ = 2.5V $\pm$ 0.2V; 1.8V $\pm$ 0.15V |
| t$_{PZH}$, t$_{PHZ}$ | GND |
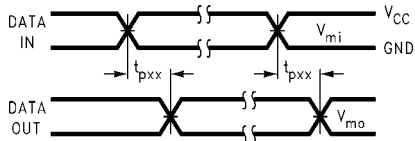


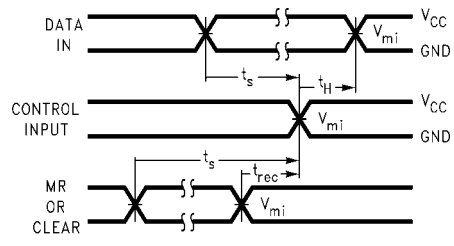**FIGURE 2. Waveform for Inverting and Non-inverting Functions**
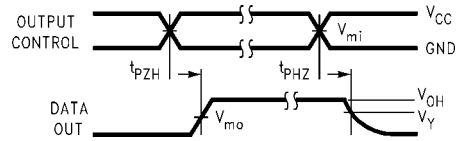


**FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic**
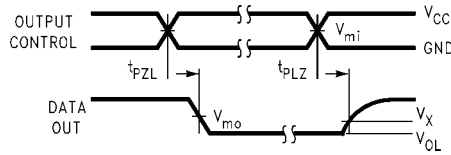


**FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic**
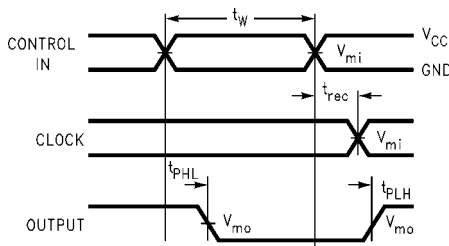


**FIGURE 5. Propagation Delay, Pulse Width and t$_{rec}$ Waveforms**



**FIGURE 6. Setup Time, Hold Time and Recovery Time for Low Voltage Logic**

| Symbol | V$_{CC}$ | | |
|---|---|---|---|
| | 3.3V $\pm$ 0.3V | 2.5V $\pm$ 0.2V | 1.8V $\pm$ 0.15V |
| V$_{mi}$ | 1.5V | V$_{CC}$/2 | V$_{CC}$/2 |
| V$_{mo}$ | 1.5V | V$_{CC}$/2 | V$_{CC}$/2 |
| V$_{X}$ | V$_{OL}$ + 0.3V | V$_{OL}$ + 0.15V | V$_{OL}$ + 0.15V |
| V$_{Y}$ | V$_{OH}$ - 0.3V | V$_{OH}$ - 0.15V | V$_{OH}$ - 0.15V |

# AC Loading and Waveforms ($V_{CC}$ 1.5V $\pm$ 0.1V)
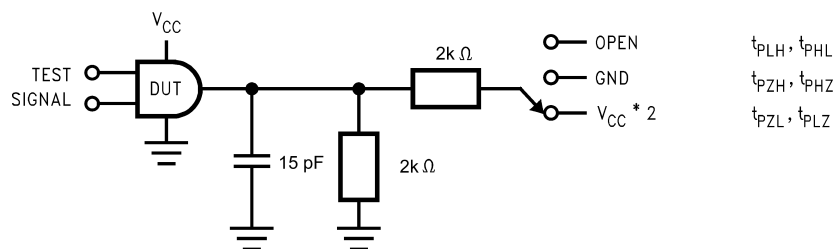


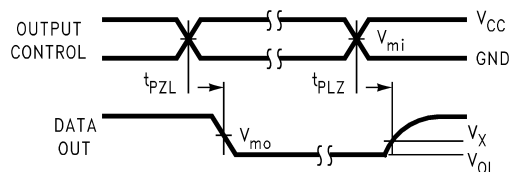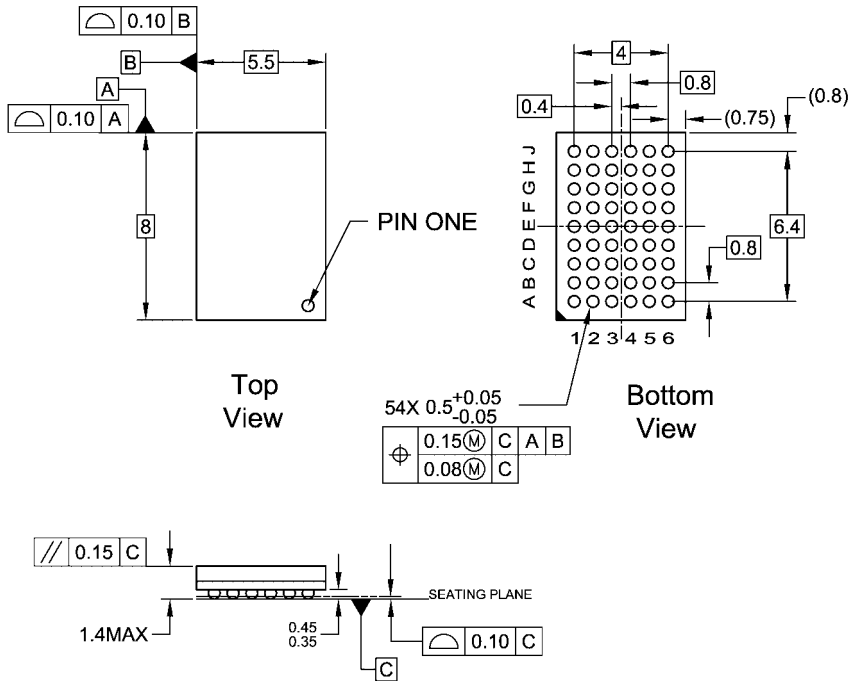| TEST | SWITCH |
|------|--------|
| $t_{PLH}$, $t_{PHL}$ | Open |
| $t_{PZL}$, $t_{PLZ}$ | $V_{CC}$ x 2 at $V_{CC}$ = 1.5 $\pm$ 0.1V |
| $t_{PZH}$, $t_{PHZ}$ | GND |

**FIGURE 7. AC Test Circuit**
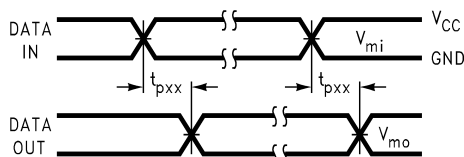


**FIGURE 8. Waveform for Inverting and Non-inverting Functions**
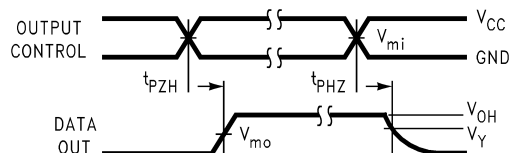


**FIGURE 9. 3-STATE Output High Enable and Disable Times for Low Voltage Logic**



**FIGURE 10. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic**

| Symbol | $V_{CC}$ |
|--------|----------|
|        | **1.5V $\pm$ 0.1V** |
| $V_{mi}$ | $V_{CC}/2$ |
| $V_{mo}$ | $V_{CC}/2$ |
| $V_X$ | $V_{OL}$ + 0.1V |
| $V_Y$ | $V_{OH}$ − 0.1V |

**Physical Dimensions** inches (millimeters) unless otherwise noted

| 0.10 | B |

B ◄ 5.5 ►

A

| 0.10 | A |

8

PIN ONE

Top
View

4

0.8

0.4

(0.8)

(0.75)

A B C D E F G H J

6.4

0.8

1/2 3/4 5 6

Bottom
View

54X 0.5 +0.05 -0.05

| ⊕ | 0.15Ⓜ | C | A | B |
| | 0.08Ⓜ | C | | |

| // | 0.15 | C |

SEATING PLANE

1.4MAX

0.45
0.35

| 0.10 | C |

C

NOTES:
A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
   .35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM  CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA54A
(Preliminary)**

# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION

DETAIL A
TYPICAL

MTD56 (REV B)
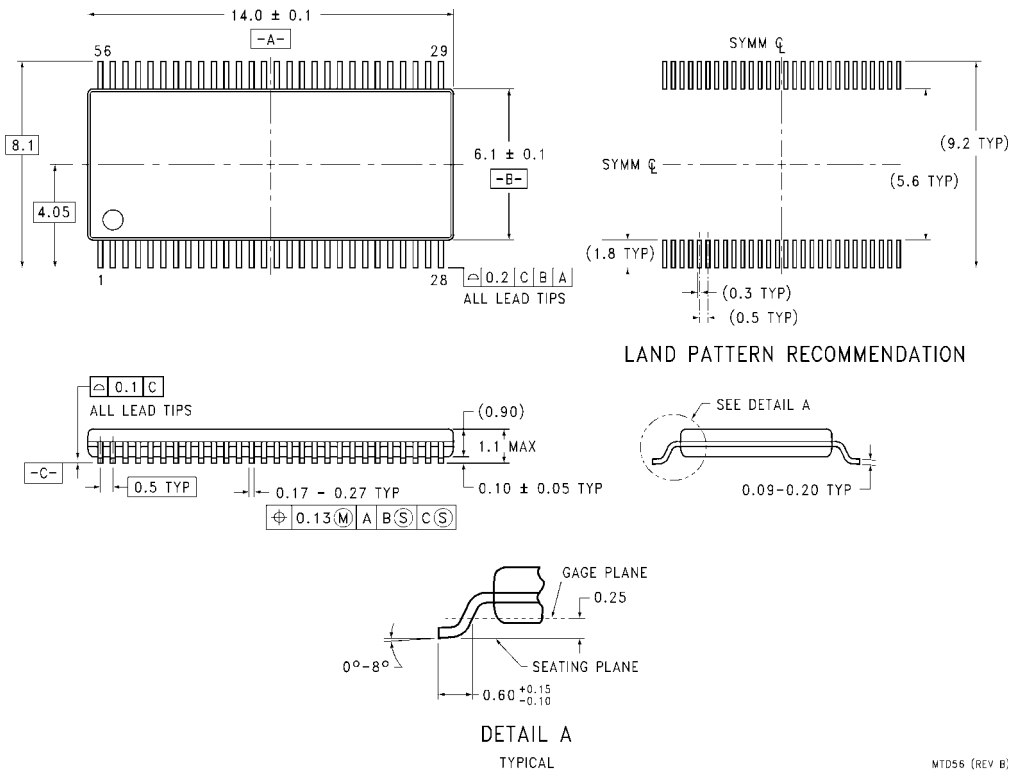
**56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide**
**Package Number MTD56**

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