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74VHC16373

16-BIT D-TYPE LATCH WITH 3-STATE OUTPUTS NON INVERTING

- HIGH SPEED:
 $t_{PD} = 5.0 \text{ ns (TYP.) at } V_{CC} = 5V$
- LOW POWER DISSIPATION:
 $I_{CC} = 4 \mu\text{A (MAX.) at } T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- POWER DOWN PROTECTION ON INPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 8 \text{ mA (MIN)}$
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC(OPR)} = 2V \text{ to } 5.5V$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 16373
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE: $V_{OLP} = 0.9V \text{ (MAX.)}$

DESCRIPTION

The 74VHC16373 is an advanced high-speed CMOS 16 BIT D-TYPE LATCH with 3 STATE OUTPUTS NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology.

These 16 bit D-TYPE latches are byte controlled by two latch enable inputs (nLE) and two output enable inputs (nOE).

While the nLE input is held at a high level, the nQ outputs will follow the data (D) inputs.

When the nLE is taken LOW, the nQ outputs will be latched at the logic level of D data inputs.

When the (nOE) input is low, the nQ outputs will be in a normal logic state (high or low logic level); when nOE is at high level, the outputs will be in a high impedance state.

Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V.

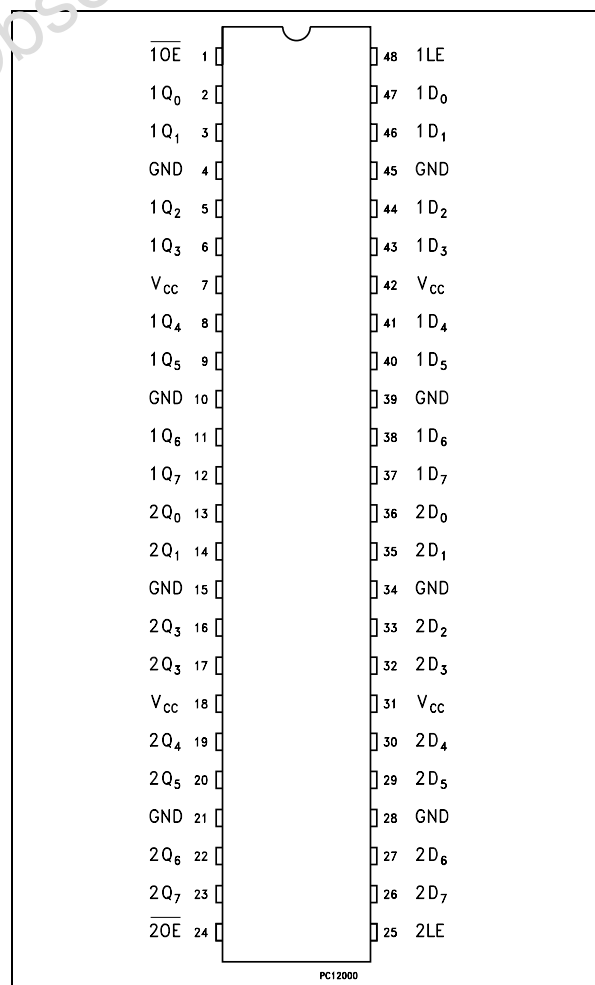
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.



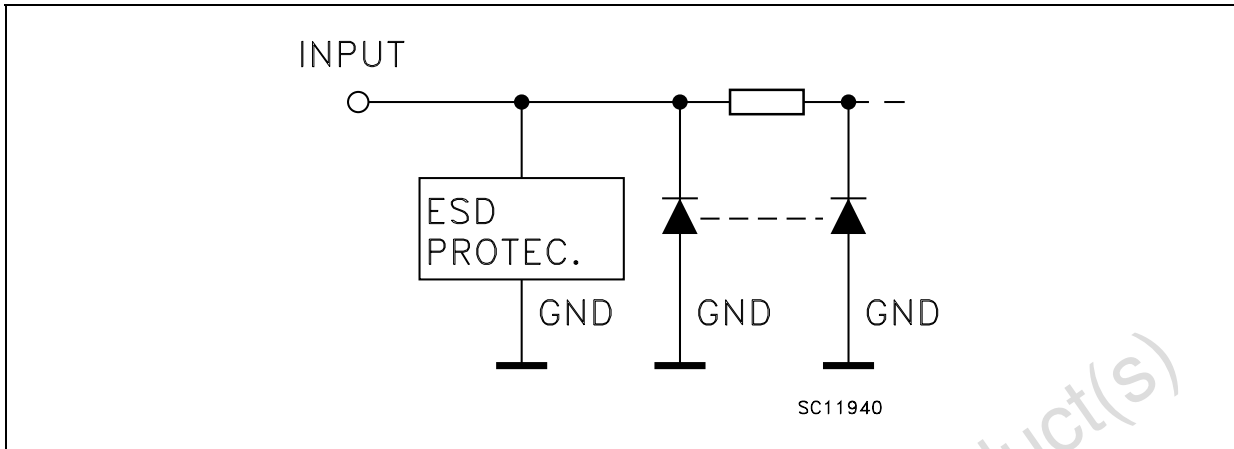
ORDER CODES

PACKAGE	TU3E	T & R
TSSOP		74VHC16373TTR

PIN CONNECTION



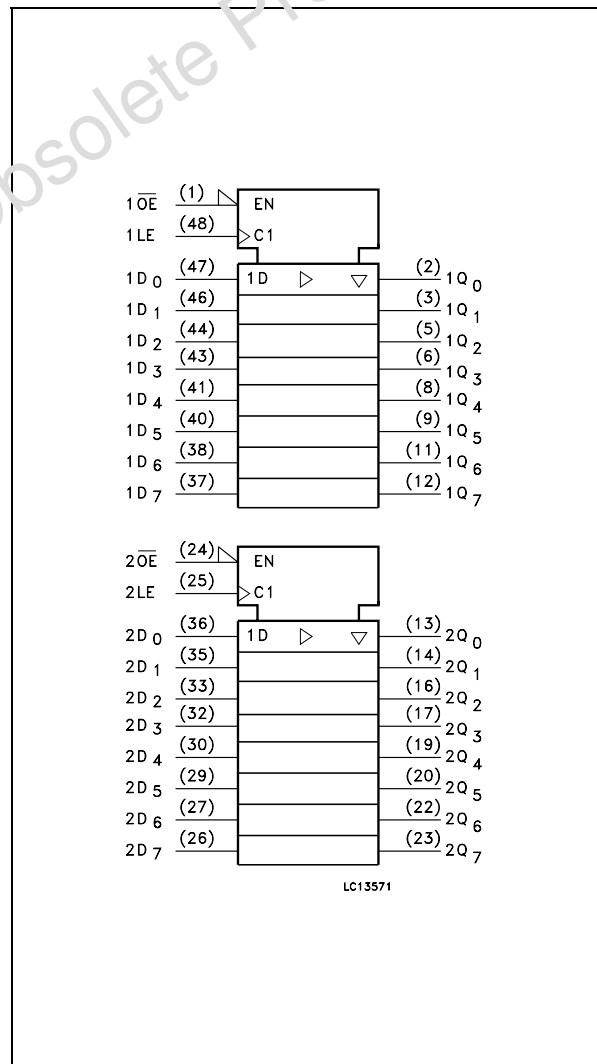
INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	1OE	3 State Output Enable Input (Active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q0 to 1Q7	3-State Outputs
13, 14, 16, 17, 19, 20, 22, 23	2Q0 to 2Q7	3-State Outputs
24	2OE	3 State Output Enable Input (Active LOW)
25	2LE	Latch Enable Input*
36, 35, 33, 32, 30, 29, 27, 26	2D0 to 2D7	Data Inputs
47, 46, 44, 43, 41, 40, 38, 37	1D0 to 1D7	Data Inputs
48	1LE	Latch Enable Input
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V _{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS



TRUTH TABLE

INPUTS			OUTPUT
OE	LE	D	Q
H	X	X	Z
L	L	X	NO CHANGE *
L	H	L	L
L	H	H	H

X : Don't Care
 Z : High Impedance
 * : Q outputs are latched at the time when the LE input is taken low logic level.

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		3.0 to 5.5		0.7V _{CC}			0.7V _{CC}		0.7V _{CC}		
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		3.0 to 5.5				0.3V _{CC}		0.3V _{CC}		0.3V _{CC}	
V _{OH}	High Level Output Voltage	2.0	I _O =-50 μA	1.9	2.0		1.9		1.9		V
		3.0	I _O =-50 μA	2.9	3.0		2.9		2.9		
		4.5	I _O =-50 μA	4.4	4.5		4.4		4.4		
		3.0	I _O =-4 mA	2.58			2.48		2.4		
		4.5	I _O =-8 mA	3.94			3.8		3.7		
V _{OL}	Low Level Output Voltage	2.0	I _O =50 μA		0.0	0.1		0.1		0.1	V
		3.0	I _O =50 μA		0.0	0.1		0.1		0.1	
		4.5	I _O =50 μA		0.0	0.1		0.1		0.1	
		3.0	I _O =4 mA			0.36		0.44		0.55	
		4.5	I _O =8 mA			0.36		0.44		0.55	
I _{OZ}	High Impedance Output Leakage Current	5.5	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND			±0.25		± 2.5		± 5	μA
I _I	Input Leakage Current	0 to 5.5	V _I = 5.5V or GND			± 0.1		± 1		± 1	μA
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			4		40		40	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3\text{ns}$)

Symbol	Parameter	Test Condition			Value						Unit	
		V_{CC} (V)	C_L (pF)		$T_A = 25^\circ\text{C}$			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t_{PLH} t_{PHL}	Propagation Delay Time LE to Qn	3.3(*)	15			5.5	13	1	15	1	15	ns
		3.3(*)	50			7	14.5	1	16.5	1	16.5	
		5.0(**)	15			3.6	8.5	1	9.5	1	9.5	
		5.0(**)	50			5	9.5	1	10.5	1	10.5	
t_{PLH} t_{PHL}	Propagation Delay Time Dn to Qn	3.3(*)	15			5.5	13	1	15	1	15	ns
		3.3(*)	50			7.5	14	1	16	1	16	
		5.0(**)	15			4	8.2	1	9.5	1	9.5	
		5.0(**)	50			5	9.2	1	10.5	1	10.5	
t_{PZL} t_{PZH}	Output Enable Time	3.3(*)	15			5.2	13	1	15	1	15	ns
		3.3(*)	50			7.6	14.9	1	16	1	16	ns
		5.0(**)	15			4	9.1	1	10	1	10	ns
		5.0(**)	50			5	10.1	1	11.5	1	11.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time	3.3(*)	50			9	15.5	1	17	1	17	ns
		5.0(**)	50			8	10.5	1	11.5	1	11.5	
t_w	Pulse Width (LE) HIGH	3.3(*)				5			5		5	ns
		5.0(**)				5			5		5	
t_s	Setup Time Dn to LE HIGH or LOW	3.3(*)				4			4		4	ns
		5.0(**)				4			4		4	
t_h	Hold Time Dn to LE HIGH or LOW	3.3(*)				1			1		1	ns
		5.0(**)				1			1		1	
t_{OSLH} t_{OSHL}	Output to Output Skew time (note 1)	3.3(*)	50				1.5		1.5		1.5	ns
		5.0(**)	50				1		1		1	

(*) Voltage range is $3.3\text{V} \pm 0.3\text{V}$ (**) Voltage range is $5.0\text{V} \pm 0.5\text{V}$ Note 1 : Parameter guaranteed by design. $t_{soLH} = |t_{pLHm} - t_{pLHn}|$; $t_{soHL} = |t_{pHLm} - t_{pHLn}|$

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition			Value						Unit	
		V_{CC} (V)			$T_A = 25^\circ\text{C}$			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C_{IN}	Input Capacitance					2.5	10		10		10	pF
C_{OUT}	Output Capacitance					4						pF
C_{PD}	Power Dissipation Capacitance (note 1)	5.0	$f_{IN} = 10\text{MHz}$			21						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/n$ (per Latch)

DYNAMIC SWITCHING CHARACTERISTICS

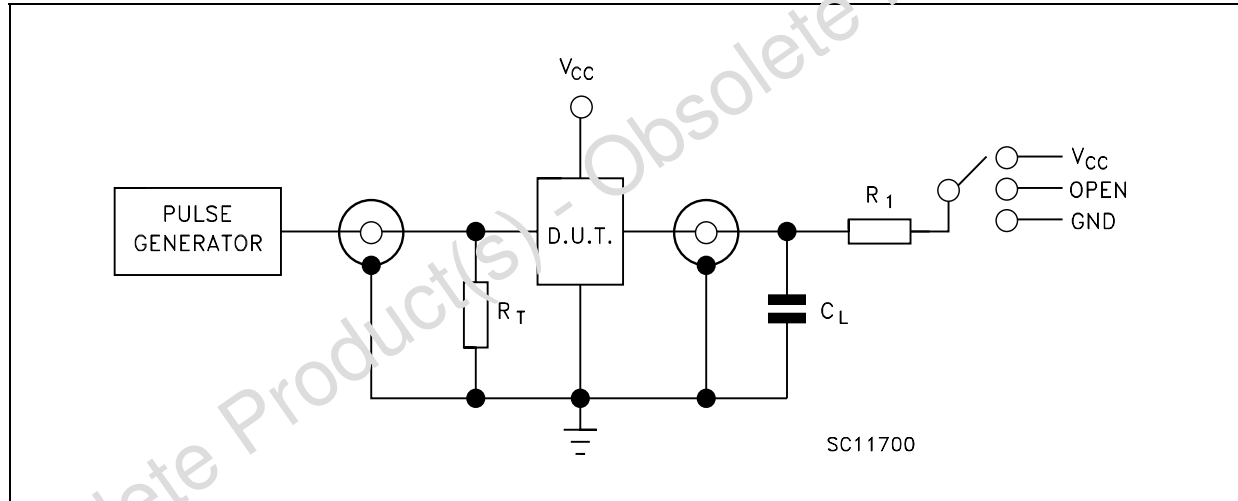
Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)	C _L (pF)	T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	5.0	C _L = 50 pF		0.6	0.9					V
V _{OLV}				-0.9	-0.6						
V _{IHD}	Dynamic High Voltage Input (note 1, 3)	5.0		3.5							V
V _{ILD}	Dynamic Low Voltage Input (note 1, 3)	5.0				1.5					V

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 5.0V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 5.0V. Inputs under test switching: 5.0V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

TEST CIRCUIT



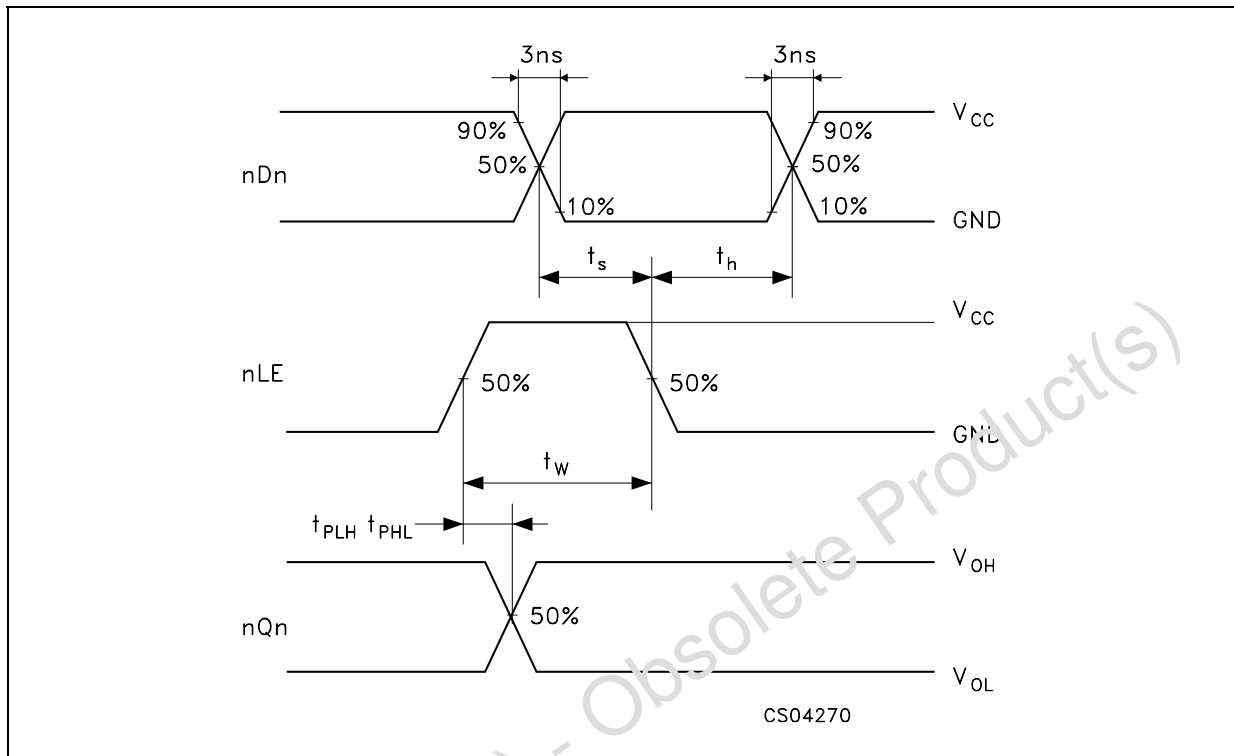
TEST	SWITCH
t _P .H, t _{PHL}	Open
t _{PZL} , t _{PLZ}	V _{CC}
t _{PZH} , t _{PHZ}	GND

C_L = 15/50 pF or equivalent (includes jig and probe capacitance)

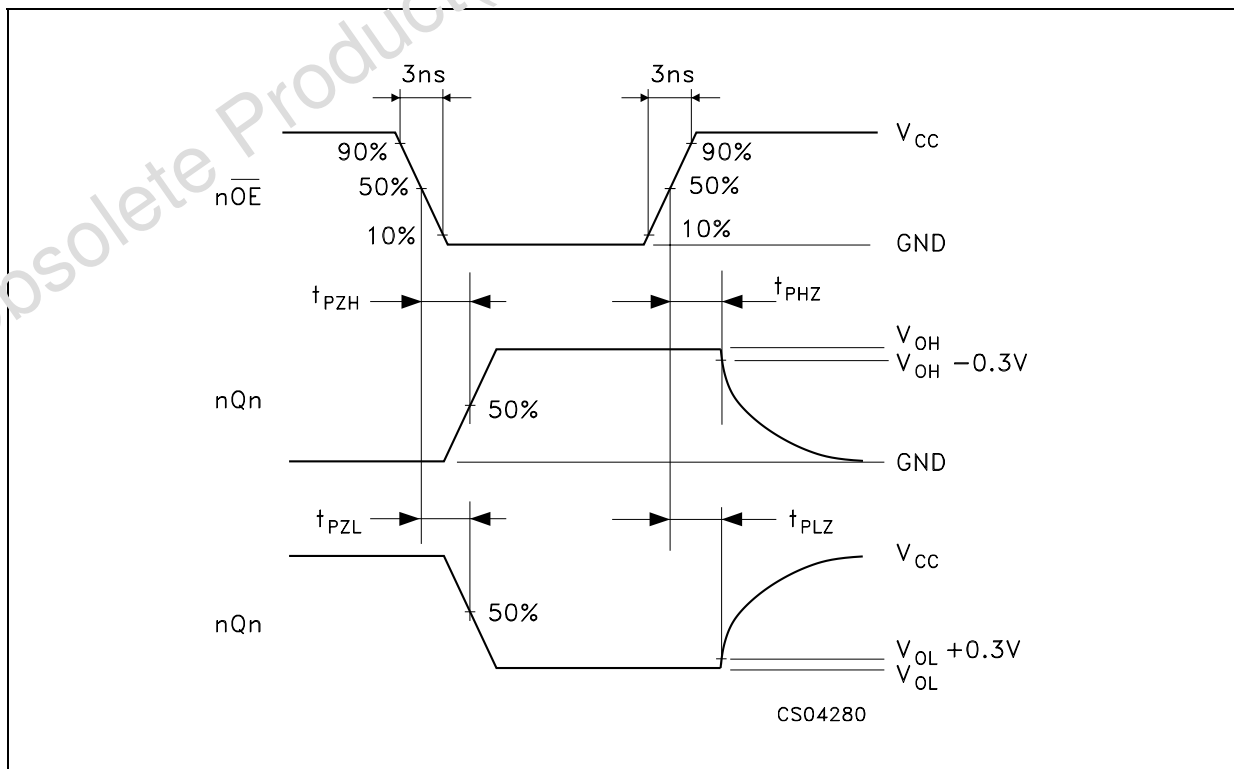
R_L = R₁ = 1KΩ or equivalent

R_T = Z_{OUT} of pulse generator (typically 50Ω)

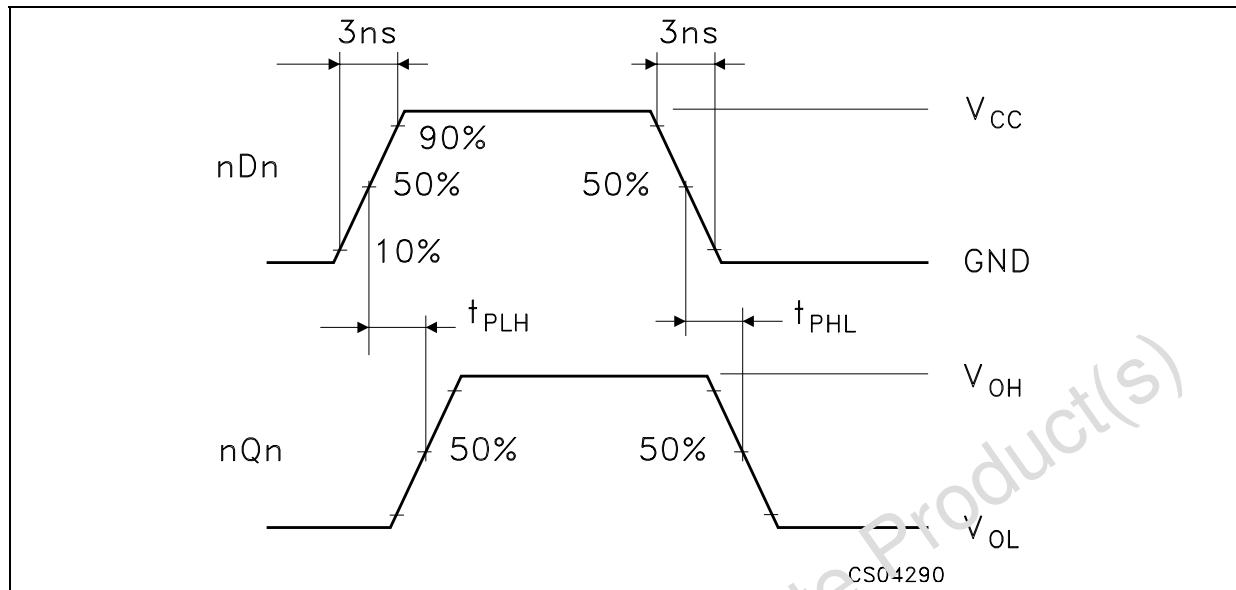
WAVEFORM 1 : LE TO Qn PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn TO LE SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)



WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)

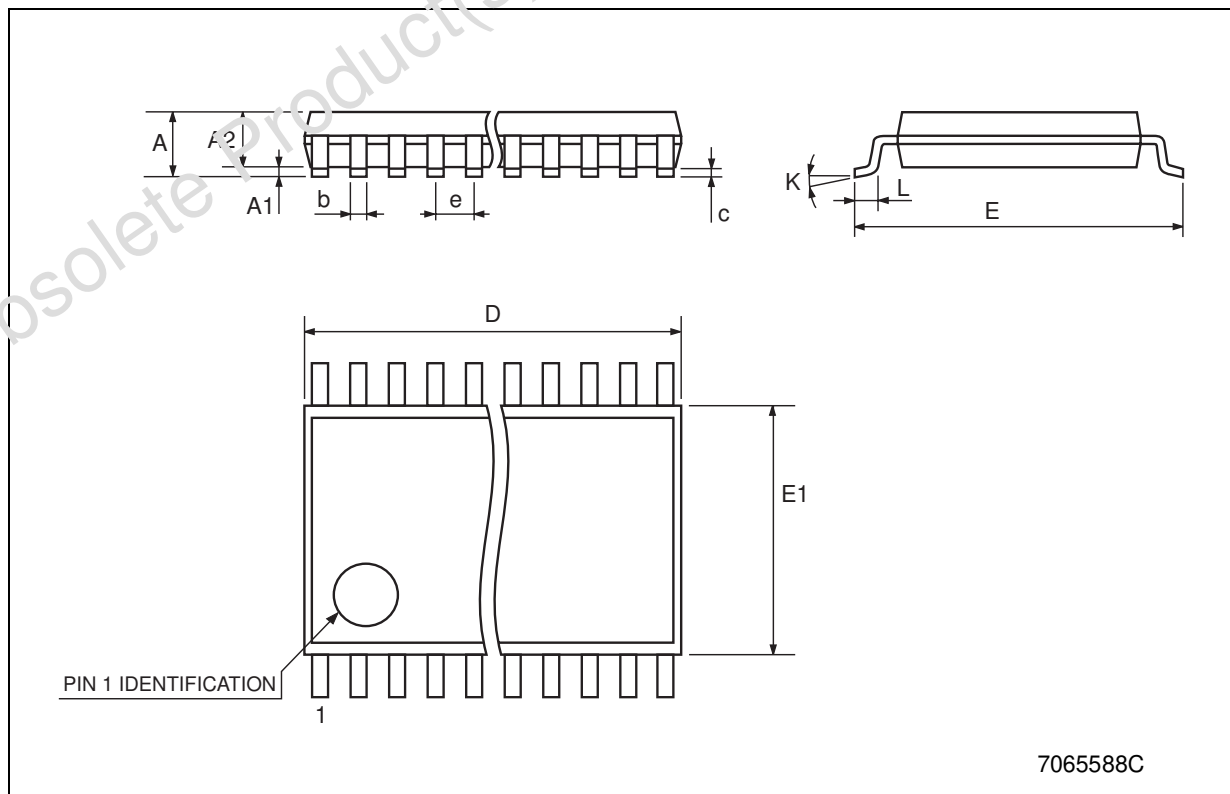


WAVEFORM 3 : PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)



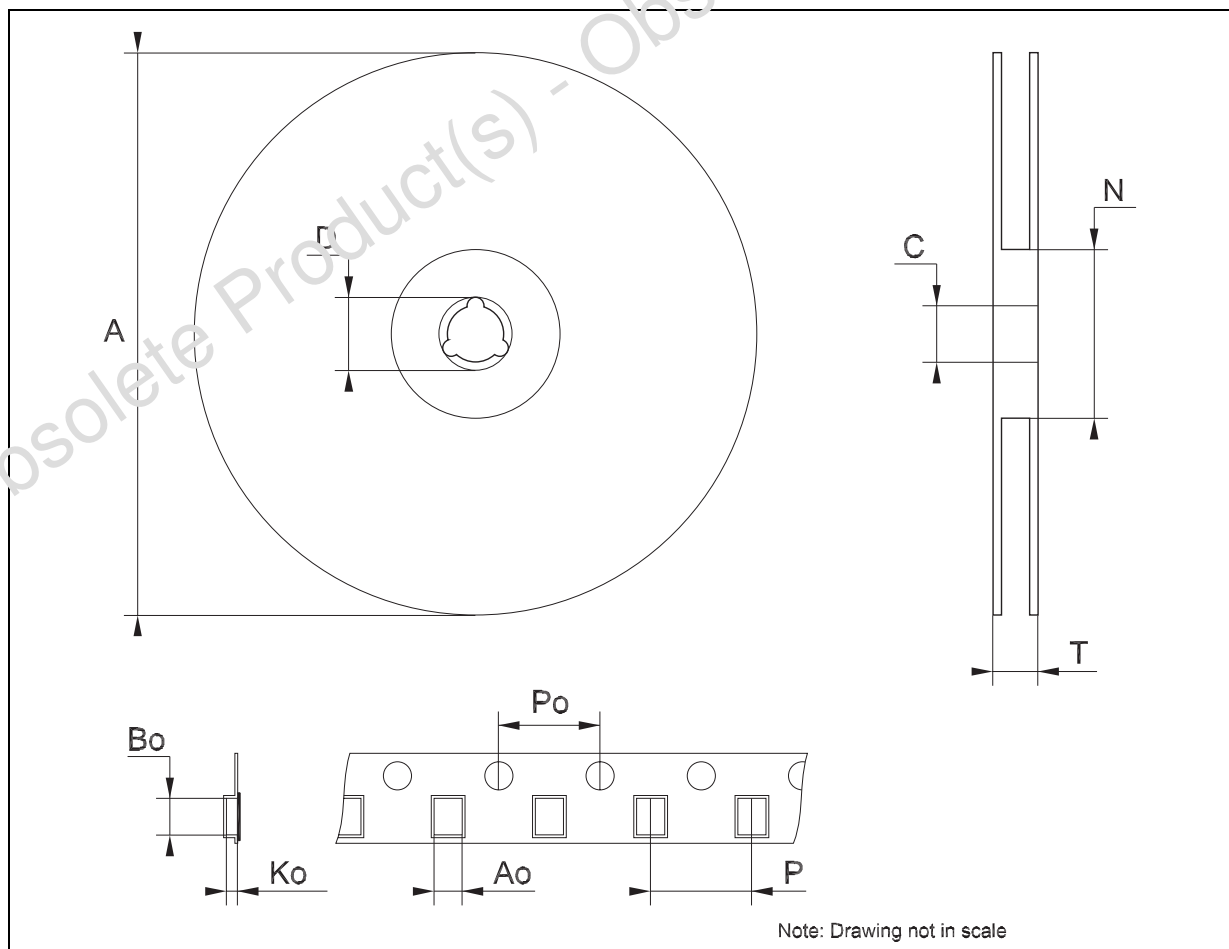
TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	12.4		12.6	0.488		0.496
E		8.1 BSC			0.318 BSC	
E1	6.0		6.2	0.236		0.244
e		0.5 BSC			0.0197 BSC	
K	0°		8°	0°		8°
L	0.50		0.75	0.020		0.030



Tape & Reel TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	8.7		8.9	0.343		0.350
Bo	13.1		13.3	0.516		0.524
Ko	1.5		1.7	0.059		0.067
Po	3.9		4.1	0.155		0.161
P	11.9		12.1	0.468		0.476



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