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SPECTRUM DIGITAL INCORPORATED

eZdsp™ LF2407A

Technical Reference

2003

DSP Development Systems

eZdsp™ LF2407A
Technical Reference

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About This Manual

This document describes board level operations of the eZdsp™ LF2407A based on the Texas Instruments TMS320LF2407A Digital Signal Processor.

The eZdsp™ LF2407A is a stand-alone module--permitting engineers and software developers evaluation of certain characteristics of the TMS320LF2407A DSP to determine processor applicability to design requirements. Evaluators can create software to execute onboard or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The “eZdsp™ LF2407A” will sometimes be referred to as the “eZdsp”.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments TMS320F2407A Users Guide
Texas Instruments TMS320C2XX Fixed Point Assembly Language Users Guide
Texas Instruments TMS320C2XX Fixed Point C Language Users Guide
Texas Instruments TMS320C2XX Code Composer Users Guide

Chapter 1

Introduction to the eZdsp™ LF2407A

This chapter provides a description of the eZdsp™ for the TMS320LF2407A Digital Signal Processor, key features, and block diagram of the circuit board.

Topic **Page**

1.0 Overview of the eZdsp™ LF2407A

The eZdsp™ LF2407A is a stand-alone card--allowing evaluators to examine the TMS320LF2407A digital signal processor (DSP) to determine if it meets their application requirements. Furthermore, the module is an excellent platform to develop and run software for the TMS320LF2407A processor.

The eZdsp™ LF2407A is shipped with a TMS320LF2407A. The eZdsp™ LF2407A allows full speed verification of LF2407A code. With 64K words of onboard program/data RAM the eZdsp can solve a variety of problems as shipped. Three expansion connectors are provided for any necessary evaluation circuitry not provided on the as shipped configuration.

To simplify code development and shorten debugging time, a C2000 Tools Code Composer driver is provided. In addition, an onboard JTAG connector provides interface to emulators, operating with other debuggers to provide assembly language and ‘C’ high level language debug.

1.1 Key Features of the eZdsp™ LF2407A

The eZdsp™ LF2407A has the following features:

- TMS320LF2407A Digital Signal Processor
- 40 MIPS operating speed
- 64K words onboard program/data RAM
- 32K words on-chip Flash memory
- Onboard 10-MHz clock circuit
- 3 Expansion Connectors (analog, I/O, expansion)
- Onboard IEEE 1149.1 JTAG Controller
- 5-volt only operation with supplied AC adapter
- TI Code Composer tools driver
- On board IEEE 1149.1 JTAG emulation connector

1.2 Functional Overview of the eZdsp™ LF2407A

Figure 1-1 shows a block diagram of the basic configuration for the eZdsp™ LF2407A. The major interfaces of the eZdsp include the external program and data RAM, JTAG interface, and expansion interface.

The DSK interfaces to 64K Words of onboard static memory. This memory is divided between the program and data space. An external I/O interface supports 65,000 parallel I/O ports.

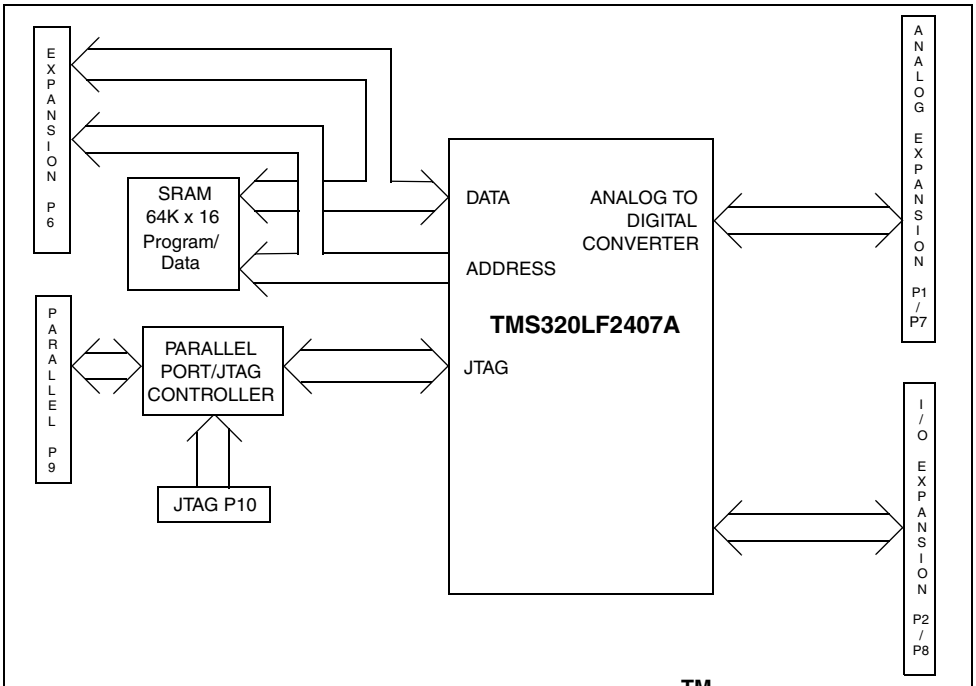

Figure 1-1, BLOCK DIAGRAM eZdsp™ LF2407A

Chapter 2

Operation of the eZdsp™ LF2407A

This chapter describes the operation of the eZdsp™ LF2407A, key interfaces and includes a circuit board outline.

2.0 The eZdsp™ LF2407A Operation

This chapter describes the eZdsp™ LF2407A, key components, and operation, Information on the eZdsp's various interfaces is also included. The eZdsp™ LF2407A consists of six major blocks of logic:

- External program and data memory
- Analog Interface
- I/O Interface
- Expansion interface
- JTAG Interface
- Parallel Port JTAG Controller Interface

2.1 The eZdsp™ LF2407A Board

The eZdsp™ LF2407A is a 5.25 x 3.0 inch, multi-layered printed circuit board, powered by an external 5-Volt only power supply. Figure 2-1 shows the layout of the LF2407A eZdsp.

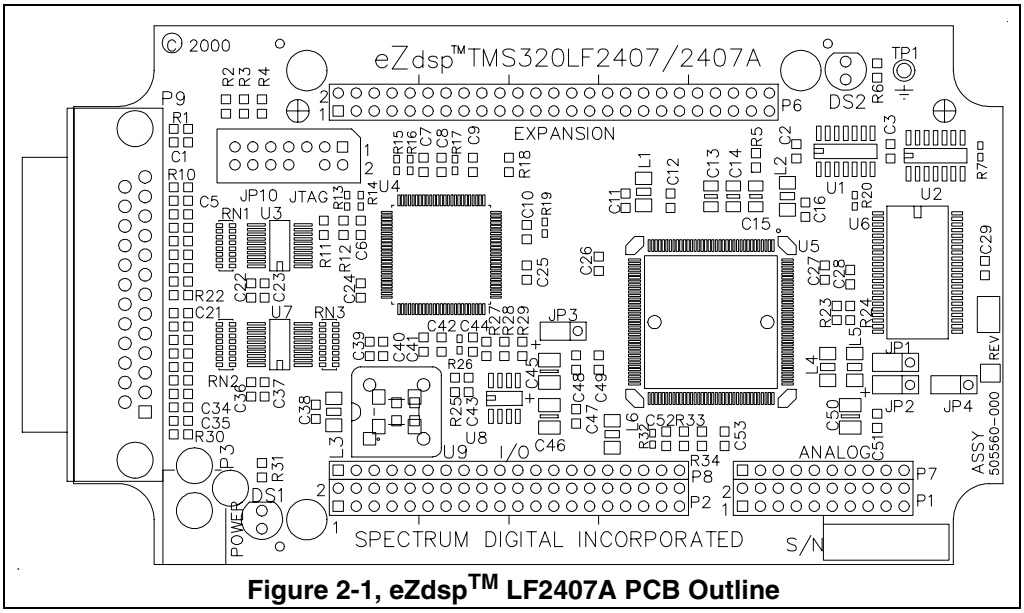

Figure 2-1, eZdsp™ LF2407A PCB Outline

2.1.1 Power Connector

The eZdsp™ LF2407A is powered by a 5-Volt only power supply, included with the unit. The power supply has a current rating of 1 amp. The unit requires 200mA. The power is supplied via connector P3. If expansion boards are connected to the eZdsp, a higher amperage power supply may be necessary. Section 2.4.2 provides more information on connector P3.

2.2 eZdsp™ LF2407A Memory Interface

The eZdsp includes the following memory: 32K words on-chip Flash memory, 64K words onboard RAM memory-- split between program and data space. The processor on the eZdsp can be configured for microcomputer or microprocessor mode.

In microprocessor mode external RAM from 0x8000-0xFFFF is mirrored at location 0x0000-0x7FFF

The eZdsp is designed so the user can develop software and load it into on board RAM for debug.

2.2.1 Program Memory

In the as shipped configuration the eZdsp™ uses the off chip program memory. This memory appears at the same address locations as the on chip Flash memory which makes it ideal for debugging software.

The figure below shows the program memory configuration on the eZdsp™ LF2407A.

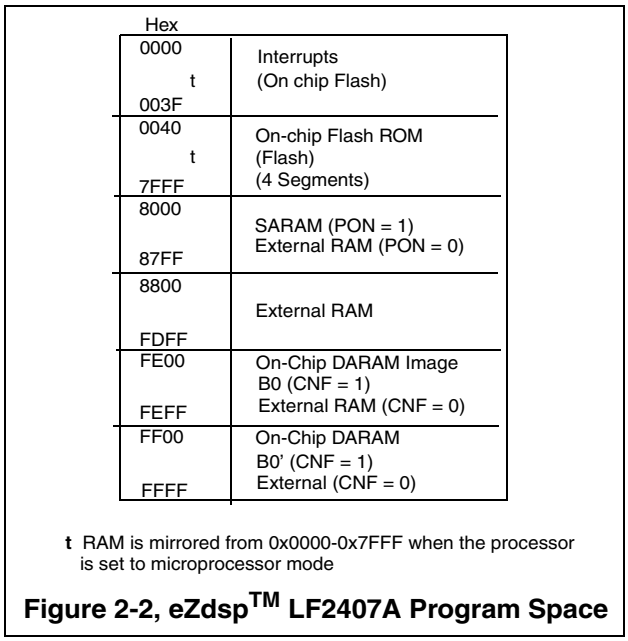

Figure 2-2, eZdsp™ LF2407A Program Space

2.2.2 Data Memory

The data memory configuration on the eZdsp^{TM} LF2407A is shown in the figure below. The location of the on-chip, memory mapped peripheral registers are also shown because these reside in the data space.

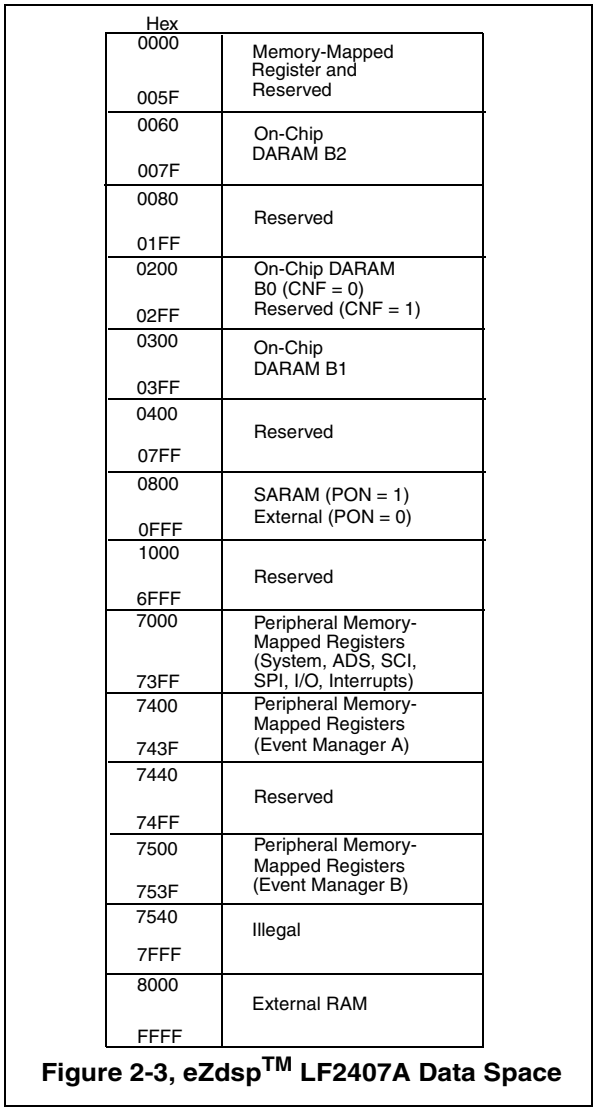

Figure 2-3, eZdsp^{TM} LF2407A Data Space

2.2.3 I/O Space

The entire I/O map for the eZdsp^{TM} LF2407A is available to the user for development.

2.3 eZdsp™ LF2407A Connectors

The eZdsp™ LF2407A has eight connectors. Pin 1 of each connector is identified by a square solder pad. The function of each connector is shown in the table below:

Table 1: eZdsp™ LF2407A Connectors

Connector	Function
P1/P7	Analog Interface
P2/P8	I/O Interface
P3	Power Connector
P6	I/O Expansion Connector
P9	Parallel Port/JTAG Controller Interface
P10	JTAG Interface

The diagram below shows the position of each connector

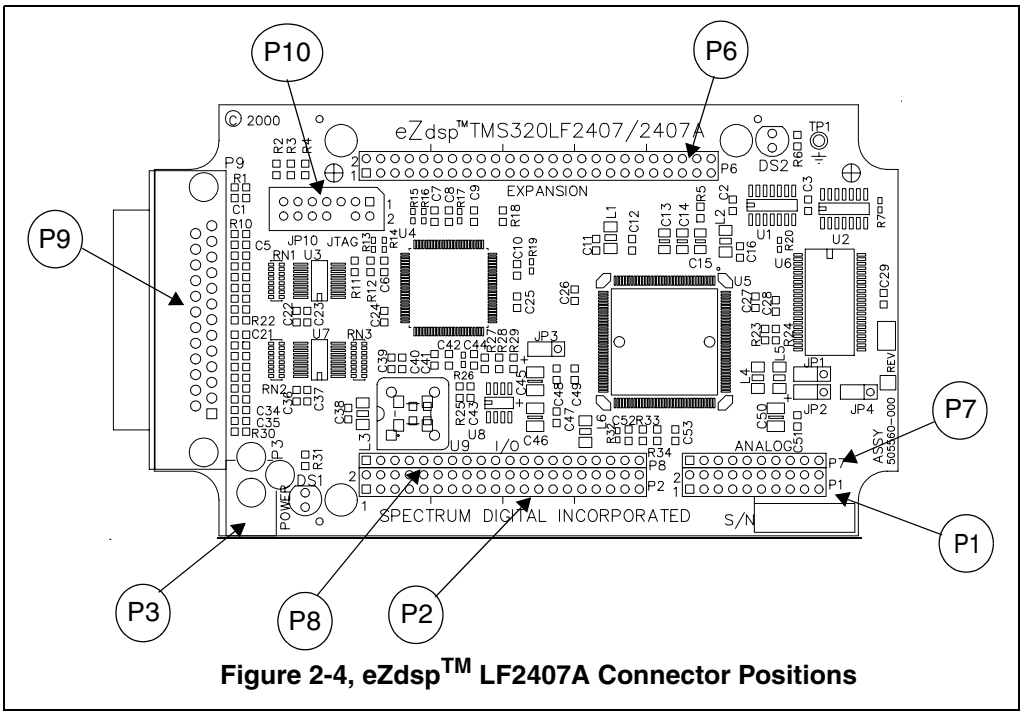

Figure 2-4, eZdsp™ LF2407A Connector Positions

2.3.1 P1/P7, Analog Interface

The positions of the 20 pins on the P1 connector and the 10 pins on the P7 are shown in the diagram below as viewed from the top of the eZdsp.

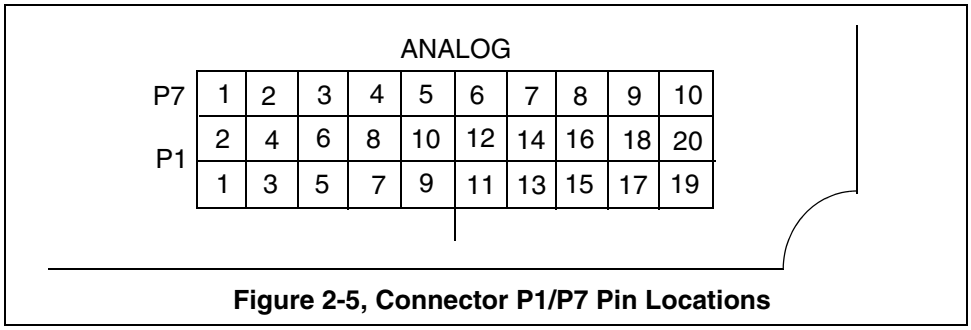

Figure 2-5, Connector P1/P7 Pin Locations

The definition of P1, which has the analog signals is shown below.

Table 2: P1, Analog Interface Connector

Pin #	Signal	Pin #	Signal
1	GND	2	ADCIN0
3	GND	4	ADCIN1
5	GND	6	ADCIN2
7	GND	8	ADCIN3
9	GND	10	ADCIN4
11	GND	12	ADCIN5
13	GND	14	ADCIN6
15	GND	16	ADCIN7
17	GND	18	VREFLO
19	GND	20	VREFHI

The definition of P7, which also has the Analog interface is shown below.

Table 3: P7, Analog Interface Connector

Pin #	Signal
1	ADCIN8
2	ADCIN9
3	ADCIN10
4	ADCIN11
5	ADCIN12
6	ADCIN13
7	ADCIN14
8	ADCIN15
9	RESERVED
10	RESERVED

2.3.2 P2/P8, I/O Interface

The positions of the 40 pins on the P2 and the 20 pins on the P8 connectors are shown in the diagram below as viewed from the top of the eZdsp.

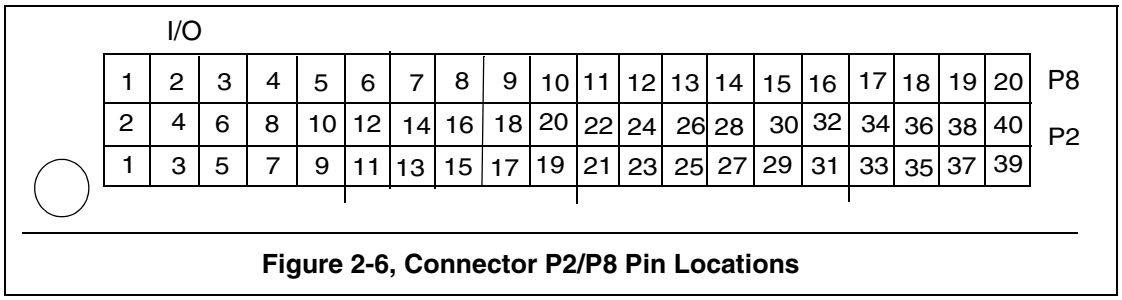

Figure 2-6, Connector P2/P8 Pin Locations

The definition of P2, which has I/O signal interface is shown below.

Table 4: P2, I/O Interface Connector

Pin #	Signal	Pin #	Signal
1	+5V	2	+5V
3	SCITXD/IOPA0	4	SCIRXD/IOPA1
5	XINT1-/IOPA2	6	CAP1/QEP1/IOPA3
7	CAP2/QEP2/IOPA4	8	CAP3/IOPA5
9	PWM1/IOPA6	10	PWM2/IOPA7
11	PWM3/IOPB0	12	PWM4/IOPB1
13	PWM5/IOPB2	14	PWM6/IOPB3
15	T1PWM/T1CMP/IOPB4	16	T2PWM/T2CMP/IOPB5
17	TDIRA/IOPB6	18	TCLKINA/IOPB7
19	GND	20	GND
21	WNR/IOPC0	22	BIO-/IOPC1
23	SPISIMO/IOPC2	24	SPISOMI/IOPC3
25	SPICLK/IOPC4	26	SPISTE/IOPC5
27	CANTX/IOPC6	28	CANRX/IOPC7
29	CLKOUT/IOPE0	30	PWM7/IOPE1
31	PWM8/IOPE2	32	PWM9/IOPE3
33	PWM10/IOPE4	34	PWM11/IOPE5
35	PWM12/IOPE6	36	CAP4/QEP3/IOPE7
37	PDPINTA-	38	PDPINTB-
39	GND	40	GND

The definition of P8, which also has the I/O signal interface is shown below.

Table 5: P8, I/O Interface Connector

Pin #	Signal
1	+5V
2	XINT2-/ADCSOC/ IOPD0
3	EMU0/IOPD1
4	EMU1/IOPD2
5	TCK/IOPD3
6	TDI/IOPD4
7	TDO/IOPD5
8	TMS/IOPD6
9	TMS2/IOPD7
10	GND
11	CAP5/QEP4/IOPF0
12	CAP6/IOPF1
13	T3PWM/T3CMP/IOPF2
14	T4PWM/T4CMP/IOPF3
15	TDIRB/IOPF4
16	TCLKINB/IOPF5
17	IOPF6
18	RESERVED
19	RESERVED
20	GND

2.3.3 P3, Power Connector

Power (5 volts) is brought onto the eZdsp^{TM} F2407A via the P3 connector. The connector has an outside diameter of 5.5 mm. and an inside diameter of 2 mm. The position of the P3 connector is shown below.

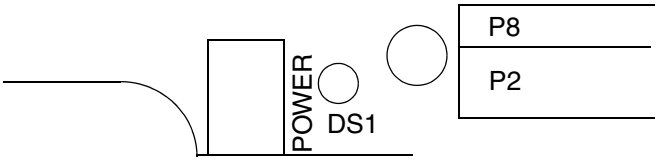

Figure 2-7, Connector P3 Location

The diagram of P3, which has the input power is shown below.

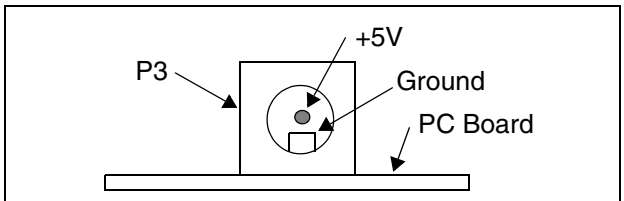

Figure 2-8, eZdsp^{TM} LF2407A Power Connector

2.3.4 P6, Expansion Connector

The positions of the 50 pins on the P6 connector are shown in the diagram below as viewed from the top of the eZdsp.

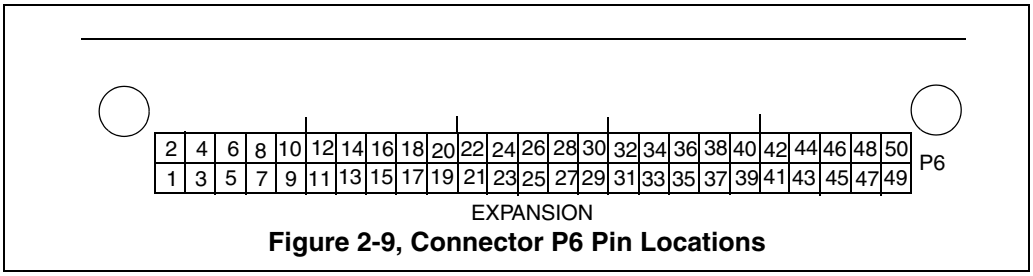

Figure 2-9, Connector P6 Pin Locations

The definition of P6, which has the memory interface signals, is shown below.

Table 6: P6, Expansion Interface Connector

Pin #	Signal	Pin #	Signal
1	+5V	2	+5V
3	D0	4	D1
5	D2	6	D3
7	D4	8	D5
9	D6	10	D7
11	D8	12	D9
13	D10	14	D11
15	D12	16	D13
17	D14	18	D15
19	A0	20	A1
21	A2	22	A3
23	A4	24	A5
25	A6	26	A7
27	A8	28	A9
29	A10	30	A11
31	A12	32	A13
33	A14	34	A15
35	GND	36	GND
37	PS-	38	DS-
39	READY	40	IS-
41	R/W-	42	STRB-
43	WE-	44	RD-
45	3.3V**	46	RESERVED
47	RS-*	48	RESERVED
49	GND	50	GND

* Bi-directional, **must** be driven with open collector.

** BR- pin on other DSKs 3.3 volt is **not** to be used for power source.

2.3.5 P9, Parallel Port/JTAG Interface

The eZdsp™ LF2407A uses a custom parallel port-JTAG interface device. This device incorporates a standard parallel port interface that supports ECP, EPP, and SPP8/bidirectional communications. The device has direct access to the integrated JTAG interface. Drivers for C2000 Code Composer tools are shipped with the eZdsp modules

2.3.6 P10, JTAG Interface

The eZdsp™ LF2407A is supplied with a 14-pin header interface, P5. This is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs.

The positions of the 14 pins on the P10 connector are shown in the diagram below as viewed from the top of the eZdsp.

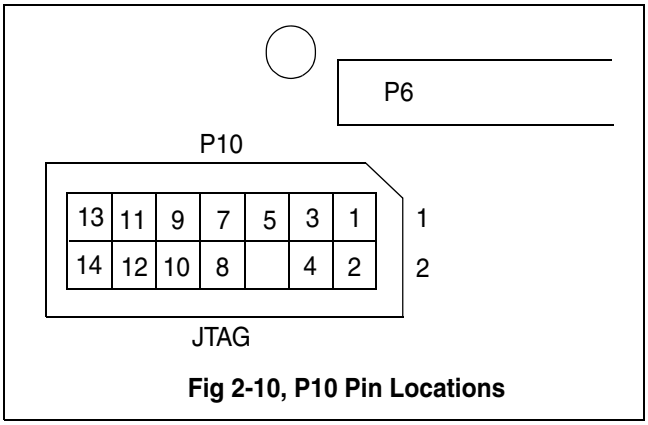

Fig 2-10, P10 Pin Locations

The definition of P10, which has the JTAG signals is shown below..

Table 7: P10, JTAG Interface Connector

Pin #	Signal	Pin #	Signal
1	TMS	2	TRST-
3	TDI	4	GND
5	PD (+5V)	6	**no pin**
7	TDO	8	GND
9	TCK-RET	10	GND
11	TCK	12	GND
13	EMU0	14	EMU1