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# **eZdsp<sup>TM</sup> F2812**

*Technical  
Reference*



eZdsp™ F2812  
Technical Reference

506265-0001 Rev. F  
September 2003

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## About This Manual

This document describes board level operations of the eZdsp™ F2812 based on the Texas Instruments TMS320F2812 Digital Signal Processor.

The eZdsp™ F2812 is a stand-alone module permitting engineers and software developers evaluation of certain characteristics of the TMS320F2812 DSP to determine processor applicability to design requirements. Evaluators can create software to execute onboard or expand the system in a variety of ways.

## Notational Conventions

This document uses the following conventions.

The “eZdsp™ F2812” will sometimes be referred to as the “eZdsp”.

“eZdsp” will include the socketed or unsocket version

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

```
equations  
!rd = !strobe&rw;
```

## Information About Cautions

This book may contain cautions.

***This is an example of a caution statement.***

A caution statement describes a situation that could potentially damage your software, hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

## Related Documents

Texas Instruments TMS320C28x DSP CPU and Instruction Set Reference Guide,  
literature #SPRU430  
Texas Instruments TMS320C28x Assembly Language Tools Users Guide,  
literature #SPRU513  
Texas Instruments TMS320C28x Optimizing C/C++ Compiler User's Guide,  
literature #SPRU514  
Texas Instruments Code Composer Studio Getting Started Guide,  
literature #SPRU509





# Chapter 1

## Introduction to the eZdsp™ F2812

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This chapter provides a description of the eZdsp™ for the TMS320F2812 Digital Signal Processor, key features, and block diagram of the circuit board.

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1.1 Key Features of the eZdsp™ F2812	1-2
1.2 Functional Overview of the eZdsp™ F2812	1-3

## **1.0 Overview of the eZdsp™ F2812**

The eZdsp™ F2812 is a stand-alone card--allowing evaluators to examine the TMS320F2812 digital signal processor (DSP) to determine if it meets their application requirements. Furthermore, the module is an excellent platform to develop and run software for the TMS320F2812 processor.

The eZdsp™ F2812 is shipped with a TMS320F2812 DSP. The eZdsp™ F2812 allows full speed verification of F2812 code. Two expansion connectors are provided for any necessary evaluation circuitry not provided on the as shipped configuration.

To simplify code development and shorten debugging time, a C2000 Tools Code Composer driver is provided. In addition, an onboard JTAG connector provides interface to emulators, operating with other debuggers to provide assembly language and 'C' high level language debug.

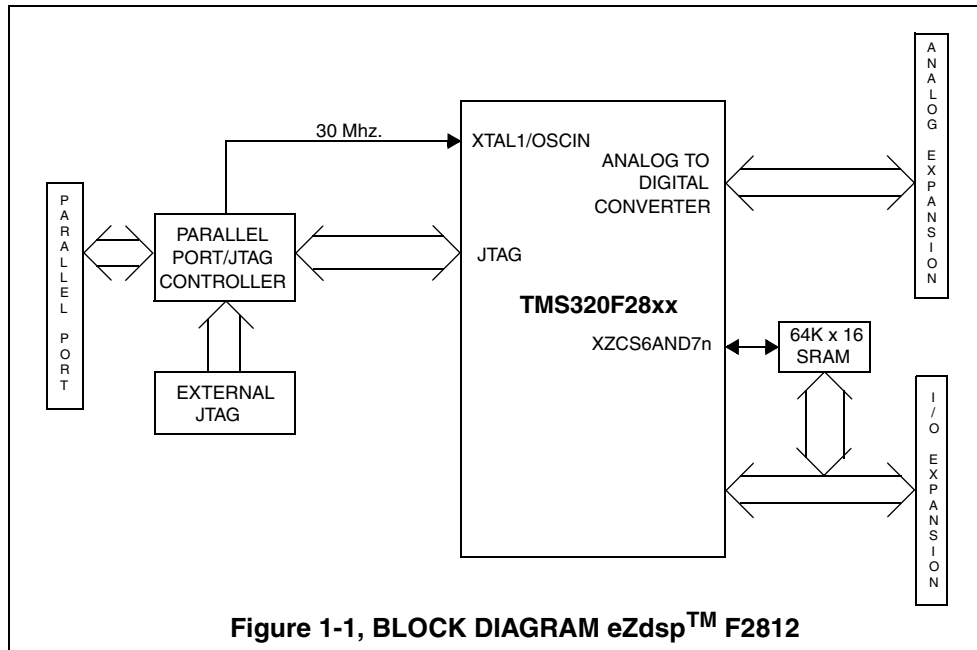
### **1.1 Key Features of the eZdsp™ F2812**

The eZdsp™ F2812 has the following features:

- TMS320F2812 Digital Signal Processor
- 150 MIPS operating speed
- 18K words on-chip RAM
- 128K words on-chip Flash memory
- 64K words off-chip SRAM memory
- 30 MHz. clock
- 2 Expansion Connectors (analog, I/O)
- Onboard IEEE 1149.1 JTAG Controller
- 5-volt only operation with supplied AC adapter
- TI F28xx Code Composer Studio tools driver
- On board IEEE 1149.1 JTAG emulation connector

## 1.2 Functional Overview of the eZdsp™ F2812

Figure 1-1 shows a block diagram of the basic configuration for the eZdsp™ F2812. The major interfaces of the eZdsp are the JTAG interface, and expansion interface.





## Chapter 2

# Operation of the eZdsp™ F2812

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This chapter describes the operation of the eZdsp™ F2812, key interfaces and includes a circuit board outline.

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## 2.0 The eZdsp™ F2812 Operation

This chapter describes the eZdsp™ F2812, key components, and operation. Information on the eZdsp's various interfaces is also included. The eZdsp™ F2812 consists of four major blocks of logic:

- Analog Interface Connector
- I/O Interface Connector
- JTAG Interface
- Parallel Port JTAG Controller Interface

## 2.1 The eZdsp™ F2812 Board

The eZdsp™ F2812 is a 5.25 x 3.0 inch, multi-layered printed circuit board, powered by an external 5-Volt only power supply. Figure 2-1 shows the layout of both the socketed and unsocketed version of the F2812 eZdsp.

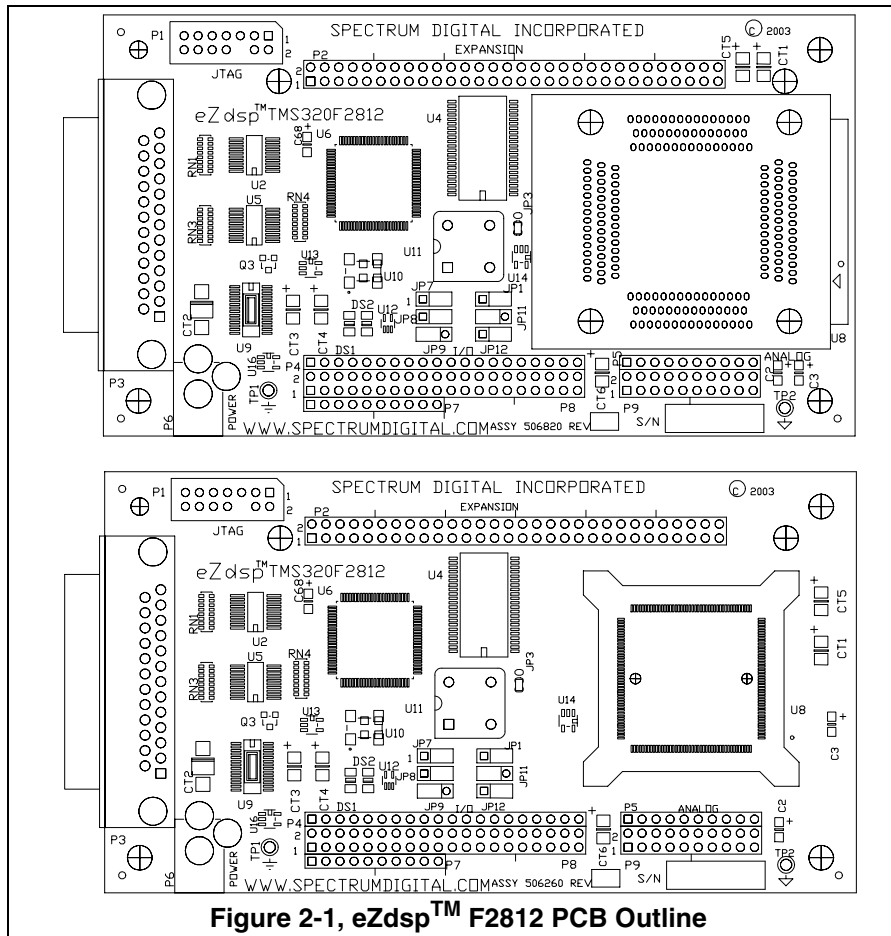


Figure 2-1, eZdsp™ F2812 PCB Outline

### 2.1.1 Power Connector

The eZdsp™ F2812 is powered by a 5-Volt only power supply, included with the unit. The unit requires 500mA. The power is supplied via connector P6. If expansion boards are connected to the eZdsp, a higher amperage power supply may be necessary. Section 2.3.6 provides more information on connector P6.

### 2.2 eZdsp™ F2812 Memory

The eZdsp includes the following on-chip memory:

- 128K x 16 Flash
- 2 blocks of 4K x 16 single access RAM (SARAM)
- 1 block of 8K x 16 SARAM
- 2 blocks of 1K x 16 SARAM

In addition 64K x 16 off-chip SRAM is provided. The processor on the eZdsp can be configured for boot-loader mode or non-boot-loader mode.

The eZdsp can load ram for debug or FLASH ROM can be loaded and run. For larger software projects it is suggested to do a initial debug with on eZdsp F2812 module which supports a total RAM environment. With careful attention to the I/O mapping in the software the application code can easily be ported to the F2812.

The table below shows the external chip select signal and its use.

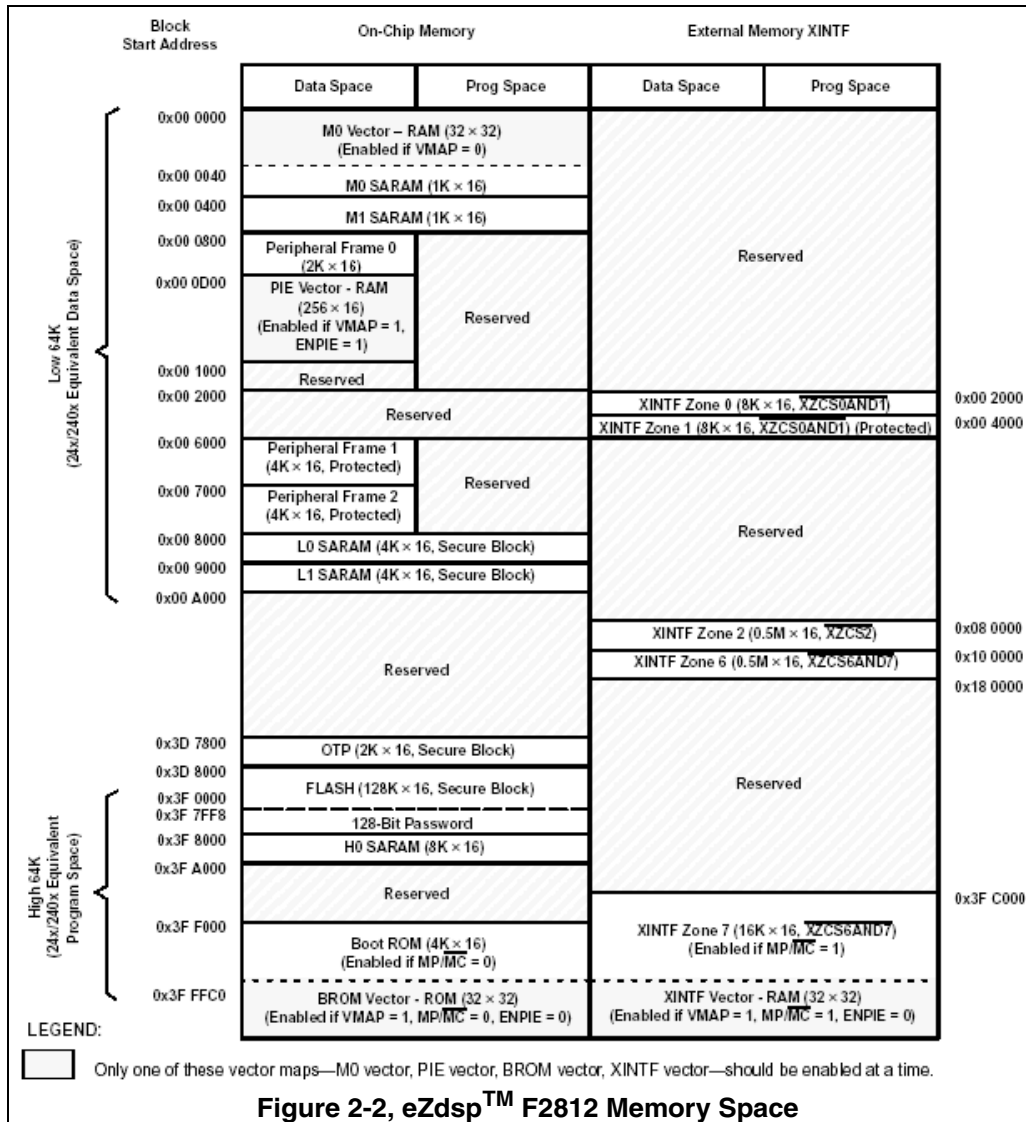
**Table 1: External Chip Select and Usage**

Chip Select Signal	Use
XZCS0AND1n	Expansion header
XZCS2n	Expansion Header
XZCS6AND7n	External SRAM



### 2.2.1 Memory Map

The figure below shows the memory map configuration on the eZdsp™ F2812.



**Note:** The on-chip flash memory has a security key which can prevent visibility when enabled.

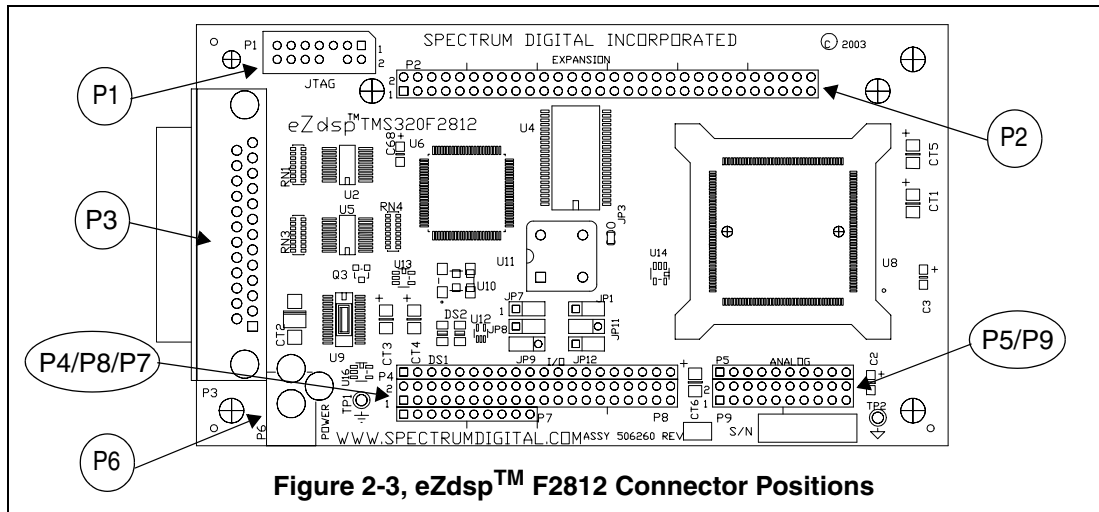
### 2.3 eZdsp™ F2812 Connectors

The eZdsp™ F2812 has five connectors. Pin 1 of each connector is identified by a square solder pad. The function of each connector is shown in the table below:

**Table 2: eZdsp™ F2812 Connectors**

Connector	Function
P1	JTAG Interface
P2	Expansion
P3	Parallel Port/JTAG Controller Interface
P4/P8/P7	I/O Interface
P5/P9	Analog Interface
P6	Power Connector

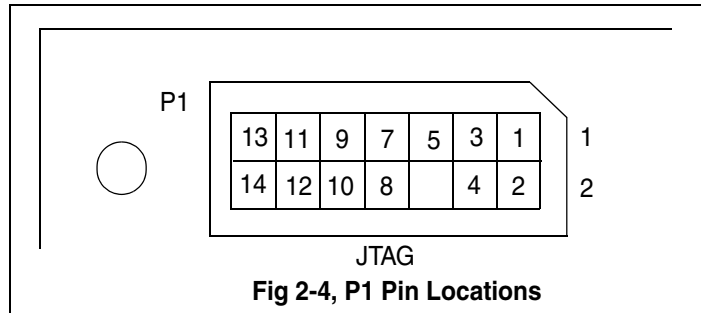
The diagram below shows the position of each connector



### 2.3.1 P1, JTAG Interface

The eZdsp™ F2812 is supplied with a 14-pin header interface, P1. This is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs.

The positions of the 14 pins on the P1 connector are shown in the diagram below as viewed from the top of the eZdsp.



The definition of P1, which has the JTAG signals is shown below.

**Table 3: P1, JTAG Interface Connector**

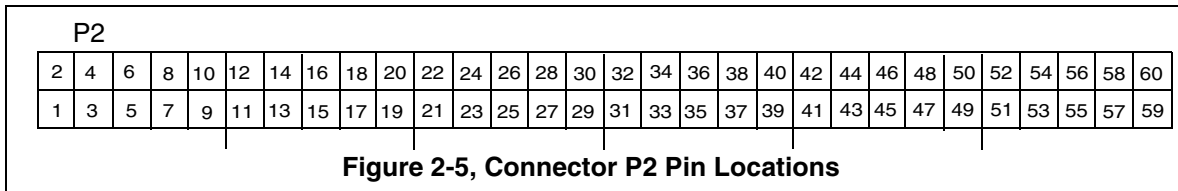
Pin #	Signal	Pin #	Signal
1	TMS	2	TRST-
3	TDI	4	GND
5	PD (+5V)	6	<b>no pin</b>
7	TDO	8	GND
9	TCK-RET	10	GND
11	TCK	12	GND
13	EMU0	14	EMU1

**WARNING !**

The TMS320F2812 supports +3.3V Input/Output levels which are NOT +5V tolerant. Connecting the eZdsp to a system with +5V Input/Output levels will damage the TMS320F2812. If the eZdsp is connected to another target then the eZdsp must be powered up first and powered down last to prevent latchup conditions.

**2.3.2 P2, Expansion Interface**

The positions of the 60 pins on the P2 connector are shown in the diagram below as viewed from the top of the eZdsp.



The definition of P2, which has the I/O signal interface is shown below.

**Table 4: P2, Expansion Interface Connector**

Pin #	Signal	Pin #	Signal
1	+3.3V/+5V/NC *	2	+3.3/+5V/NC *
3	XD0	4	XD1
5	XD2	6	XD3
7	XD4	8	XD5
9	XD6	10	XD7
11	XD8	12	XD9
13	XD10	14	XD11
15	XD12	16	XD13
17	XD14	18	XD15
19	XA0	20	XA1
21	XA2	22	XA3
23	XA4	24	XA5
25	XA6	26	XA7
27	XA8	28	XA9
29	XA10	30	XA11
31	XA12	32	XA13
33	XA14	34	XA15
35	GND	36	GND
37	XZCS0AND1n	38	XZCS2n
39	XREADY	40	10K Pull-up
41	XRnW	42	10K Pull-up
43	XWE	44	XRDn
45	+3.3V	46	XNMI/INT13
47	XRSn/RSn	48	No connect
49	GND	50	GND
51	GND	52	GND
53	XA16	54	XA17
55	XA18	56	XHOLDn
57	XHOLDAn	58	No connect
59	No connect	60	No connect

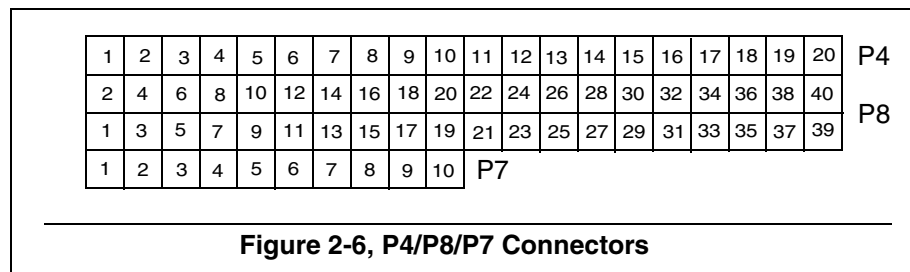
\* Default is No Connect (NC). User can jumper to +3.3V or +5V on backside of eZdsp with JP5.

### 2.3.3 P3, Parallel Port/JTAG Interface

The eZdsp™ F2812 uses a custom parallel port-JTAG interface device. This device incorporates a standard parallel port interface that supports ECP, EPP, and SPP8/bidirectional communications. The device has direct access to the integrated JTAG interface. Drivers for C2000 Code Composer tools are shipped with the eZdsp modules

### 2.3.4 P4/P8/P7, I/O Interface

The connectors P4, P8, and P7 present the I/O signals from the DSP. The layout of these connectors are shown below.



The pin definition of P4/P8 connectors are shown in the table below.

**Table 5: P4/P8, I/O Connectors**

P4 Pin #	P4 Signal	P8 Pin #	P8 Signal	P8 Pin #	P8 Signal
1	+3.3V/+5V/NC *	1	+3.3V/+5V/NC *	2	+3.3V/+5V/NC *
2	XINT2/ADCSOC	3	SCITXDA	4	SCIRXDA
3	MCLKXA	5	XINT1n/XBIO <sub>n</sub>	6	CAP1/QEP1
4	MCLKRA	7	CAP2/QEP2	8	CAP3/QEP11
5	MFSXA	9	PWM1	10	PWM2
6	MFSRA	11	PWM3	12	PWM4
7	MDXA	13	PWM5	14	PWM6
8	MDRA	15	T1PWM/T1CMP	16	T2PWM/T2CMP
9	No connect	17	TDIRA	18	TCLKINA
10	GND	19	GND	20	GND
11	CAP5/QEP4	21	No connect	22	XINT1N/XBIO <sub>n</sub>
12	CAP6/QEP12	23	SPISIMOA	24	SPISOMIA
13	T3PWM/T3CMP	25	SPICLKA	26	SPISTEA
14	T4PWM/T4CMP	27	CANTXA	28	CANRXA
15	TDIRB	29	XCLKOUT	30	PWM7
16	TCLKINB	31	PWM8	32	PWM9
17	XF/XPLLDIS <sub>n</sub>	33	PWM10	34	PWM11
18	SCITXDB	35	PWM12	36	CAP4/QEP3
19	SCIRXDB	37	T1CTRIP/PDPINTA <sub>n</sub>	38	T3CTRIP/PDPINTB <sub>n</sub>
20	GND	39	GND	40	GND

\* Default is No Connect (NC). User can jumper to +3.3V or +5V on backside of eZdsp with JP4.

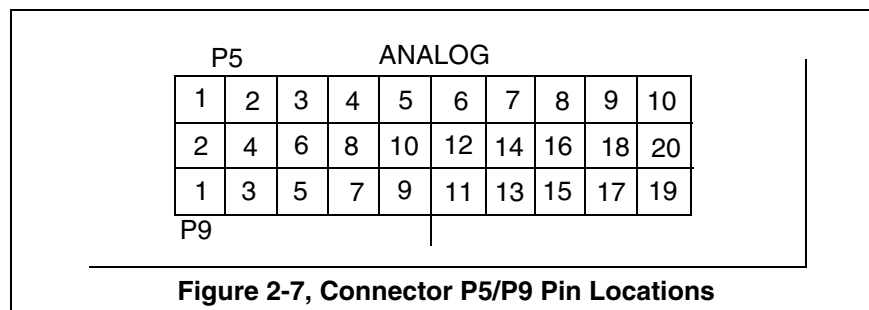
The pin definition of P7 connector is shown in the table below.

**Table 6: P7, I/O Connector**

P7 Pin #	P7 Signal
1	C1TRIPn
2	C2TRIPn
3	C3TRIPn
4	T2CTRIPn/EVASOCn
5	C4TRIPn
6	C5TRIPn
7	C6TRIPn
8	T4CTRIPn/EVBSOCn
9	No connect
10	GND

### 2.3.5 P5/P9, Analog Interface

The position of the 30 pins on the P5/P9 connectors are shown in the diagram below as viewed from the top of the eZdsp.





The definition of P5/P9 signals are shown in the table below.

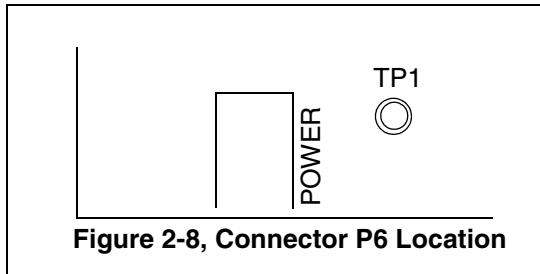
**Table 7: P5/P9, Analog Interface Connector**

P5 Pin #	Signal	P9 Pin #	Signal	P9 Pin #	Signal
1	ADCINB0	1	GND	2	ADCINA0
2	ADCINB1	3	GND	4	ADCINA1
3	ADCINB2	5	GND	6	ADCINA2
4	ADCINB3	7	GND	8	ADCINA3
5	ADCINB4	9	GND	10	ADCINA4
6	ADCINB5	11	GND	12	ADCINA5
7	ADCINB6	13	GND	14	ADCINA6
8	ADCINB7	15	GND	16	ADCINA7
9	ADCREFM	17	GND	18	VREFLO *
10	ADCREFP	19	GND	20	No connect

\* Connect VREFLO to AGND or VREFLO of target system for proper ADC operation.

### 2.3.6 P6, Power Connector

Power (5 volts) is brought onto the eZdsp™ F2812 via the P6 connector. The connector has an outside diameter of 5.5 mm. and an inside diameter of 2 mm. The position of the P6 connector is shown below.



The diagram of P6, which has the input power is shown below.

