Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

SPECTRUM DIGITAL INCORPORATED

eZdsp™ F28335

Technical Reference

2007

DSP Development Systems

eZdsp™ F28335
Technical Reference

510195-0001 Rev. C
November 2007

SPECTRUM DIGITAL, INC.
12502 Exchange Dr., Suite 440 Stafford, TX. 77477
Tel: 281.494.4505 Fax: 281.494.5310
sales@spectrumdigital.com www.spectrumdigital.com

IMPORTANT NOTICE

Spectrum Digital, Inc. reserves the right to make changes to its products or to discontinue any product or service without notice. Customers are advised to obtain the latest version of relevant information to verify data being relied on is current before placing orders.

Spectrum Digital, Inc. warrants performance of its products and related software to current specifications in accordance with Spectrum Digital's standard warranty. Testing and other quality control techniques are utilized to the extent deemed necessary to support this warranty.

Please be aware, products described herein are not intended for use in life-support appliances, devices, or systems. Spectrum Digital does not warrant, nor is it liable for, the product described herein to be used in other than a development environment.

Spectrum Digital, Inc. assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does Spectrum Digital warrant or represent any license, either express or implied, is granted under any patent right, copyright, or other intellectual property right of Spectrum Digital, Inc. covering or relating to any combination, machine, or process in which such Digital Signal Processing development products or services might be or are used.

WARNING

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user, at his own expense, will be required to take any measures necessary to correct this interference.

TRADEMARKS

eZdsp is a trademark of Spectrum Digital, Inc.

Contents

List of Figures

List of Tables

About This Manual

This document describes board level operations of the eZdsp™ F28335 based on the Texas Instruments TMS320F28335 Digital Signal Controller (DSC).

The eZdsp™ F28335 is a stand-alone module permitting engineers and software developers evaluation of certain characteristics of the TMS320F28335 DSC to determine processor applicability to design requirements. Evaluators can create software to execute onboard or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The “eZdsp™ F28335” will sometimes be referred to as the “eZdsp”.

“eZdsp” will include the socketed or unsocket version

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments TMS320F28335 Digital Signal Controllers Data Manual, literature #SPRS439
Texas Instruments TMS320C28x DSP CPU and Instruction Set Reference Guide, literature #SPRU430
Texas Instruments TMS320C28x Assembly Language Tools Users Guide, literature #SPRU513
Texas Instruments TMS320C28x Optimizing C/C++ Compiler User’s Guide, literature #SPRU514
Texas Instruments Code Composer Studio Getting Started Guide, literature #SPRU509

Table 1: Manual History

Revision	History
A	Production Release
B	Updated Figures, Text, Schematics
C	Updated Figures, Tables, Text

Table 2: Board History

PWB Revision	History
A	Production Release
B	Updated Silk-screen

Chapter 1

Introduction to the eZdsp™ F28335

This chapter provides a description of the eZdsp™ for the TMS320F28335 Digital Signal Controller, key features, and block diagram of the circuit board.

Topic **Page**

1.0 Overview of the eZdsp™ F28335

The eZdsp™ F28335 is a stand-alone card--allowing developers to evaluate the TMS320F28335 digital signal controller (DSC) to determine if it meets their application requirements. Furthermore, the module is an excellent platform to develop and run software for the TMS320F28335 processor.

The eZdsp™ F28335 is shipped with a TMS320F28335 DSC. The eZdsp™ F28335 allows full speed verification of F28335 code. Several expansion connectors are provided for any necessary evaluation circuitry not provided on the as shipped configuration.

To simplify code development and shorten debugging time, a C2000 Code Composer Studio™ driver is provided. In addition, an onboard JTAG connector provides interface to emulators, with assembly language and 'C' high level language debug.

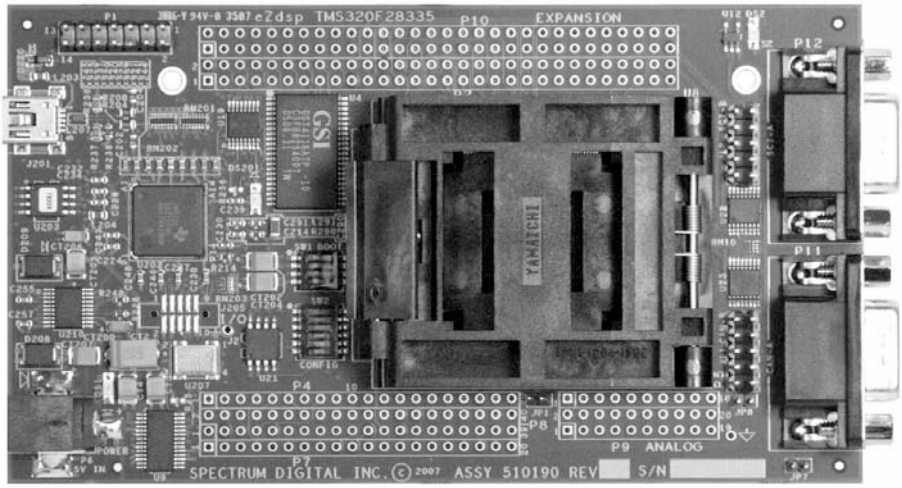

Figure 1-1, eZdsp F28335

1.1 Key Features of the eZdsp™ F28335

1.1.1 Hardware Features

The eZdsp™ F28335 has the following features:

- TMS320F28335 Digital Signal Controller
- 150 Mhz. operating speed
- On chip 32-bit floating point unit
- 68K bytes on-chip RAM
- 512K bytes on-chip Flash memory
- 256K bytes off-chip SRAM memory
- On chip 12 bit Analog to Digital (A/D) converter with 16 input channels
- 30 MHz. input clock
- On board RS-232 connector with line driver
- On board CAN 2.0 interface with line driver and connector
- Multiple Expansion Connectors (analog, I/O)
- On board embedded USB JTAG Controller
- 5-volt only operation with supplied AC adapter
- On board IEEE 1149.1 JTAG emulation connector

1.1.2 Software Features

- TI F28xx Code Composer Studio™ Integrated Development Environment, Version 3.3
- Texas Instruments' Flash APIs to support the F28335
- Texas Instruments' F28335 header files and example software

1.2 Functional Overview of the eZdsp™ F28335

Figure 1-1 shows a block diagram of the basic configuration for the eZdsp™ F28335. The major interfaces of the eZdsp are the JTAG interface, and expansion interface.

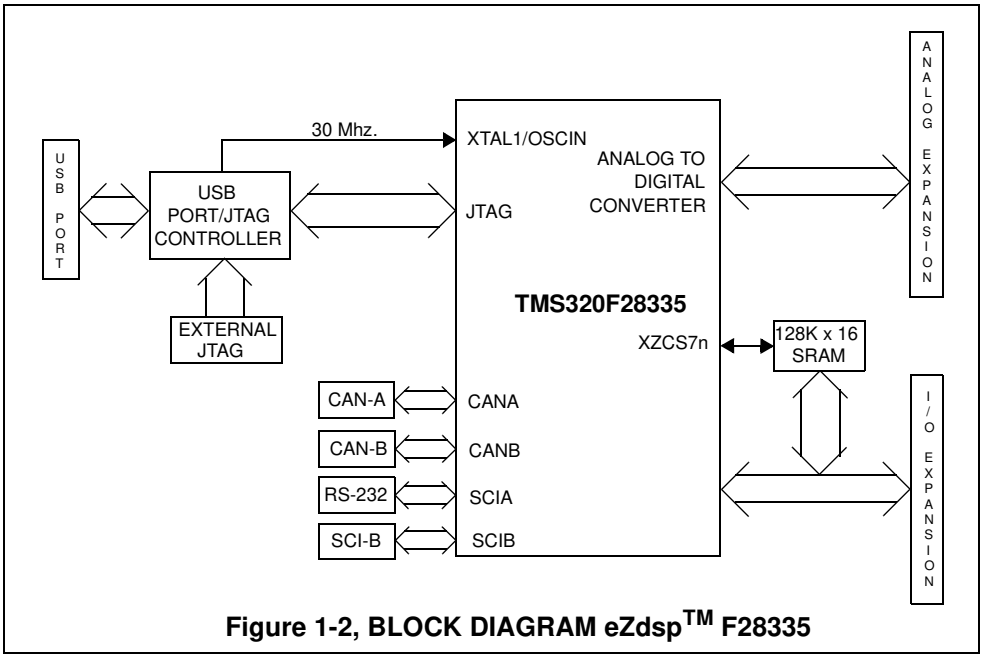

Figure 1-2, BLOCK DIAGRAM eZdsp™ F28335

Chapter 2

Operation of the eZdsp™ F28335

This chapter describes the operation of the eZdsp™ F28335, key interfaces and includes a circuit board outline.

Topic **Page**

Topic **Page**

2.0 The eZdsp™ F28335 Operation

This chapter describes the eZdsp™ F28335, key components, and operation. Information on the eZdsp's various interfaces is also included. The eZdsp™ F28335 consists of four major blocks of logic:

- Analog Interface Connector
- I/O Interface Connector
- On board Memory
- JTAG Interface
- Embedded USB JTAG Controller Interface

2.1 The eZdsp™ F28335 Board

The eZdsp™ F28335 is a 5.35 x 3.0 inch, multi-layered printed circuit board, powered by an external 5-Volt only power supply. Figure 2-1 shows the layout of the top side of the F28335 eZdsp.

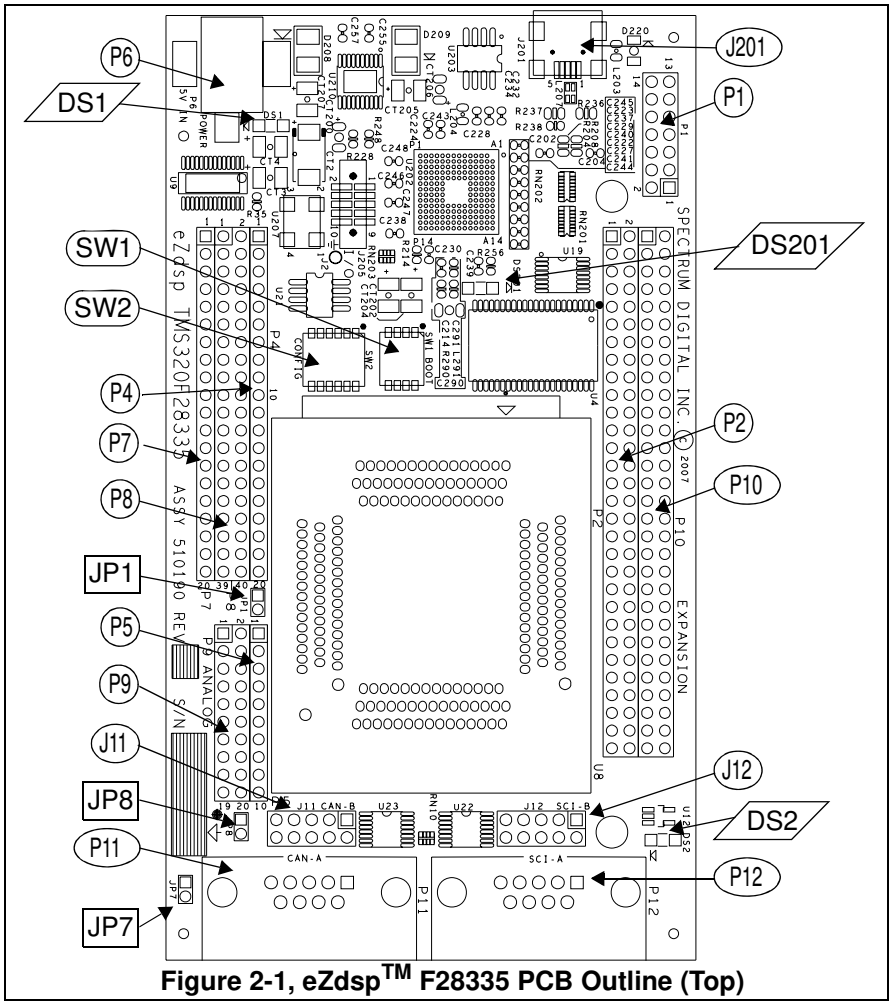

Figure 2-1, eZdsp™ F28335 PCB Outline (Top)

Figure 2-2 shows the layout of the bottom side of the F28335 eZdsp.

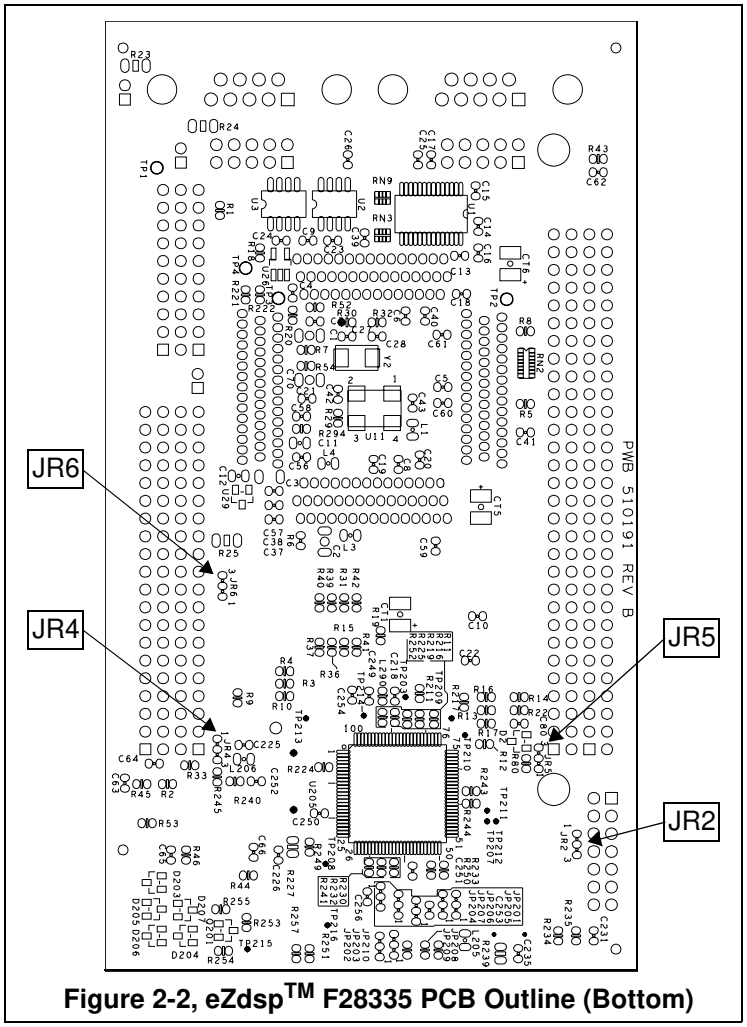

Figure 2-2, eZdsp™ F28335 PCB Outline (Bottom)

2.1.1 Power Connector

The eZdsp™ F28335 is powered by a +5 Volt only power supply, included with the unit. The power is supplied via connector P6. If expansion boards are connected to the eZdsp, a higher amperage power supply may be necessary.

2.2 eZdsp™ F28335 Memory

The eZdsp includes the following on-chip memory:

- 256K x 16 Flash
- 8 blocks of 4K x 16 single access RAM (SARAM)
- 2 blocks of 8K x 16 SARAM
- 2 blocks of 1K x 16 SARAM

In addition 128K x 16 off-chip SRAM is provided. The processor on the eZdsp can be configured for boot-loader mode or non-boot-loader mode.

The eZdsp can load ram for debug or FLASH ROM can be loaded and run. For larger software projects it is suggested to do a initial debug with on eZdsp F28335 module which supports a total RAM environment. With careful attention to the I/O mapping in the software the application code can easily be ported to the F28335.

The table below shows the external chip select signal and its use.

Table 1: External Chip Select and Usage

Chip Select Signal	Use
XZCS0n	Expansion header
XZCS6n	Expansion Header
XZCS7n	External SRAM

2.2.1 Memory Map

The figure below shows the memory map configuration on the eZdsp™ F28335.

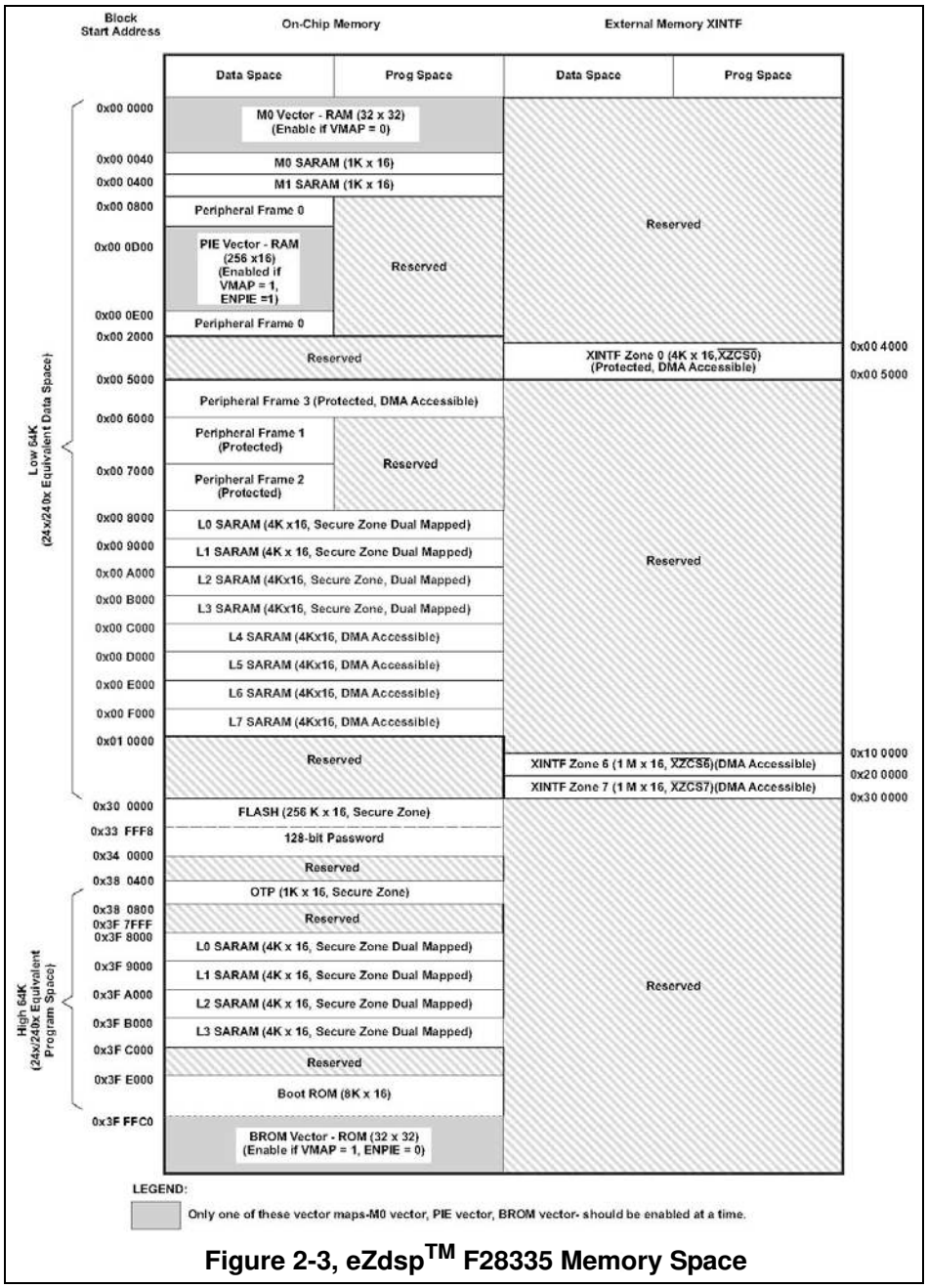

Figure 2-3, eZdsp™ F28335 Memory Space

Note: The on-chip flash memory has a security key which can prevent visibility when enabled.

2.3 eZdsp™ F28335 Connectors

The eZdsp™ F28335 has fourteen connectors. The function of each connector is shown in the table below:

Table 2: eZdsp™ F28335 Connectors

Connector	Function
P1	JTAG Interface
P2	Expansion
P4/P8/P7	I/O Interface
P5/P9	Analog Interface
P6	Power Connector
P10	Expansion
P11	CAN-A
P12	SCI-A
J11	CAN-B
J12	SCI-B
J201	Embedded JTAG

2.3.1 P1, JTAG Interface

The eZdsp™ F28335 is supplied with a 14-pin header interface, P1. This is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs.

The positions of the 14 pins on the P1 connector are shown in the diagram below as viewed from the top of the eZdsp.

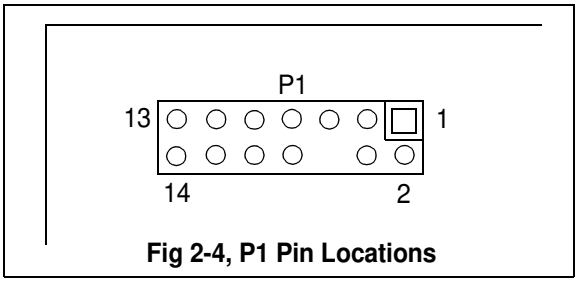

Fig 2-4, P1 Pin Locations

The definition of P1, which has the JTAG signals is shown below.

Table 3: P1, JTAG Interface Connector

Pin #	Signal	Pin #	Signal
1	XTMS	2	XTRST-
3	XTDI	4	GND
5	XTPD (+3.3/5V)	6	**no pin**
7	T_TDO	8	USBSEL
9	T_TCK RET	10	GND
11	XTCK	12	GND
13	T_EMU0	14	T_EMU1

WARNING !

The TMS320F28335 supports +3.3V Input/Output levels which are NOT +5V tolerant. Connecting the eZdsp to a system with +5V Input/Output levels will damage the TMS320F28335. If the eZdsp is connected to another target then the eZdsp must be powered up first and powered down last to prevent lactchup conditions.

2.3.2 P2, Expansion Interface

The positions of the 60 pins on the P2 connector are shown in the figure below.

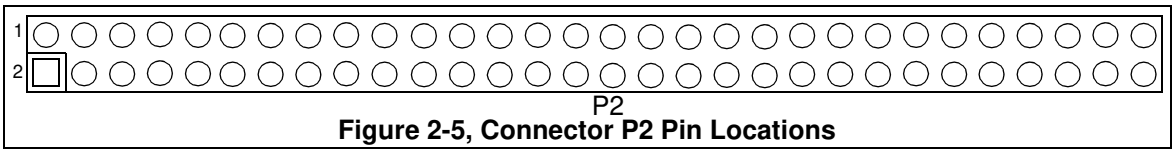

Figure 2-5, Connector P2 Pin Locations

The definition of P2, which has the I/O signal interface is shown below.

Table 4: P2, Expansion Interface Connector

Pin #	Signal	Pin #	Signal
1	+3.3V/+5V/NC *	2	+3.3/+5V/NC *
3	GPIO79_XD0	4	GPIO78_XD1
5	GPIO77_XD2	6	GPIO76_XD3
7	GPIO75_XD4	8	GPIO74_XD5
9	GPIO73_XD6	10	GPIO72_XD7
11	GPIO71_XD8	12	GPIO70_XD9
13	GPIO69_XD10	14	GPIO68_XD11
15	GPIO67_XD12	16	GPIO66_XD13
17	GPIO65_XD14	18	GPIO64_XD15
19	GPIO40_XA0_XWE1n	20	GPIO41_XA1
21	GPIO42_XA2	22	GPIO43_XA3
23	GPIO44_XA4	24	GPIO45_XA5
25	GPIO46_XA6	26	GPIO47_XA7
27	GPIO80_XA8	28	GPIO81_XA9
29	GPIO82_XA10	30	GPIO83_XA11
31	GPIO84_XA12	32	GPIO85_XA13
33	GPIO86_XA14	34	GPIO87_XA15
35	GND	36	GND
37	GPIO36_SCIRXDA-XZCS0n	38	GPIO37_ECAP2_XZCS7n
39	GPIO34_ECAP1_XREADY	40	B_GPIO28_SCIRXDA_XZCS6n
41	GPIO35_SCIRXDA_XRNW	42	10K Pull-up
43	GPIO38_WE0n	44	XRDn
45	+3.3V	46	No connect
47	DSP_RSn	48	XCLKOUT
49	GND	50	GND
51	GND	52	GND
53	GPIO39_XA16	54	GPIO31_CANTXA_XA17
55	GPIO30_CANRXA_XA18	56	GPIO14_TZ3n_XHOLDn_SCITXB_MCLKXB
57	GPIO15_XHOLDAn_SCIRXDB_MFSXB	58	GPIO29_SCITXDA_XA19
59	No connect	60	No connect

* Default is No Connect (NC). User can jumper to +3.3V or +5V on backside of eZdsp with JR5.

2.3.3 P4/P8/P7, I/O Interface

The connectors P4, P8, and P7 present the I/O signals from the DSC. The layout of these connectors are shown below.

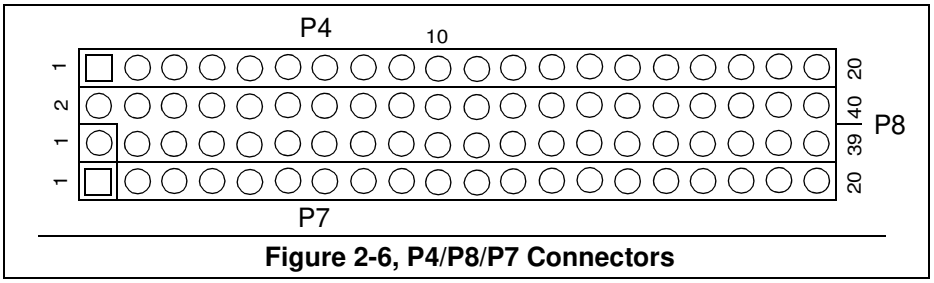

Figure 2-6, P4/P8/P7 Connectors

The pin definition of the P4 connector is shown in the table below.

Table 5: P4, I/O Connectors

Pin #	Signal
1	+3.3V/+5V/NC *
2	No connect
3	GPIO22_EQEP1S_MCLKRA_SCITXDB
4	GPIO7_EPWM4B_MCLKRA_ECAP2
5	GPIO23_EQEP1_MFSXA_SCIRXDB
6	GPIO5_EPWM3B_MFSRA_ECAP1
7	GPIO20_EAEP1A_MXDA_CANTXB
8	GPIO21_EQEP1B_MDRA_CANRXB
9	No connect
10	GND
11	GPIO3_EPWM2B_ECAP5_MCLKRB
12	GPIO1_EPWM1B/ECAP6/MFSRB
13	No connect
14	No connect
15	No connect
16	No connect
17	No connect
18	GPIO14_TZ3n_XHOLD_SCITXDB_MCLKXB
19	GPIO15_TZ4n_XHOLDA_SCIRXDB_MFSXB
20	GND

The pin definition of the P8 connector is shown in the table below.

Table 6: P8, I/O Connectors

Pin #	Signal	Pin #	Signal
1	+3.3V/+5V/NC *	2	+3.3V/+5V/NC *
3	MUX_GPIO29_SCITXDA_XA19	4	MUX_GPIO28_SCIRXDA_XZCS6n
5	GPIO14_TZ3n_XHOLD_SCITXDB_MCLKXB	6	GPIO20_EAEP1A_MXDA_CANTXB
7	GPIO21_EQEP18_MDRA_CANRXB	8	GPIO23_EQEP1_MFSXA_SCIRXDB
9	GPIO0_EPWM1A	10	GPIO1_EPWM1B/ECAP6/MFSRB
11	GPIO2_EPWM2A	12	GPIO3_EPWM2B_ECAP5_MCLKRB
13	GPIO4_EPWM3A	14	GPIO5_EPWM3B_MFSRA_ECAP1
15	GPIO27_ECAP4_EQEP2S_MFSXB	16	GPIO6_EPWMN4A_EPWMSYNCI/EPWMSYNCO
17	GPIO13_TZ2N_CANRXB_MDRB	18	GPIO34_ECAP1_XREADY
19	GND	20	GND
21	GPIO7_EPWM4B_MCLKRA_ECAP2	22	GPIO15TZ4n_XHOLDA_SCIRXDB_MFSXB
23	GPIO16_SPISIMOA_CANTXB_TZ5n	24	GPIO17_SPISOMIA_CANRXB_TZ6n
25	GPIO18_SPICLKA_SCITXDB_CANRXA	26	GPIO19_SPISTAn_SCIRXDB_CANTXA
27	_MUX_GPIO31_CANRXA_XA17	28	MUX_GPIO30_CANRXA_XA18
29	MUX_GPIO11_EPWM6B_SCIRXDB_ECAP4	30	MUX_GPIO8EPWM5A_CANTXB_ADCSOCA0nP3
31	MUX_GPIO9_EPWM5B_SCITXDB_ECAP3	32	MUX_GPIO10_EPWM6A_CANRXB_ADCASOCB0n
33	MUX_GPIO22	34	GPIO25_ECAP2_EPEQ2B_MDRB
35	GPIO26_ECAP3_EQEP21_MCLKXB	36	GPIO32_SDAA_EPWMSYNCI_ADCSOCAOn
37	GPIO12_TZ1N_CANTXB_MDXB	38	GPIO33_SCLA_EPWNSYNCVO_ADCSOCBOn
39	GND	40	GND

* Default is No Connect (NC). User can jumper to +3.3V or +5V on backside of eZdsp with JR4.

The P7 connector is supplied for backwards compatibility. Signals from other connectors can be wired to this connector to support existing user interfaces. The pin definition of P7 connector is shown in the table below.

Table 7: P7, I/O Connector

Pin #	Signal	Pin #	Signal
1	No connect	11	No connect
2	No connect	12	No connect
3	No connect	13	No connect
4	No connect	14	No connect
5	No connect	15	No connect
6	No connect	16	No connect
7	No connect	17	No connect
8	No connect	18	No connect
9	No connect	19	No connect
10	No connect	20	GND