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78M6610+LMU
Energy Measurement Processor for Load Monitoring Units

DATA SHEET

GENERAL DESCRIPTION

The 78M6610+LMU is an energy measurement processor (EMP) for load monitoring and control of any 2-wire single-phase or 3-wire split-phase (120/180°) AC circuit. It provides flexible sensor configuration of four analog inputs and numerous host interface options for easy integration into any system architecture.

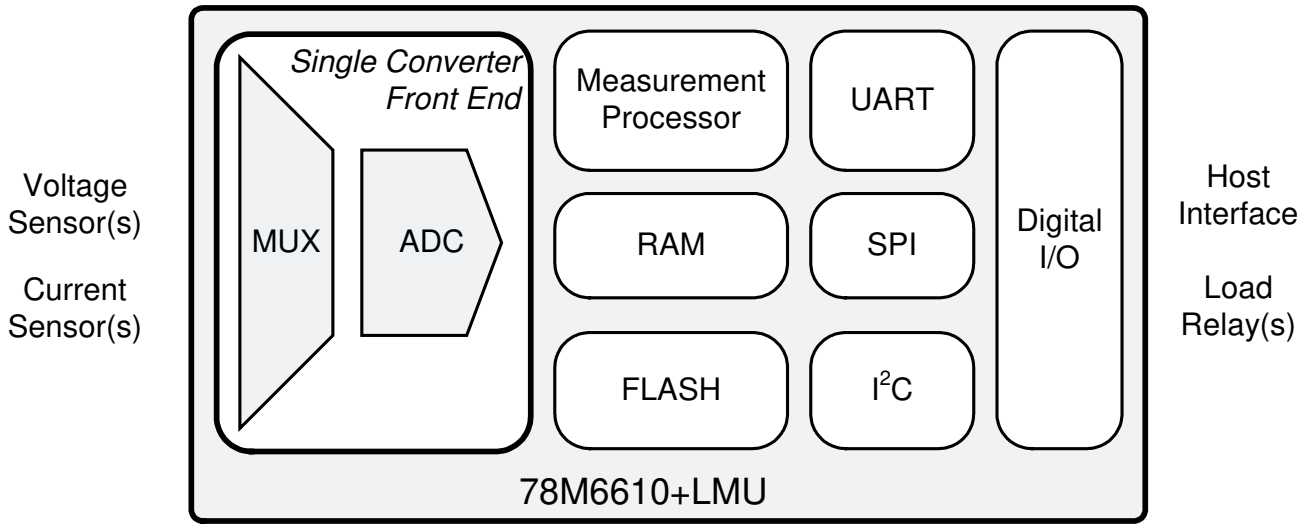
The internal 24-bit processor and field upgradeable firmware performs all the necessary signal processing, compensation, and data formatting for accurate real-time measurement. Energy accumulation, alarm monitoring, and fault detection schemes minimize the overhead requirements of the host interface and/or network. The integrated flash memory also provides for nonvolatile storage of input configurations and calibration coefficients.

APPLICATIONS

- Building Automation Systems (Commercial, Industrial)
- Inverters and Renewable Energy Systems
- Level 1 and 2 EV Charging Systems
- Grid-Friendly Appliances and Smart Plugs

FEATURES

- Four Configurable Analog Inputs for Monitoring Any Single-Phase Circuit (2/3-Wire)
- Supports Current Transformers (CT) and Resistive Shunts
- Flexible SPI, I^2C, or UART Interface Options with Configurable I/O Pins for Alarm Signaling, Address Pins, or User Control
- Nonvolatile Storage of Calibration and Configuration Parameters
- Small 24-TQFN Package and Reduced Bill of Materials
- Internal or External Oscillator Timing References
- Quick Calibration Routines Minimize Manufacturing (System) Cost



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Electrical Specifications

ABSOLUTE MAXIMUM RATINGS

(All voltages with respect to ground.)

Supplies and Ground Pins:	
V_{3P3D}, V_{3P3A}	-0.5V to +4.6V
GNDD, GNDA	-0.5V to +0.5V
Analog Input Pins:	
A0, A1, A2, A3, A4, A5	-10mA to +10mA -0.5V to (V_{3P3} + 0.5V)
Oscillator Pins:	
XIN, XOUT	-10mA to +10mA -0.5V to +3.0V
Digital Pins:	
IFC0, IFC1, SSB/DIR/SCL, SDO/TX/SDAO, SDI/RX/SDAI, $\overline{\text{RESET}}$, SCK/ADDR0, MP10, MP0, MP4, MP6/ADDR1, MP7	-30mA to +30mA, -0.5V to (V_{3P3D} + 0.5V)
Digital Pins Configured as Inputs	-10mA to +10mA, -0.5V to +6V
Temperatures:	
Operating Junction Temperature)	
Peak, 100ms	+140°C
Continuous	+125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+260°C
Soldering Temperature (reflow)	+300°C
ESD Stress on All Pins	±4kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended External Components

NAME	FROM	TO	FUNCTION	VALUE	UNITS
XTAL	XIN	XOUT	20.000MHz	20.000	MHz
CXS	XIN	GNDD	Load capacitor for crystal (exact value depends on crystal specifications and parasitic capacitance of board)	18 ±10%	pF
CXL	XOUT	GNDD		18 ±10%	pF

Recommended Operating Conditions

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
3.3V Supply Voltage (V_{3P3})	Normal operation	3.0	3.3	3.6	V
Operating Temperature		-40		+85	°C

Performance Specifications

Note that production tests are performed at room temperature.

Input Logic Levels

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Digital High-Level Input Voltage (V_{IH})		2			V
Digital Low-Level Input Voltage (V_{IL})				0.8	V

Output Logic Levels

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Digital High-Level Output Voltage (V_{OH})	I_{LOAD} = 1mA	V_{3P3} - 0.4			V
	I_{LOAD} = 10mA	V_{3P3} - 0.6			V
Digital Low-Level Output Voltage (V_{OL})	I_{LOAD} = 1mA	0		0.4	V
	I_{LOAD} = 10mA			0.5	V

Supply Current

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{3P3D} and V_{3P3A} Current (Compounded)	Normal operation, V_{3P3} = 3.3V		8.1	10.3	mA

Crystal Oscillator

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
XIN to XOUT Capacitance	(Note 1)		3		pF
Capacitance to GNDD (Note 1)	XIN		5		pF
	XOUT		5		

Note 1: Guaranteed by design; not subject to test.

Internal RC Oscillator

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Nominal Frequency			20.000		MHz
Accuracy	V_{3P3} = 3.0V, 3.6V; temperature = -40°C to +85°**C**		±1.5	±1.75	%

ADC Converter, V_{3P3} Referenced

LSB values do not include the 9-bit left shift at EMP input.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Usable Input Range (V_{IN} - V_{3P3})		-250		+250	mV peak
THD (First 10 Harmonics)	V_{IN} = 65Hz, 64kpts FFT, Blackman-Harris window		-85		dB
Input Impedance	V_{IN} = 65Hz	30		90	kΩ
Temperature Coefficient of Input Impedance	V_{IN} = 65Hz (Note 1)		1.7		Ω/°C
ADC Gain Error vs. %Power Supply Variation $\frac{10^6 \Delta Nout_{PK}\, 357nV/V_{IN}}{100 \Delta V3P3A/3.3}$	V_{IN} = 200mVpk, 65Hz; V_{3P3} = 3.0V, 3.6V			50	ppm/%
Input Offset (V_{IN} - V_{3P3})		-10		+10	mV

[1] Guaranteed by design; not subject to test.

Timing Specifications

Reset

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reset Pulse Fall Time	(Note 1)		1		µs
Reset Pulse Width	(Note 1)		5		µs

SPI Slave Port

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SCK Cycle Time (t_{SPIcyc})		1			µs
Enable Lead Time ($t_{SPILead}$)		15			ns
Enable Lag Time (t_{SPILag})		0			ns
SCK Pulse Width (t_{SPIW})	High	250			ns
	Low	250			
SSB to First SCK Fall (t_{SPISCK})	Ignore if SCK is low when SSB falls (Note 1)		2		ns
Disable Time (t_{SPIDIS})	(Note 1)		0		ns
SCK to Data Out (SDO) (t_{SPIEV})				25	ns
Data Input Setup Time (SDI) (t_{SPISU})		10			ns
Data Input Hold Time (SDI) (t_{SPIH})		5			ns

Note 1: Guaranteed by design, not subject to test.

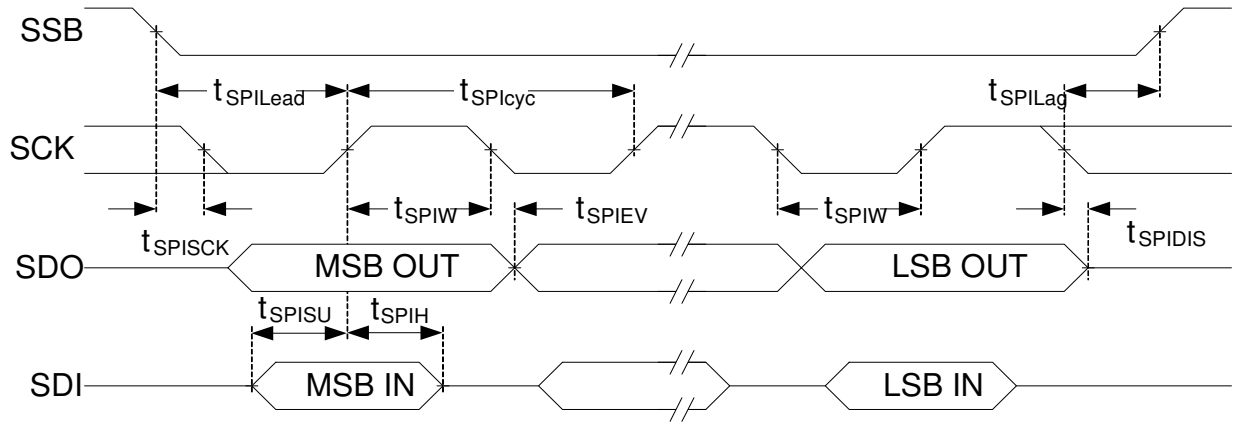


Figure 1. SPI Timing

I²C Slave Port (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Bus Idle (Free) Time Between Transmissions (STOP/START) (t_{BUF})		1500			ns
I²C Input Fall Time (t_{ICF})	(Note 2)	20		300	ns
I²C Input Rise Time (t_{ICR})	(Note 2)	20		300	ns
I²C START or Repeated START Condition Hold Time (t_{STH})		500			ns
I²C START or Repeated START Condition Setup Time (t_{STS})		600			ns
I²C Clock High Time (t_{SCH})		600			ns
I²C Clock Low Time (t_{SCL})		1300			ns
I²C Serial Data Setup Time (t_{SDS})		100			ns
I²C Serial Data Hold Time (t_{SDH})		10			ns
I²C Valid Data Time (t_{VDA}): SCL Low to SDA Output Valid ACK Signal from SCL Low to SDA (Out) Low				900	ns

Note 1: Guaranteed by design, not subject to test

Note 2: Dependent on bus capacitance.

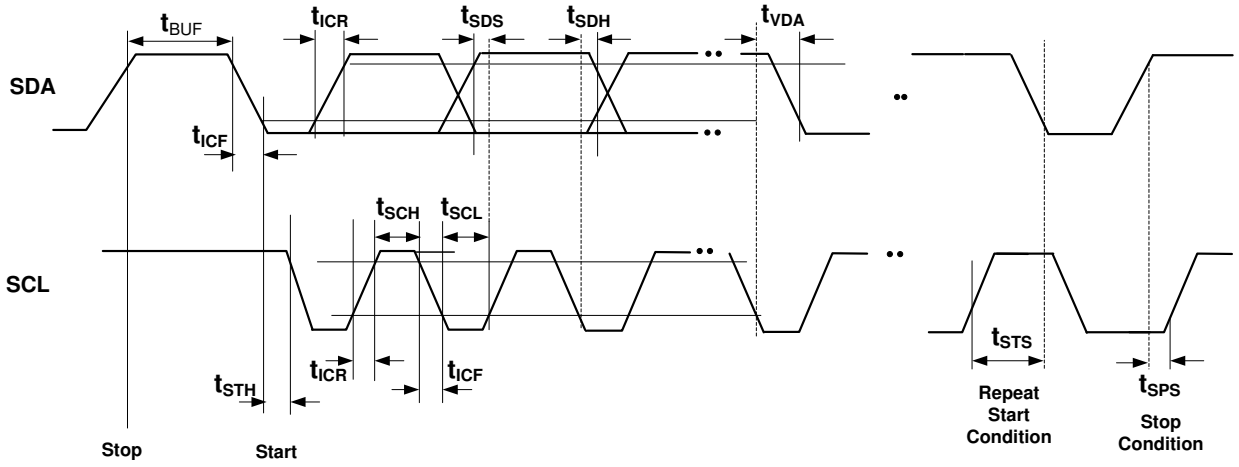


Figure 2. I²C Timing

Pin Configuration

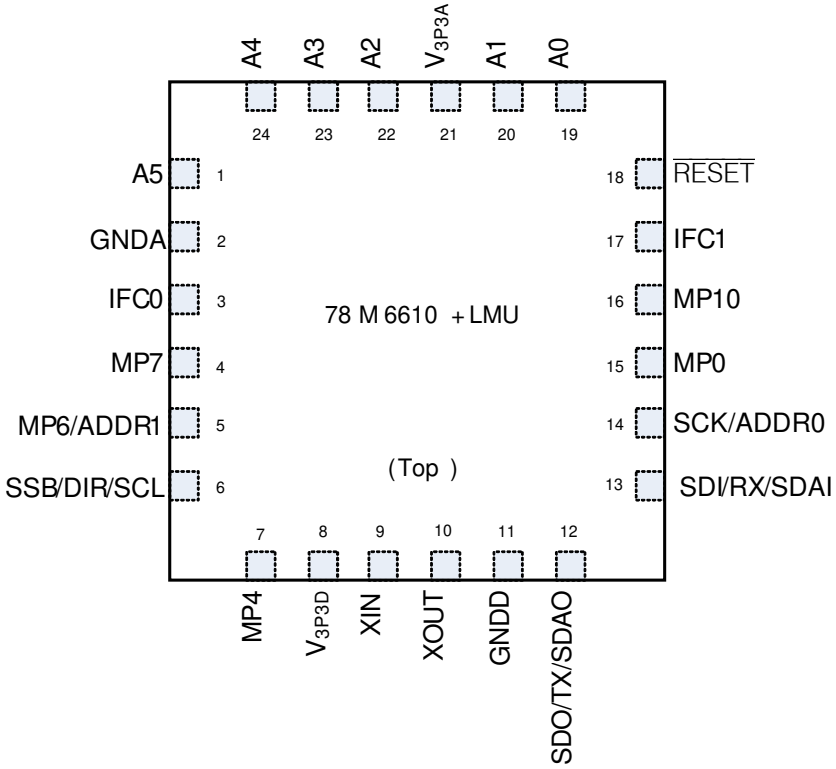


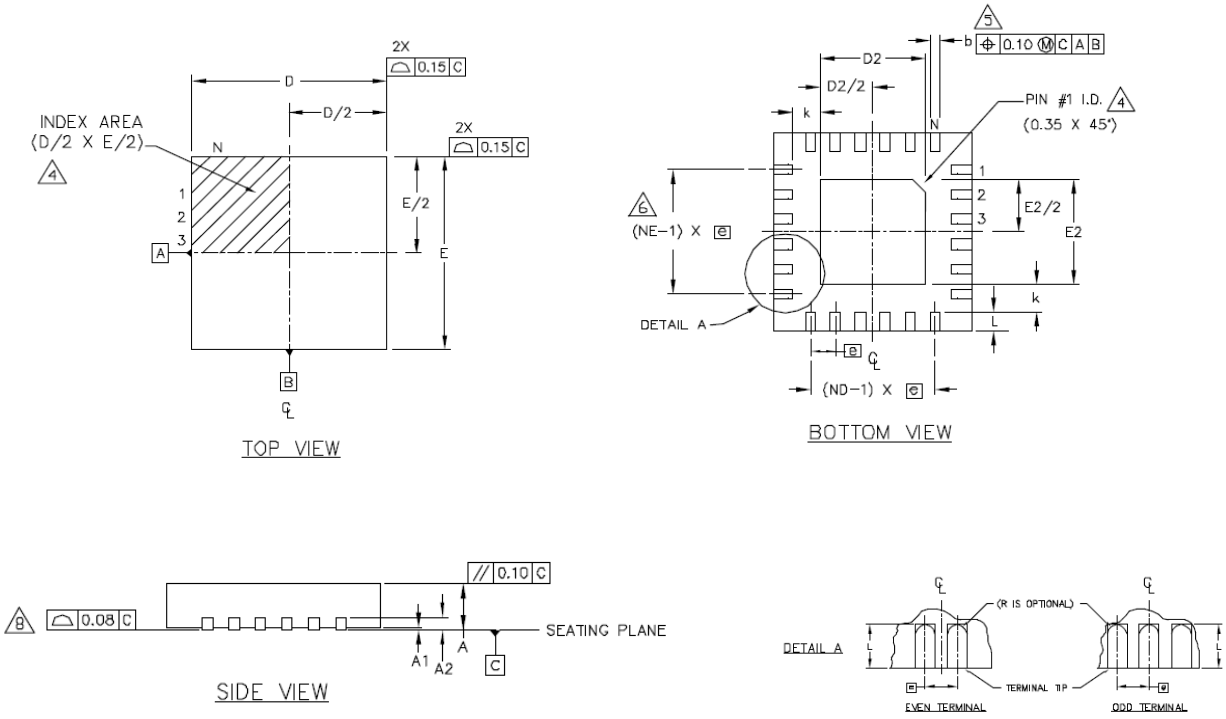
Figure 3. QFN Package Pinout

PIN	SIGNAL	FUNCTION	PIN	SIGNAL	FUNCTION
1	A5	Analog Input (Negative)	13	SDI/RX/ SDAI	SPI DATA IN/UART RX/ I^2C Data In
2	GNDA	Ground (Analog)	14	SCK/ ADDR0	SPI CLOCK/MPIO
3	IFC0	IFC1/SPI (1 = IFC1; 0 = SPI)	15	MP0	Multipurpose Digital I/O
4	MP7	Multipurpose Digital I/O	16	MP10	Multipurpose Digital I/O
5	MP6/ADDR1	Multipurpose Digital I/O	17	IFC1	I^2C/UART (1 = I^2C;0 = UART)
6	SSB/DIR/ SCL	Slave Select (SPI)/RS-485 TX-RX/ I^2C Serial Clock	18		Active-Low Reset Input
7	MP4	Multipurpose Digital I/O	19	A0	Analog Input
8	V_{3P3D}	3.3V DC Supply (Digital)	20	A1	Analog Input
9	XIN	Crystal Oscillator Driver Input	21	V_{3P3A}	3.3V DC Supply (Analog)
10	XOUT	Crystal Oscillator Driver Output	22	A2	Analog Input (Positive)
11	GNDD	Ground (Digital)	23	A3	Analog Input (Negative)
12	SDO/TX/ SDAO	SPI DATA OUT/UART TX/ I^2C Data Out	24	A4	Analog Input (Positive)

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TQFN	T2444+4	21-0139	90-0022



PKG	24L 4x4		
REF.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.0	0.02	0.05
A2	0.20 REF		
b	0.18	0.23	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e	0.50 BSC.		
k	0.25	-	-
L	0.30	0.40	0.50
N	24		
ND	6		
NE	6		
Jedec Var.	WGGD-2		

Figure 4. Package Outline

On-Chip Resources Overview

The 78M6610+LMU device integrates all the hardware blocks required for accurate AC power and energy measurement. Included on device are:

- Oscillator circuits and clock management logic
- Power-on reset, watchdog timer, and reset circuitry
- High-accuracy analog front-end (AFE) with trimmed voltage reference and temperature sensor
- 24-bit energy measurement processor (EMP) with RAM and flash memory
- Serial UART, SPI, I^2C interfaces and multipurpose digital I/O

IC Block Diagram

The following is a block diagram of the hardware resources available on the 78M6610+LMU.

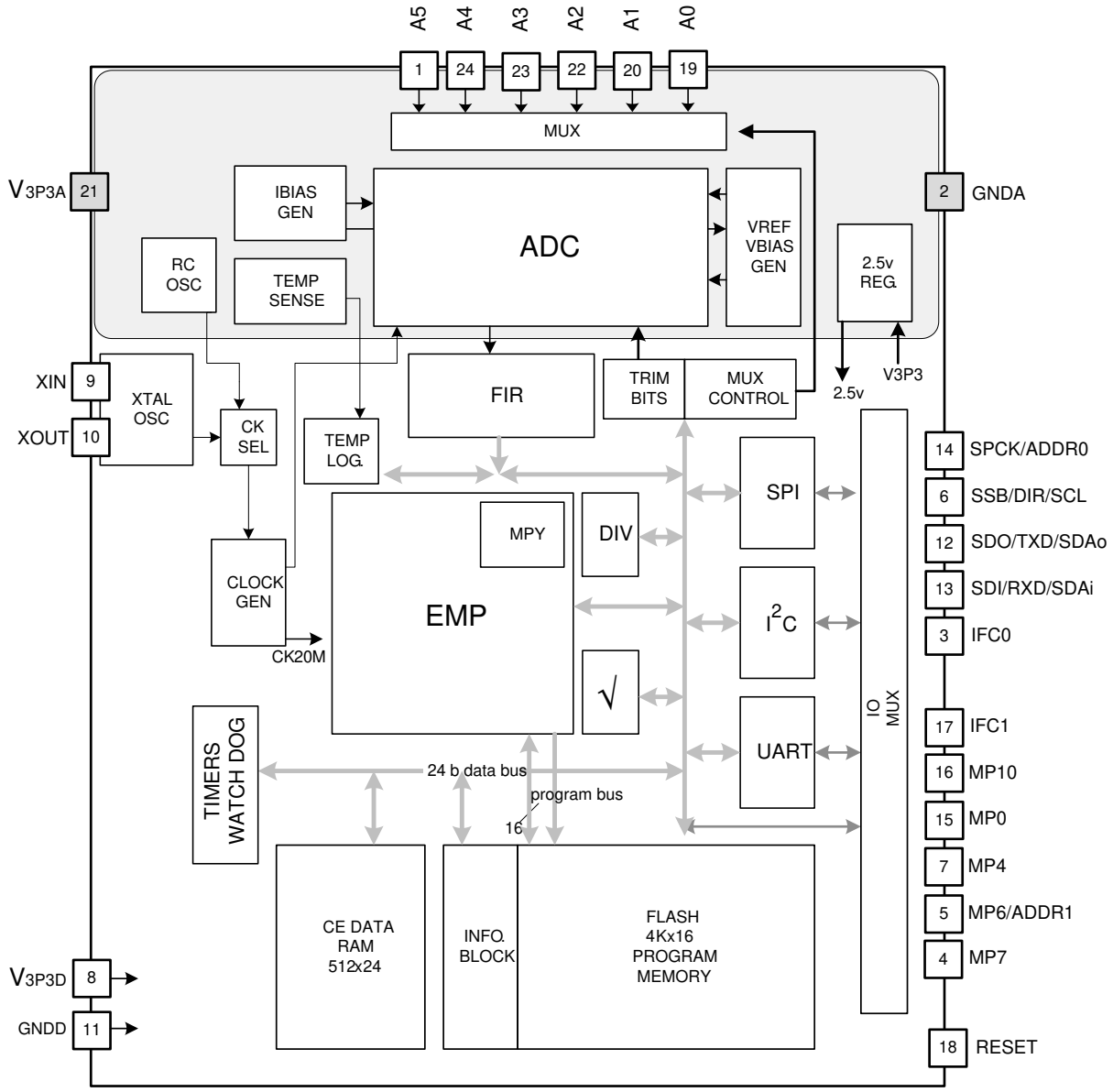


Figure 5. Block Diagram

Clock Management

The device can be clocked by either a trimmed internal RC oscillator or by oscillator circuitry that relies on an external crystal. The internal RC oscillator provides an accurate clock source for UART baud rate generation. Only time based calculations such as line frequency and watt-hour (energy) are affected by clock accuracy.

The chip hardware automatically handles the clock sources logic and distributes the clock to the rest of the device. Upon reset or power-on, the device will utilize the internal RC oscillator circuit for the first 1024 clock cycles, allowing the external crystal adequate time to start-up. The device will then automatically select the external clock, if available. It will also automatically switch back to the internal oscillator in the event of a failure with the external oscillator. This condition is also monitored by the processor and available to the user in the STATUS register.

The 78M6610+LMU external clock circuitry requires a 20.000MHz crystal. The circuitry includes two 18pF ceramic capacitors. The figure below shows the typical connection of the external crystal. This oscillator is self biasing and therefore an external resistor should NOT be connected across the crystal.

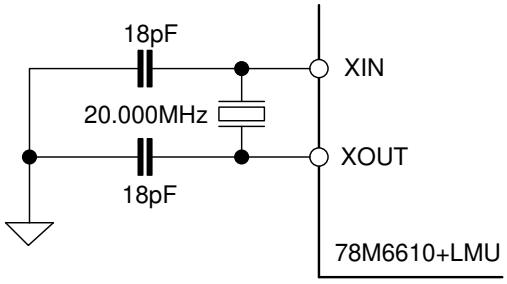


Figure 6. Crystal Connections

An external 20MHz system clock signal can also be utilized instead of the crystal. In this case, the external clock should be connected to the XOUT pin while the XIN pin should be connected to GNDD.

Alternatively, if no external crystal or clock is utilized, the XOUT pin should be connected to GNDD and the XIN pin left unconnected.

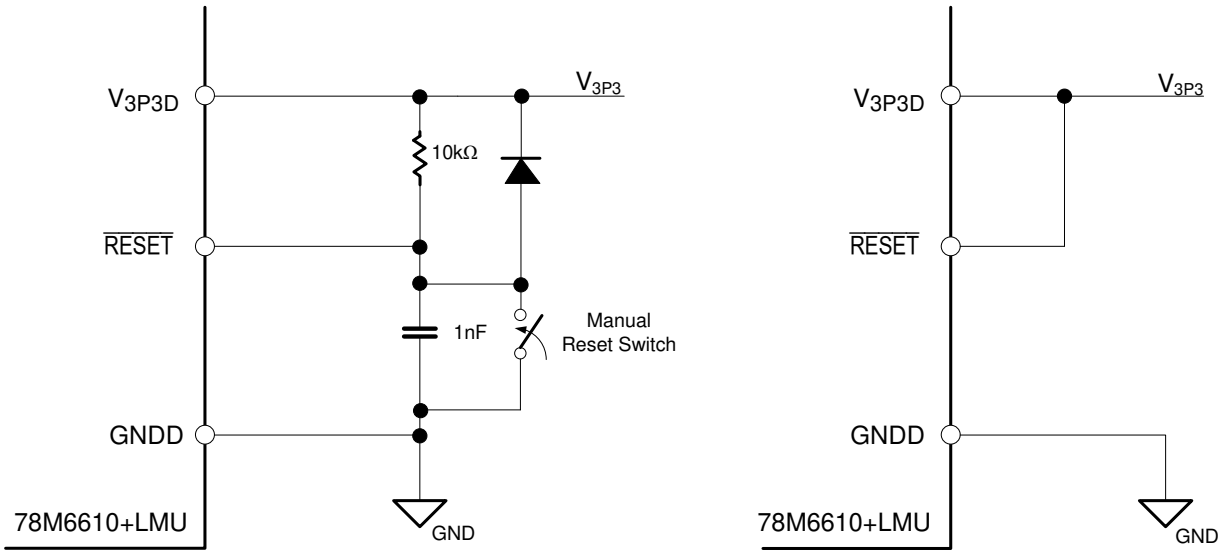
Power-On and Reset Circuitry

An on-chip power-on reset (POR) block monitors the supply voltage (V_{3P3D}) and initializes the internal digital circuitry at power-on. Once V_{3P3D} is above the minimum operating threshold, the POR circuit triggers and initiates a reset sequence. It will also issue a reset to the digital circuitry if the supply voltage falls below the minimum operating level.

In addition to the internal sources, a reset can be forced by applying a low level to the $\overline{\text{RESET}}$ pin. If the $\overline{\text{RESET}}$ pin is pulled low, all digital activities in the device stop, except the clock management circuitry and oscillators, which continue to run. The external reset input is filtered to prevent spurious reset events in noisy environments. The reset does not occur until $\overline{\text{RESET}}$ has been held low for at least 1µs.

Once initiated, the reset mode persists until the $\overline{\text{RESET}}$ is set high and the reset timer times out (4096 clock cycles). At the completion of the reset sequence, the internal reset is released and the processor (EMP) begins executing from address 0.

If not used, the $\overline{\text{RESET}}$ pin can be connected either directly or through a pullup resistor to V_{3P3D} supply. A simple connection diagram is shown below.



a) External $\overline{\text{RESET}}$ Connection Example

b) Unused $\overline{\text{RESET}}$ Connection Example

Figure 7. Reset Connections

Watchdog Timer

A Watchdog Timer (WDT) block detects any software processing errors. The software periodically refreshes the free-running watchdog timer to prevent it from timing out. If the WDT times out, it is an indication that software is no longer being executed in the intended sequence; thus, a system reset is initiated.

Analog Front-End and Conversion

The Analog Front-End (AFE) includes an input multiplexer, optional pre-amplifier gain stage, Delta-Sigma A/D Converter, bias current references, voltage references, temperature sensor, and several voltage fault comparators.

Analog Inputs

Up to four external sensors can be connected to the 78M6610+LMU. Two single-ended inputs are available for voltage sensors and two differential pairs are available for connecting current sensors. Although the current inputs are differential inputs, a common-mode voltage of less than V_{3P3A} ±25 mV is recommended in order to utilize the available dynamic range. The full-scale signal level that can be applied to the analog input pins is V_{3P3A} ±250mVpk. Considering a sinusoidal AC waveform, the maximum RMS voltage applied to the inputs pins is:

$$\text{rmsMAX} = \frac{250mVpk}{\sqrt{2}} = 176.78\text{mVrms}$$

Delta-Sigma A/D Converter

A second-order Delta-Sigma converter digitizes the analog inputs. The converted data is then processed through a FIR filter.

Voltage Reference

The device includes an on-chip precision bandgap voltage reference that incorporates auto-zero techniques as well as production trims to minimize errors caused by component mismatch and drift. The voltage reference is digitally compensated over temperature.

Die Temperature Measurement

The device includes an on-chip die temperature sensor used for digital compensation of the voltage reference. It is also used to report temperature information to the user.

24-Bit Energy Measurement Processor (EMP)

The 78M6610+LMU integrates a dedicated 24-bit signal processor that performs the entire digital signal processing necessary for energy measurement, alarm generation, calibration, compensation, etc. Refer to Section 2 for a description of functionality and operations.

Flash and RAM

The 78M6610+LMU includes 8KB of on-chip flash memory. The flash memory primarily contains program code, but also stores calibration data and defaults for select nonvolatile configuration registers. The device also includes 1.5KB of on-chip RAM which contains the values of input and output registers and is utilized by the processor for its operations.

Multipurpose DIOs

There are a total of eleven digital input/outputs (DIOs) on the 78M6610+LMU device. Some are dedicated to serial interface communications and configuration. Others are multipurpose I/O that can be used as a simple output under user control or routed to special purpose internal signals like alarm signaling and relay control.

Communication Interface

The 78M6610+LMU includes three communication interfaces: UART, SPI, and I^2C. Since the I/O pins are shared, only one mode is supported at a time. Interface configuration and address pins are sampled at power-on or reset to determine which interface will be active and to set device addresses.

Functional Description and Operation

This section describes the operation and configuration of the 78M6610+LMU. It includes the flow of measurement data, relevant calculations, alarm monitoring, I/O control, and user configurations.

Measurement Interface

The 78M6610+LMU incorporates a flexible measurement interface for simplified integration into any single-phase system. This section describes the configuration and signal conditioning of the analog inputs.

Settings and calibration parameters described in this section can be saved to flash memory and automatically initialized upon power on or reset.

AFE Input Multiplexer

The 78M6610+LMU samples four (4) external sensors with an effective sample rate of 4Ksps for each multiplexer slot. Two analog input pins are defined as single ended voltage inputs with the other four analog input pins defined as a pair of differential current inputs.

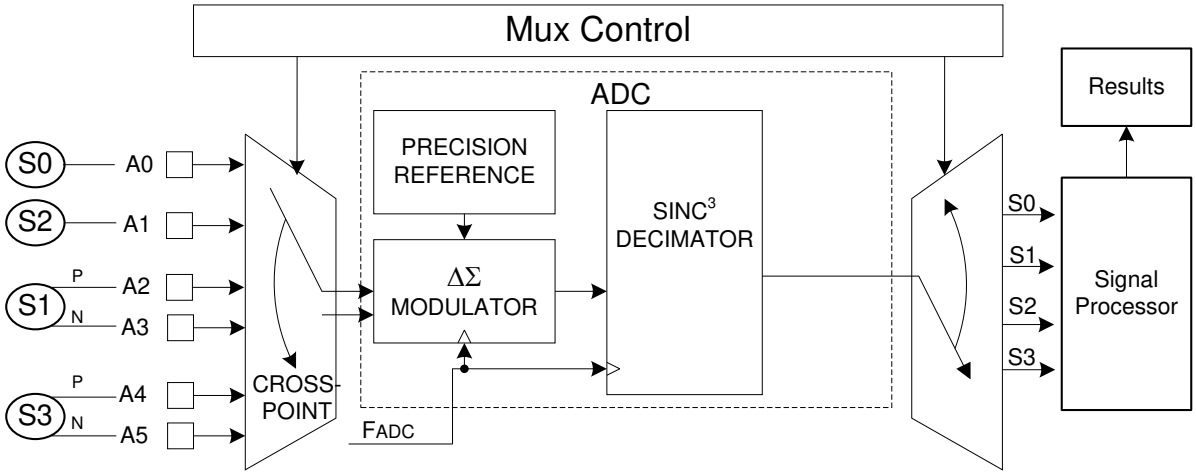


Figure 8. AFE Input Multiplexer

Sensor Slot	Analog Input Pins	Input Type
S0	A0	Voltage
S1	A2 (pos) and A3 (neg)	Current
S2	A1	Voltage
S3	A4 (pos) and A5 (neg)	Current

High Pass Filters and Offset Removal

Offset registers for each analog input contain values to be subtracted from the raw ADC outputs for the purpose of removing inherent system DC offsets from any calculated power and RMS values. These registers are signed fixed point numbers with a possible range of -1.0 to 1 - LSB. They default to 0 and can be manually changed by the user or integrated offset calibration routines.

Register	Description
S1_OFFS	Current Input S1 Offset Calibration
S0_OFFS	Voltage Input S0 Offset Calibration
S3_OFFS	Current Input S3 Offset Calibration
S2_OFFS	Voltage Input S2 Offset Calibration

Alternatively, the user can enable an integrated High Pass Filter (HPF) to dynamically update the offset registers every accumulation interval. During each accumulation interval (or low-rate cycle) the HPF calculates the median or DC average of each input. Adjustable coefficients determine what portion of the measured offset is combined with the previous offset value.

HPF_COEF_x registers contain signed fixed point numbers with a usable range of 0 to 1 - LSB (0.99999), negative values are not supported. By default, they are initialized to 0.5 (0x400000) meaning the new offset value will come from one-half of the measured offset and one-half will come from the previous offset value. Setting them to 1.0 (0x7FFFFF) causes the entire measured offset to be applied to the offset register enabling lump-sum offset removal. Setting them to zero disables any dynamic update of the offset registers by the HPF.

Register	Description
HPF_COEF_I	HPF coefficient for S1 and S3 current inputs
HPF_COEF_V	HPF coefficient for S0 and S2 voltage inputs

To allow the DC component of the load current to be included in the measurement (i.e. half-wave rectified current waveforms), the HPF_COEF_I coefficients must be set to zero.

Using the offset calibration routine will automatically set the filter coefficients to zero to disable the HPF.

Gain Correction

The system (sensors) and the 78M6610+LMU device inherently have gain errors that can be corrected by using the gain registers. These registers can be directly accessed and modified by an external processor or automatically updated by an integrated self calibration routine.

Input gain registers are signed fixed point numbers with the binary point to the left of bit 21. They are set to 1.0 by default and have a usable range of 0 to 4 - LSB, negative values are not supported. The gain equation for each input slot can be described as Sx = Sx * Sx_GAIN.

Register	Description
S0_GAIN	Voltage Input S0 Gain Calibration.
S1_GAIN	Current Input S1 Gain Calibration
S2_GAIN	Voltage Input S2 Gain Calibration.
S3_GAIN	Current Input S3 Gain Calibration

Die Temperature Compensation

The 78M6610+LMU has an on-chip temperature sensor that can be used by the signal processor for monitoring the voltage reference error and made available to the user in the TEMPC register.

Setting the Temperature Compensation (TC) bit in the Command Register allows the firmware to further adjust the system gain based on measured die temperature. Die Temperature Offset is typically calibrated by the user during the calibration stage. Die temperature gain is set to a factory default value for most applications, but can be adjusted by the user.

Register	Description
T_OFFS	Die Temperature Offset Calibration.
T_GAIN	Die Temperature Slope Calibration. Set by factory.

Voltage Reference Gain Adjustment

The on-chip precision bandgap voltage reference incorporates auto-zero techniques as well as production trims to minimize errors caused by component mismatch and drift. It can be assumed that the part is trimmed at 22°C to produce a uniform voltage reference gain at that temperature. The voltage reference is digitally compensated over changes in measured die temperature using a quadratic equation.

Phase Compensation

Phase compensation registers are used to compensate for phase errors or time delays between the voltage input source and respective current source that are introduced by the off-chip sensor circuit. The user configurable registers are signed fixed point numbers with the binary point to the left of bit 21. Values are in units of high rate (4kHz) sample delays so each integer unit of delay is 250µs with a total possible delay of ±4 samples (roughly ±20° at 60Hz).

Register	Description
PHASECOMP1	Phase (delay) compensation for S1 input current
PHASECOMP3	Phase (delay) compensation for S3 input current

Example:

To compensate a phase error of 277.77µs (or 6° at 60Hz) introduced by a current transformer (CT) it is necessary to enter the following:

$$Phase\ Compensation = \frac{Phase\ Error}{\frac{1}{Sample\ Rate}}$$

$$Phase\ Compensation = \frac{277E^{-6}}{\frac{1}{4000}} = 1.111$$

The value to be entered in the phase compensation register is therefore:

$$PComp = 1.111 * 2^{21} = 2330169 = \ 0\text{x}238\text{E}39$$

Voltage Input Configuration

The 78M6610+LMU supports multiple analog input configurations for determining the three potential voltage sources in a split-phase circuit. The device measures the voltage difference between any two references and uses this information to derive the voltages VA, VB, and VC as shown below.

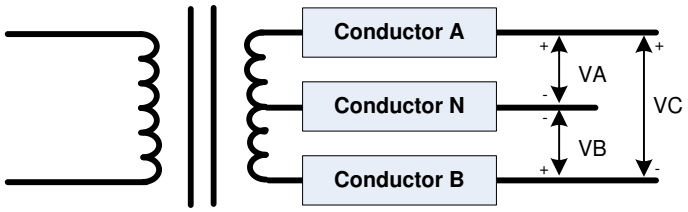


Figure 9. Voltage Input Configuration

Each calculated voltage source (VA, VB, and VC) is derived from the following user configurable function of the voltage input multiplexer slots (S0, S2) and three pairs of multiplier values (M0, M2). This function derives source voltages VA, VB, and VC by summing S0 x M0 and S2 x M2.

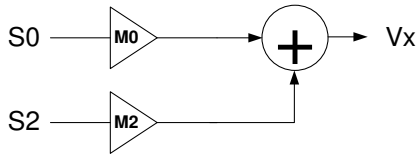


Figure 10. Voltage Computation

The user sets the multiplier values M0 and M2 for each voltage source in the CONFIG register using the model where a one (1) value adds the input, a two (2) value adds two of the input, a minus one (-1) value subtract the input, a zero (0) value does not include the input.

CONFIG Bits	19:18	17:16	15:14	13:12	11:10	9:8
Multiplier	M2	M0	M2	M0	M2	M0
Source	VC		VB		VA	

There are four choices for every M value as shown below.

Multiplier Bits	00	01	10	11
M (multiplier) Value	-1	0	1	2

The output registers VA, VB, and VC are automatically scaled by a factor of 0.5 if M0 and M2 are both nonzero.
For example, by setting the multiplier bits as follows:

$$Vc = +1 * S0 - 1 * S2$$

The effective content of the Vc register would result in:

$$Vc = \frac{(+1 * S0) + (-1 * S2)}{2}$$

This scaling is done to prevent the output register from overflowing.

Two example configurations are shown below. For determining the sign of S0 or S2 measurements, one should note that results for single ended inputs are referenced to V_{3P3}.

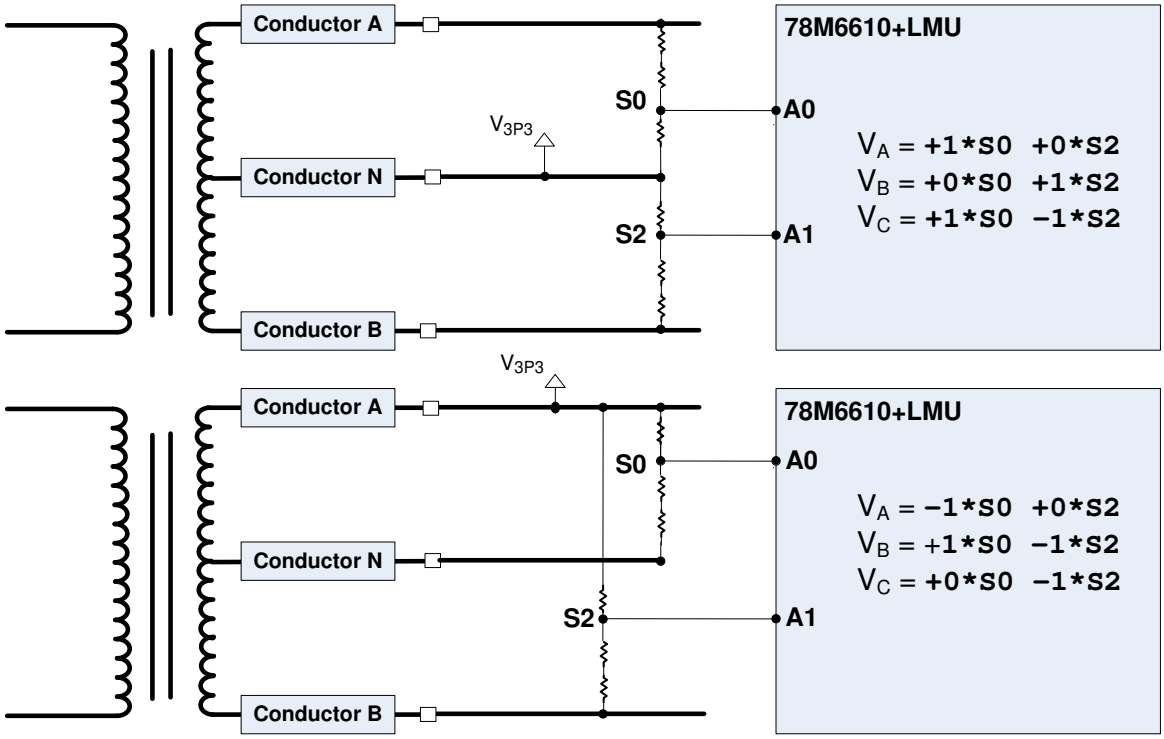


Figure 11. Example Voltage Configurations

Voltage Input Flowchart

The figure below illustrates the computational flowchart for VA, VB, and VC. The values for voltage input configuration register can be saved in flash memory and automatically restored at power-on or reset.

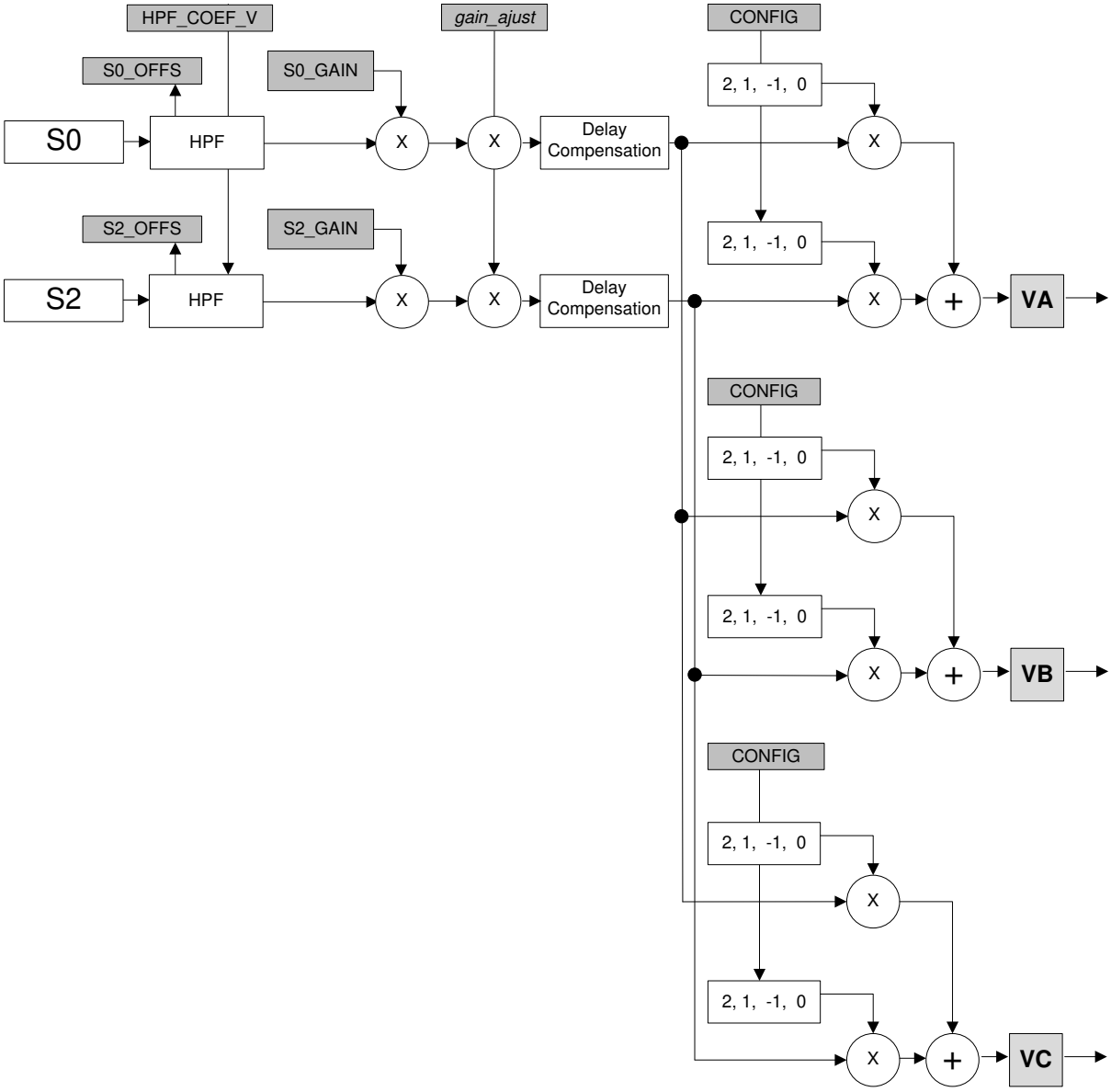


Figure 12. Voltage Input Flowchart

Current Input Configuration

The 78M6610+LMU supports multiple analog input configurations for determining the two load currents in a split-phase AC circuit. The device measures the current of any two conductors and uses this information to derive the load currents shown below.

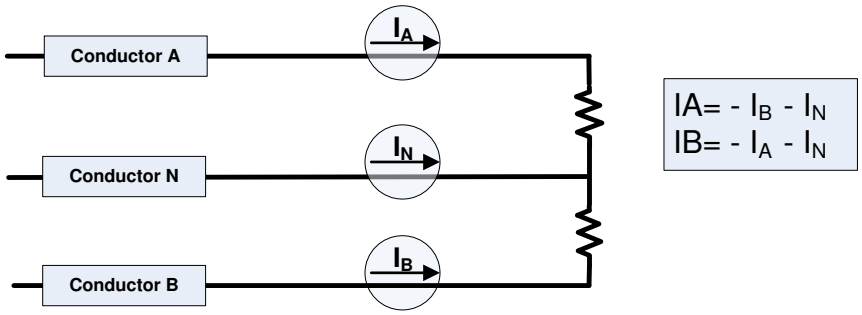


Figure 13. Current Input Configuration

Each calculated load current (IA and IB) is derived from the following function of the current input slots (S1 and S3) and 2 pairs of multiplier values (M1 and M3). This function derives source currents IA and IB by summing S1 x M1 and S3 x M3.

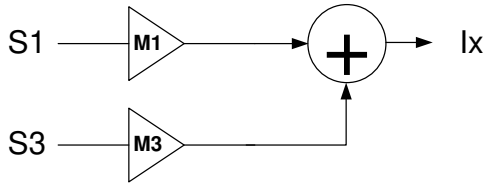


Figure 14. Current Computation

The user sets the multiplier values for each current source in the CONFIG register using the model where a one (1) value adds the input, a two (2) value adds two of the input, a minus one (-1) value subtract the input, a zero (0) value does not include the input.

CONFIG Bits	**7:6**	**5:4**	**3:2**	**1:0**
Multiplier	M3	M1	M3	M1
Source	IB		IA	

There are four choices for every M value as shown below.

Bit Values	**00**	**01**	**10**	**11**
M (multiplier) Value	-1	0	1	2

The output registers IA and IB are automatically scaled by a factor of 0.5 if M1 and M3 are both nonzero. For example, by setting the multiplier bits as follows:

$$IB = +1 * S1 - 1 * S3$$

The effective content of the Vc register would result in:

$$Vc = \frac{(+1 * S1) + (-1 * S3)}{2}$$

This scaling is done to prevent the output register from overflowing.

Current Configuration Examples

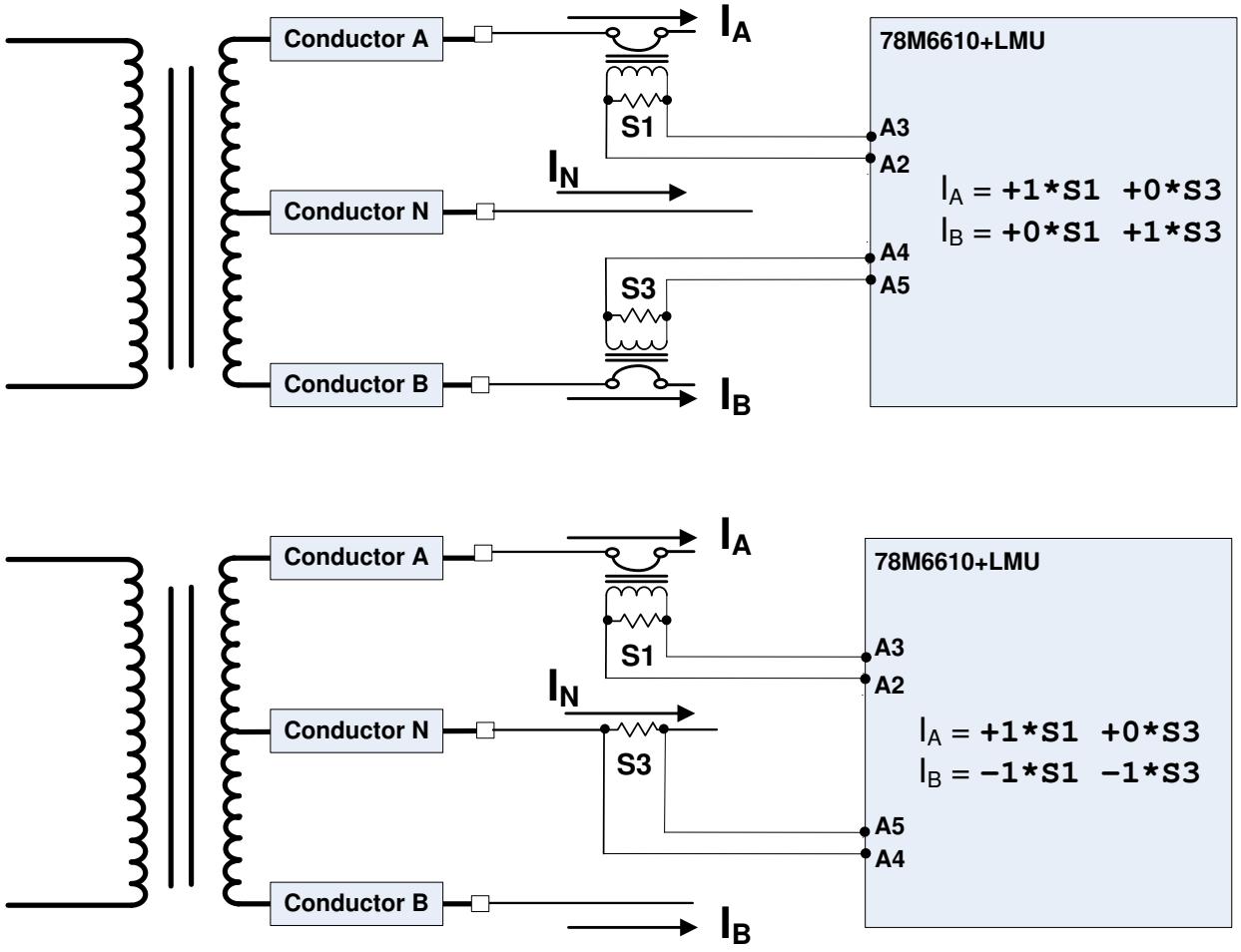


Figure 15. Current Configuration Examples

Pre-Amp

By default, the full-scale signal that can be applied to the current inputs is V_{3P3A} ±250mVpk (176.78mV_{RMS}). This setting provides the widest dynamic range and is recommended for most applications.

For applications requiring a much lower value shunt resistor, an optional pre-amplifier with an 8x gain is included for the current inputs. The maximum input signal applied to the current inputs in this case would be is V_{3P3A} ±31.25mVpk.

CONFIG[21:20]	00	01	10	11
8x Gain Enable	none	S1	S3	both

The gain is set by a ratio of internal resistors with one of the resistors in series from the input pad to the pre-amp itself. As such, the device must only be directly connected to a shunt with minimal resistance when using the pre-amp.

Current Input Flowchart

The figure below illustrates the computational flowchart for IA and IB. The values for current input configuration register can be saved in flash memory and automatically restored at power-on or reset.

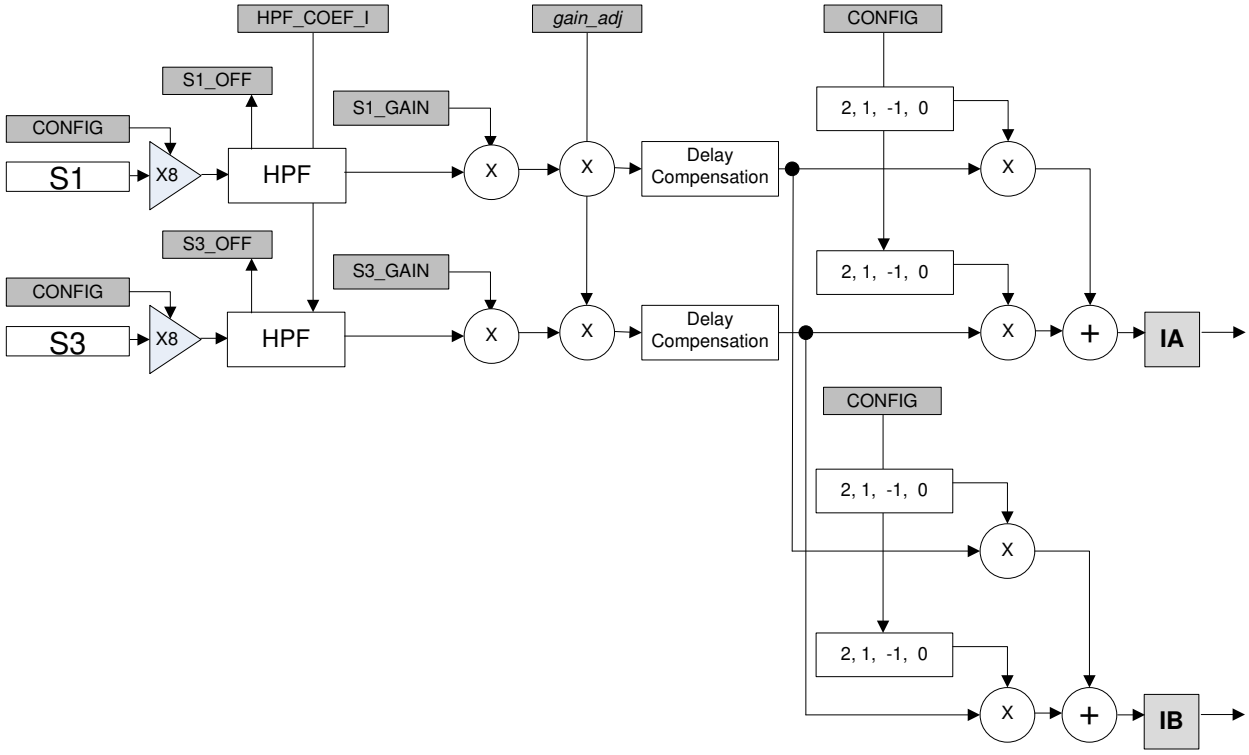


Figure 16. Current Input Flowchart