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78M6610+PSU

Energy Measurement Processor for Single-Phase Power-Supply Units

DESCRIPTION

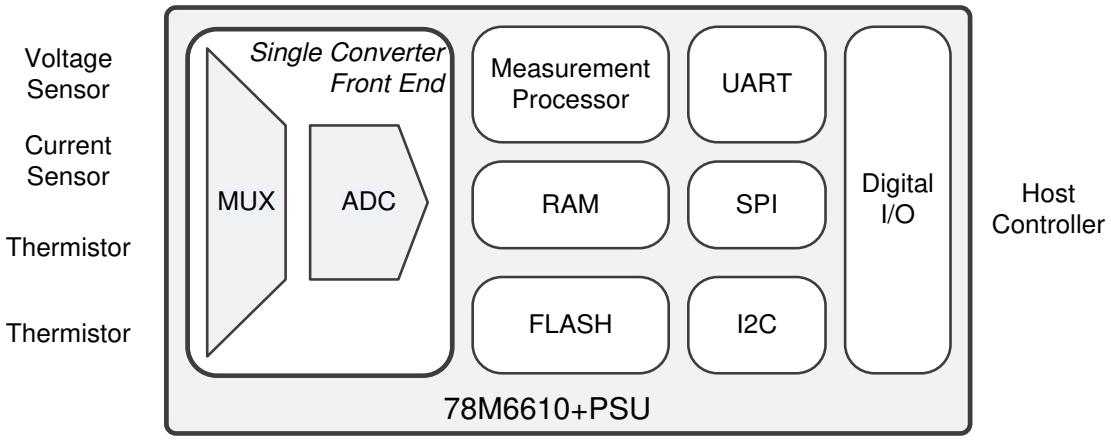
The 78M6610+PSU is a single-core energy measurement processor for single-phase power supplies. It is designed specifically for real-time monitoring at the input of AC/DC power converters used in data centers and IT server rooms. It is available in either a 24-pin QFN or 16-pin TSSOP package for optimal space savings.

The 78M6610+PSU provides four analog inputs (two differential and two single ended) for interfacing to voltage, current, and two optional temperature sensors. Scaled voltages from the sensors are fed to the single converter front-end utilizing a high-resolution delta-sigma converter. An embedded 24-bit energy measurement processor (EMP) and firmware performs all the necessary computation, compensation, and data formatting for accurate, real-time reporting to the host. With integrated flash memory, the 78M6610+PSU is a completely autonomous solution capable of storing nonvolatile data such as calibration coefficients and input configuration settings.

The 78M6610+PSU is designed to interface to the host processor via the UART interface. Alternatively, SPI or I^2C may also be used. Supported current sensors include Current Transformers (CT) and Resistive Shunts.

FEATURES

- Delta-sigma ADC with precision voltage reference
- Internal or external oscillator timing reference
- SPI, I^2C, or UART interface options with configurable I/O pins for alarm signaling, address pins, or user control
- 24-bit energy measurement processor (EMP) with integrated firmware and flash memory provides the user with:
  - True RMS calculations for current, voltage, line frequency, real power, reactive power, apparent power, and power factor
  - Compensation for ambient temperature, sensor tolerances, offsets, and EMI filter components
  - Real-time data accumulation based on an integer number of AC cycles
  - Quick calibration routines for manufacturability
  - Up to two voltage inputs for optional connection to thermal sensors



19-6396; Rev 3; 8/14

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1 On-Chip Resources Overview

The 78M6610+PSU integrates all the functional hardware blocks required to embed solid-state AC power and energy measurement. Included on the device are:

- Accurate oscillator and clock management logic
- Power-on reset, watchdog timer, and reset circuitry
- High-accuracy analog front-end (AFE) with trimmed voltage reference and temperature sensor
- 24-bit energy measurement processor (EMP)
- RAM and flash memory
- Communication interfaces
- Multipurpose Digital I/O

Figure 1-1 shows a block diagram of the device. A detailed description of various functional blocks follows.

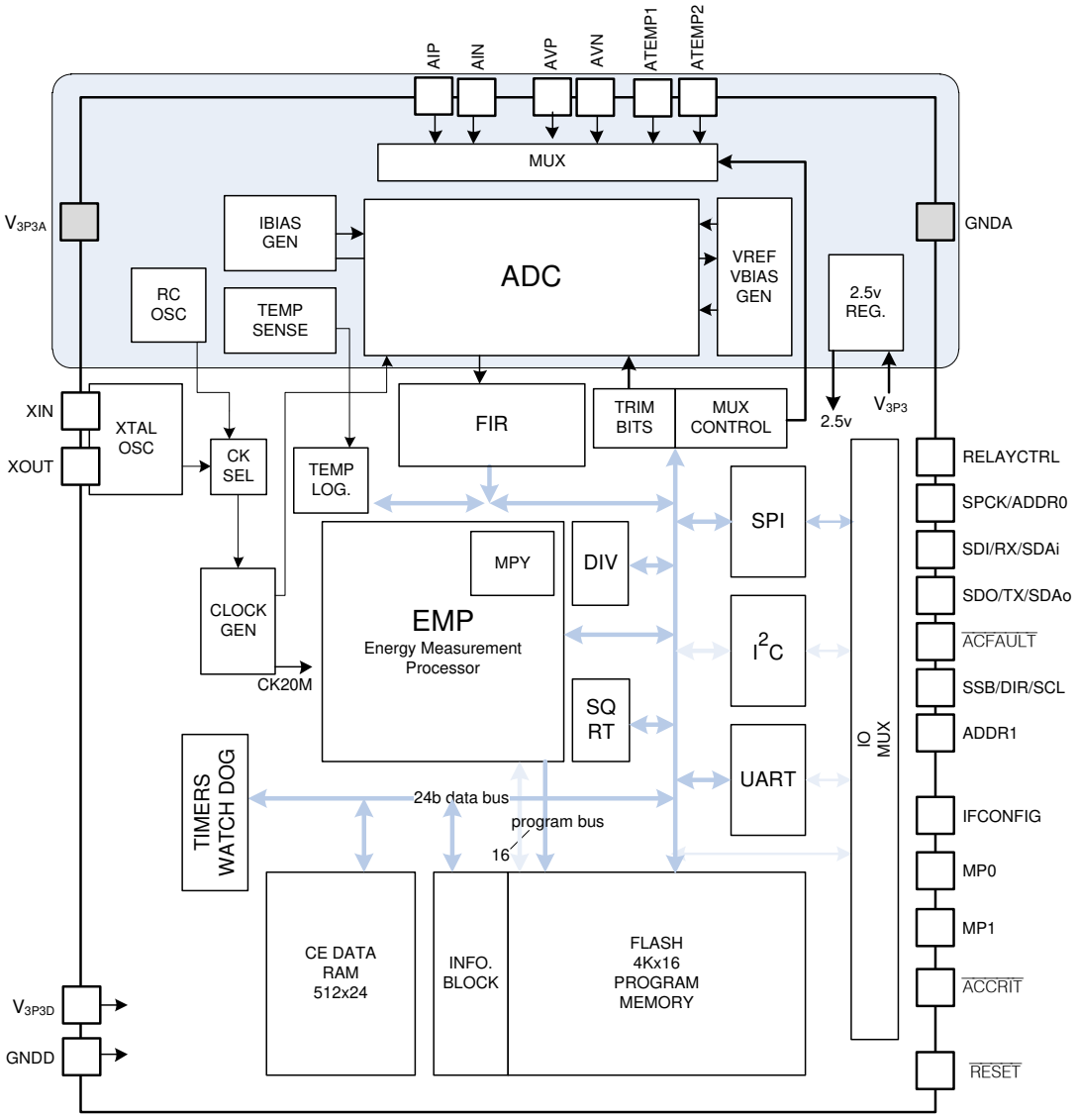


Figure 1-1: IC Functional Block Diagram

1.1 Clock Management

The 78M6610+PSU can be clocked by either the trimmed internal RC oscillator or by oscillator circuitry that relies on an external crystal. The 78M6610+PSU hardware automatically handles the clock sources logic and distributes the clock to the rest of the device.

Upon reset or power-on, the 78M6610+PSU will automatically select the external clock, if available, after 1024 clock cycles of the internal oscillator, allowing the external crystal adequate time to start up. After power-on or during run-time, the 78M6610+PSU will automatically switch to the internal oscillator in the event of a failure with the external oscillator (or crystal not mounted). This condition is also monitored by the processor and available to the user in the ALARMS register.

The internal RC oscillator is trimmed and temperature compensated. It provides an accurate clock source, however for applications requiring highest line frequency accuracy, the use of an external crystal is recommended (only available in the 24-pin QFN package).

The 78M6610+PSU external clock circuitry requires a 20.000MHz crystal. The circuitry includes two 18pF ceramic capacitors. Figure 1-2 shows the typical connection of the external crystal. This oscillator is self-biasing and therefore an external resistor should NOT be connected across the crystal.

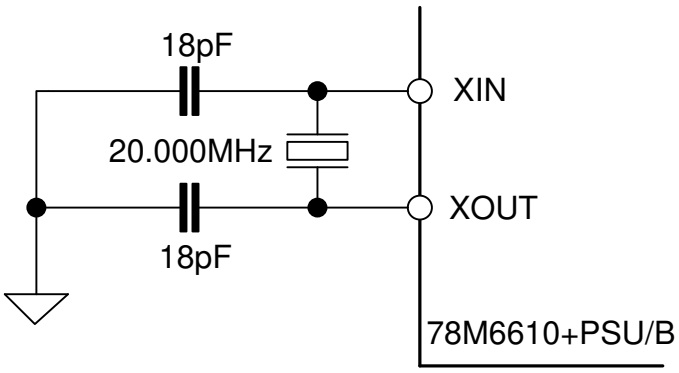


Figure 1-2: XTAL Connection

Alternatively, an external clock signal can be utilized instead of the crystal. In this case, the external clock should be connected to the XOUT pin while the XIN pin should be connected to GNDD.

If the external crystal is not utilized (not mounted), the XOUT pin should be connected to GNDD and the XIN pin left unconnected.

1.2 Power-On Reset, WD Timer, and Reset Circuitry

Power-On Reset (POR)

An on-chip Power-On Reset (POR) block monitors the supply voltage (V_{3P3D}) and initializes the internal digital circuitry at power-on. Once V_{3P3D} is above the minimum operating threshold, the POR circuit triggers and initiates a reset sequence. It will also issue a reset to the digital circuitry if the supply voltage falls below the minimum operating level.

Watchdog Timer (WDT)

A Watchdog Timer (WDT) block detects any software processing errors. The embedded software periodically refreshes the free-running watchdog timer to prevent it from timing out. If the WDT times out, it is an indication that software is no longer being executed in the intended sequence; thus, a system reset is initiated.

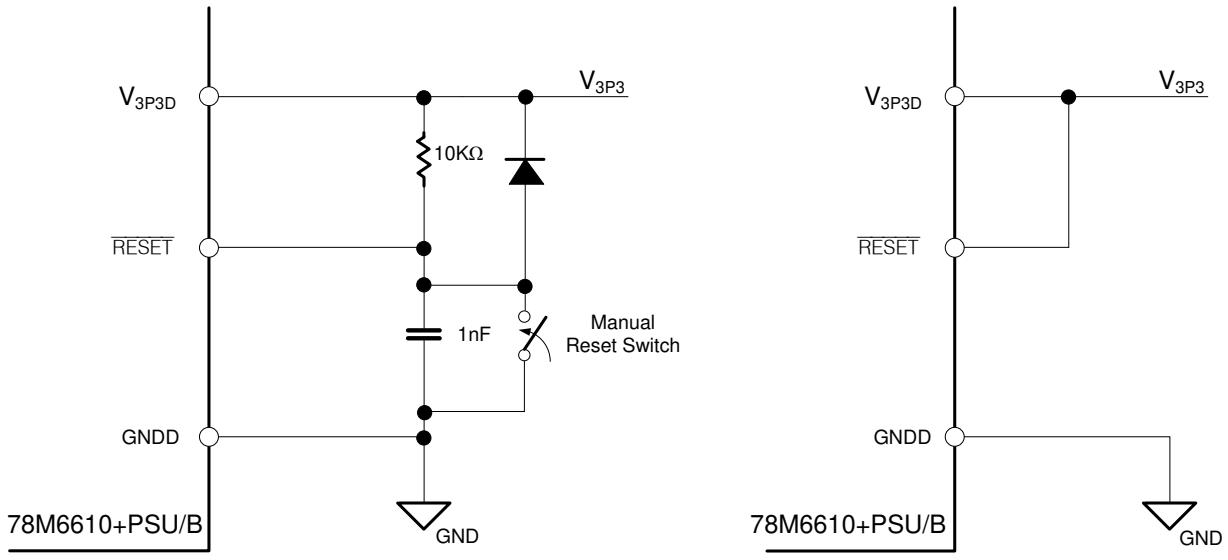
External Reset Pin ($\overline{\text{RESET}}$ Pin)

The 24-pin QFN package provides a dedicated reset ($\overline{\text{RESET}}$) pin. In addition to the internal sources, a reset can be forced by applying a low level to the $\overline{\text{RESET}}$ pin.

If the $\overline{\text{RESET}}$ pin is pulled low, all digital activities in the device stop, except the clock management circuitry and oscillators, which continue to run. The external reset input is filtered to prevent spurious reset events in noisy environments. The reset does not occur until $\overline{\text{RESET}}$ has been held low for at least 1 µs.

Once initiated, the reset mode persists until the $\overline{\text{RESET}}$ is set high and the reset timer times out (4096 clock cycles). At the completion of the reset sequence, the internal reset is released and the processor (EMP) begins executing from address 0.

If not used, the $\overline{\text{RESET}}$ pin can be connected either directly or through a pull-up resistor to V_{3P3D} supply. A simple connection diagram is shown in Figure 1-3.



a) $\overline{\text{RESET}}$ External Connection Example

b) Unused $\overline{\text{RESET}}$ Connection Example

Figure 1-3: $\overline{\text{RESET}}$ Pin Connections

1.3 Analog Front-End and Conversion

The Analog Front-End (AFE) of the 78M6610+PSU includes an input multiplexer, delta-sigma A/D converter, bias current references, voltage references, temperature sensor, and several voltage fault comparators.

Delta-Sigma A/D Converter

A second-order delta-sigma converter digitizes the analog inputs. The converted data is then processed through an FIR filter.

Voltage Reference

The device includes an on-chip precision bandgap voltage reference that incorporates auto-zero techniques as well as production trims to minimize errors caused by component mismatch and drift. The voltage reference is digitally compensated over temperature.

Die Temperature Measurement

The device includes an on-chip die temperature sensor used for digital compensation of the voltage reference. It is also used to report temperature information to the user.

Voltage and Current Inputs

The external voltage and current sensors are connected to differential voltage input pins. The full-scale signal level that can be applied to the voltage input pins is V_{3P3A} ±250 mV. Considering a sinusoidal waveform, the maximum RMS voltage is:

$$\text{VrmsMAX} = \frac{250mV}{\sqrt{2}} = 176.78\text{mV}$$

Although the voltage input is differential, a common-mode voltage of less than ±25 mV is recommended in order to utilize the available dynamic range.

Temperature Inputs

ATEMP1 and ATEMP2 are single-ended inputs that allow temperature measurement through an external sensing element (NTC, RTD etc.). The temperature measurement is generally used to monitor heat-sink or exhaust air operating conditions. TEMP2 is only available with the 24-pin package option.

1.4 24-Bit Energy Measurement Processor (EMP)

The 78M6610+PSU integrates a dedicated 24-bit signal processor that performs all the digital signal processing necessary for energy measurement, alarm generation, calibration, compensation, etc. See Section 2 for a description of functionality and operations.

1.5 Flash and RAM

The 78M6610+PSU includes 8KB of on-chip flash memory. The flash memory primarily contains program code, but also stores coefficients, calibration data, and configuration settings. The 78M6610+PSU includes 1.5KB of on-chip RAM which contains the values of input and output registers and is utilized by the FW for its operations.

1.6 Communication Peripherals

The 78M6610+PSU includes three communication interface options: UART, SPI, and I^2C.

Since the I/O pins are shared, only one mode is supported at a time. Two pins are sampled at power-on or reset to determine which interface will be active.

1.7 Multi-Purpose Digital I/O Pins

The MP0 and MP1 input/output pins are not currently used. The pins have an internal pull-up and can be left floating.

1.8 Alarm Pins ($\overline{\text{ACFAULT}}$, $\overline{\text{ACCRIT}}$)

Alarm pins are available to signal an alarm condition has been reached. Table 1-1 shows the available alarm pins and the intended usage. The alarm thresholds and conditions are programmable through dedicated registers. The status of each individual alarm is accessible through a status register.

Table 1-1: Alarm Pins Functional Description

$\overline{\text{ACFAULT}}$	Non critical warning updated once per accumulation interval.
$\overline{\text{ACCRIT}}$	Critical condition detected; AC Dropout, or SAG (see Section 2.5).

The alarm pins are open drain and active low (0=alarm). These pins need to be pulled up and can be wired-OR.

2 Functional Description and Operation

This section describes the 78M6610+PSU functionality. It includes measurements and relevant calculations, alarms, auxiliary functions such as calibrations, zero-crossing, relay control, etc.

A set of input (write), output (read) and read/write registers are provided to allow access to calculated data and alarms and to configure the device. The input (write) registers values can be saved into flash memory through a specific command. The values saved into flash memory will be loaded in these registers at reset or power-on as defaults.

2.1 Voltage and Current Inputs Conditioning

The sensor input voltages are digitized using a single integrated second-order delta-sigma A/D converter. The analog front-end includes a temperature sensor whose output is digitized and used for temperature (gain) compensation.

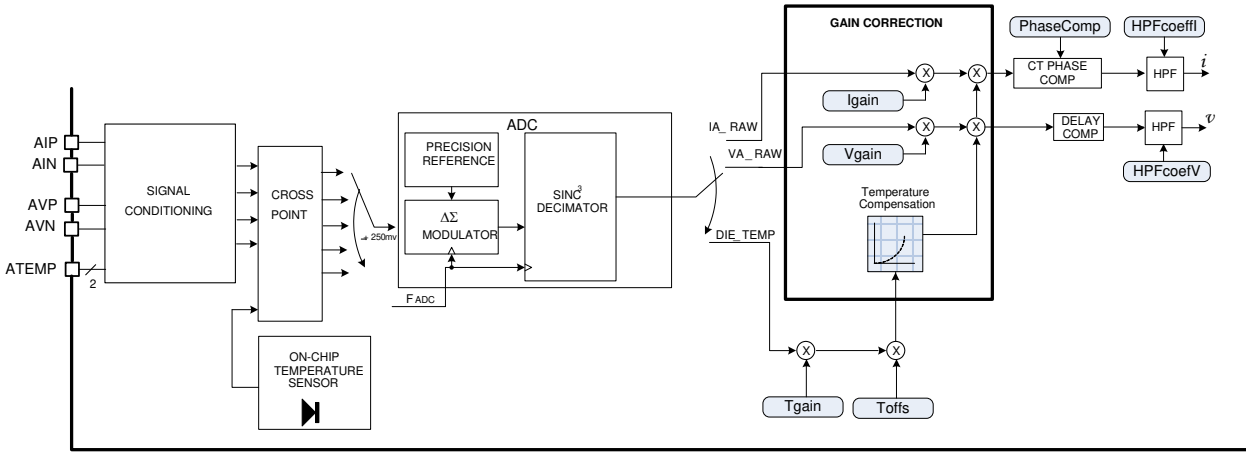


Figure 2-1: Analog Input Signal Conditioning

2.1.1 High Pass Filters (HPF) and Offset Correction

The high-pass filters (HPF) in Figure 2-1 and Figure 2-2 can remove any DC from the signal paths and consequently from power and RMS calculated values. The HPFs work by subtracting the value of the offset register (Voffs, Ioffs) from the corresponding voltage or current input. The offset registers can be set by the user, by an automatic calibration routine or adjusted dynamically by the FW.

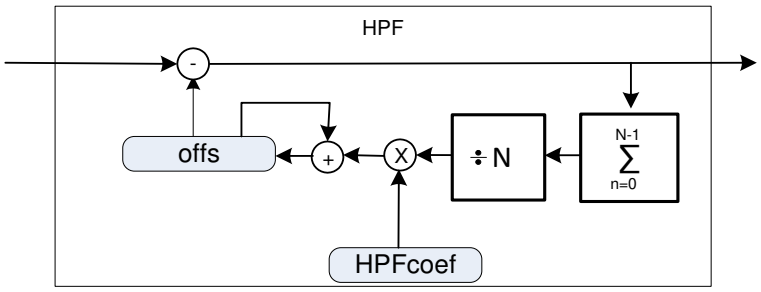


Figure 2-2: HPF

2.1.2 Phase Compensation

A phase compensation register is provided to compensate phase errors introduced by current transformers (CT) or external filters. The amount of phase shift is set by the PhaseComp register as a fractional number of ADC samples with a total range of +/- 4 ADC samples (roughly +/- 20 degrees for a 60Hz line frequency).

2.2 Current and Voltage RMS Calculations

The 78M6610+PSU provides true RMS measurements for both current and voltage inputs. The RMS is obtained by performing the square sum of the instantaneous samples of voltage and current over a time interval (commonly referred as accumulation time) and then performing a square root of the result after dividing by the number of samples in the time interval.

$$VRMS = \sqrt[2]{\frac{\sum_{n=0}^{N-1} Vn^2}{N}} \qquad IRMS = \sqrt[2]{\frac{\sum_{n=0}^{N-1} In^2}{N}}$$

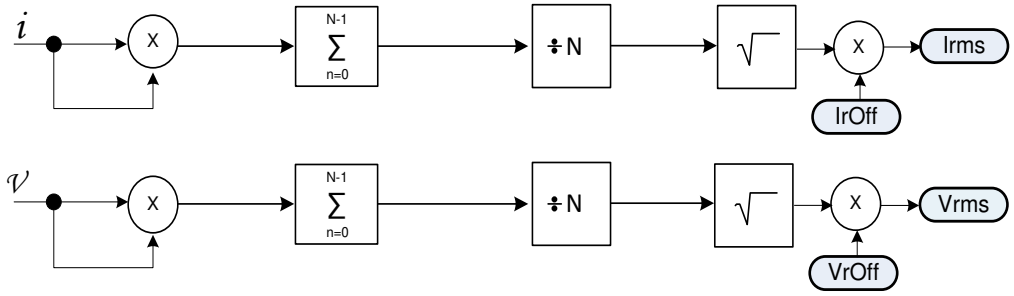


Figure 2-3: RMS Calculations

2.3 Power Calculations and Power Factor

The 78M6610+PSU computes the active, reactive, and apparent power. In addition, the 78M6610+PSU computes the fundamental power, determined only by the fundamental components of the voltage and current and the harmonic power, determined by the harmonic components of the voltage and current.

2.3.1 Active Power Calculation

Active power is calculated as the product of the voltage and current waveforms. The resulting waveform is the instantaneous power signal, and it is equal to the rate of energy flow at every instant of time. The unit of power is the watt or joules/sec. The instantaneous power is then averaged over N samples (accumulation time) for the computation of the active power available at register WATT.

$$WATT = \frac{\sum_{n=1}^{N-1} v_n \, i_n}{N}$$

2.3.2 Apparent Power

The apparent power (S) is the product of RMS voltage (V_{RMS}) and current (I_{RMS}). The apparent power results, also referred as Volt-Amps, are available at the register VA.

$$S = I_{RMS} * V_{RMS}$$

2.3.3 Power Factor

The power factor (PF) is calculated as active power (WATT) divided by the apparent power (S). The sign of the power factor is determined by the active power sign.

$$PF = \frac{\mathrm{WATT}}{\mathrm{S}}$$

2.3.4 Reactive Power

The reactive power is calculated as multiplication of instantaneous samples of current (i) and the instantaneous quadrature voltage (Vq). The quadrature voltage is obtained through a 90° phase shift (quadrature delay) of the voltage samples. The samples are then averaged over the accumulation time interval and updated in the VAR register.

$$Q = \sqrt{\sum_{n=0}^{N-1} i_n \times vq_n}$$

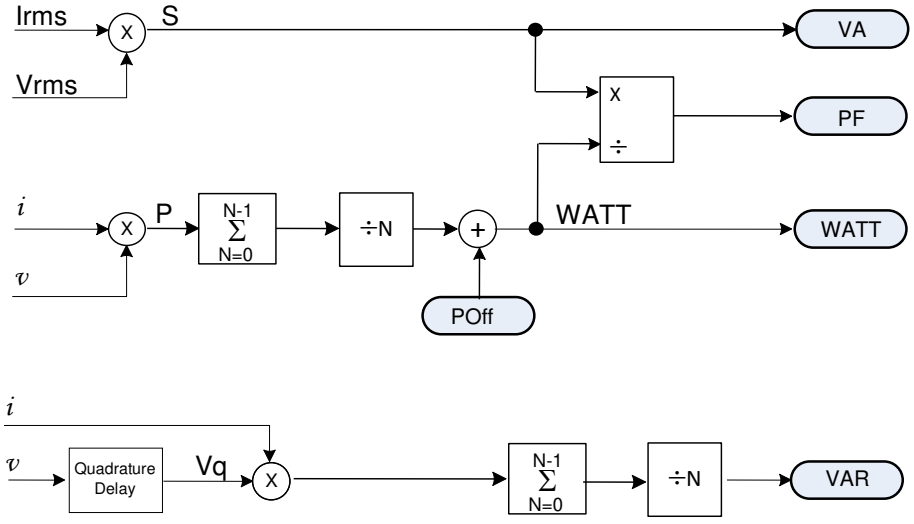


Figure 2-4: Power (Active, Reactive, and Apparent) and Power Factor Calculation

2.4 Fundamental and Harmonics Calculations

Fundamental and Harmonics

The 78M6610+PSU provides measurements on fundamental and total harmonic of voltage, current, and power (active, reactive, and apparent).

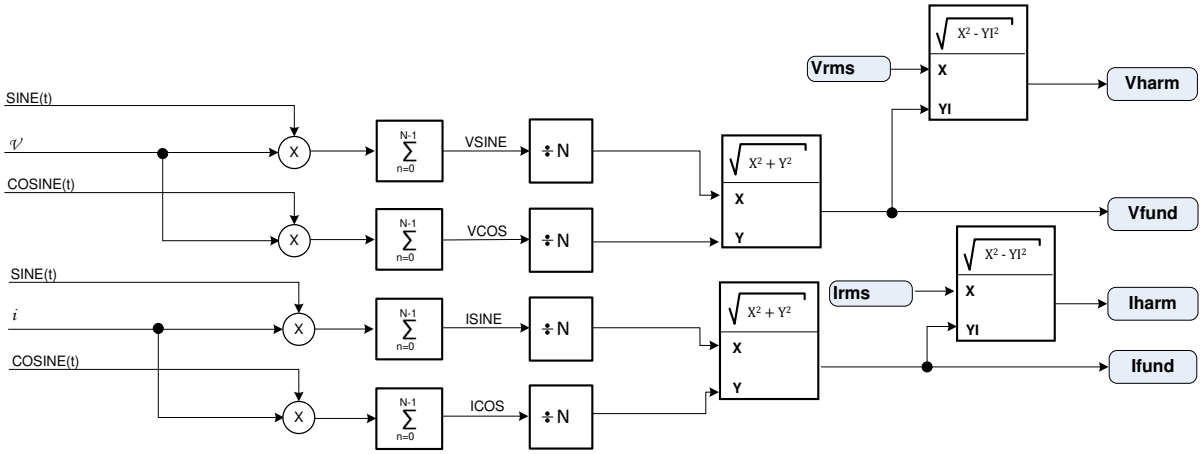


Figure 2-5: Voltage and Current Fundamental and Harmonic Calculations

Fundamental and Harmonic Selection

The 78M6610+PSU allows extraction and calculation of a single selected harmonic. By default, the fundamental (first harmonic) is selected for voltage, current, active, reactive real and apparent power calculations. The HARM register is used to select the single harmonic to extract.

By setting the value in the HARM register to a higher harmonic, the fundamental result registers will contain amplitudes of the selected harmonic. In this case the harmonic result register will contain the balance of the voltage, current, or power.

2.5 Accumulation Interval

The accumulation interval mode is configurable by the user through the Accum and AccumCyc registers and the status of the line lock bit.

The ACCUM register contains an unsigned integer values representing the accumulation interval (time) expressed in number of high-rate samples.

The accumulation interval can also be locked to the incoming line voltage cycles. The LINELOCK bit in the command register allows the accumulation interval to be determined by the ACCUM register or to be locked to the line cycle.

Once locked to the line cycle the accumulation interval will end after the first low-to-high zero crossing of the Reference AC Voltage (see Zero-Crossing Detection) input occurs once the Minimum Accumulation time has elapsed. The Actual Accumulation Interval will span an integer number of line cycles. When LINELOCK is not set, the Accumulation Interval will equal the value set by the ACCUM register.

The effective sample rate for each input of the 78M6610+PSU is 4KS/s. The DIVISOR register reports the actual number of samples within any given accumulation interval.

It is also possible to set the accumulation interval based on a number of AC Voltage line cycles. If the Line Lock (LL) Command register bit is set and AccumCyc register is non-zero then the device will calculate, on every frequency update, a new Accum value based upon the line frequency. The formula is as follows:

$$Accum = \frac{\text{SampleRate}}{\text{Line Frequency}} - 18$$

The computed Accum value locks the accumulation interval to the number of AC line voltage cycles, specified by the AccumCyc line cycles regardless of the system frequency.

2.6 Zero-Crossing Detection

The 78M6610+PSU includes a zero-crossing detection feature on both AC input channels. The zero-crossing detection allows measurements to be synchronized to the frequency of the incoming waveforms. The time delay of the zero-crossing output versus the effective zero crossing is approximately 500 µs.

2.7 Alarms

The 78M6610+PSU includes a set of user-configurable alarms. Most alarms have a corresponding register to store the threshold above which (in the case of “max” limits), or below which (in the case of “min” limits) an alarm condition is generated. Such a condition does not necessarily cause an alarm. The condition must exist for the duration of the associated hold-off time.

If the alarm condition exceeds the hold-off time, an alarm event is generated and reported in the corresponding bit of the alarm register. The corresponding event counter is also incremented.

The alarm bit will continue to be set as long as the alarm condition persists, even if the user clears it by accessing the AlarmReset register. However, event counters will only record one event until the next new assertion of the alarm.

The registers AlarmMask1 and AlarmMask2 allow the user to select which alarm will be used to drive the corresponding alarm pins (AlarmMask1 controls $\overline{\text{ACFAULT}}$ pin while AlarmMask2 controls $\overline{\text{ACCRIT}}$ pin). For example, to select OverCurrent and Vsurge to drive the $\overline{\text{ACFAULT}}$ pin, AlarmMask1 should be set to 0x000440.

The AlarmSet register allows forcing a particular alarm in the alarm register. This function is mainly intended for relay control and system test purposes.

The AlarmReset register allows clearing a particular alarm in the alarm register.

The AlarmSticky register allows the user to select which bits in the alarm register should remain set even after the alarm condition no longer exists. These bits will remain set until reset by the host/user. All other Alarms will be reset at the end of the accumulation interval unless the alarm condition remains.

Exceptions: Relay_On, Zero_Cross, and Data_Ready are not influenced by the value of the AlarmSticky register. By default, all the bits in the AlarmSticky register are set.

2.8 Voltage and Current Min/Max and Peak Tracking

2.8.1 Voltage and Current Min/Max Tracking

The 78M6610+PSU allows recording the lowest and highest voltage and current rms values. These values are stored in the registers Vhi, Vlo, Ihi, and Ilo. To reset these values it is necessary to write to these registers. For example, a value of 0x000000 should be written in the Vhi or Ihi register in order to reset them. Similarly, a value of 0x7FFFFF should be written to the Vlo and Ilo registers in order to reset them.

2.8.2 Voltage and Current Peak Tracking

The 78M6610+PSU allows recording the highest voltage and current measured during an accumulation interval. These values are updated at each accumulation interval and available on the output registers Vpeak and Ipeak, for voltage and current, respectively.

2.9 X+Y Capacitor Current and I/R Voltage Drop Compensation

The 78M6610+PSU location in the power supply AC input stage can be different from design to design. In order to achieve high accuracy, the components preceding the measurement point should be accounted for. For example, current flowing in filter capacitors or the voltage drop across PCB traces (I, Vdrop) should be considered in the measurement as shown in Figure 2-6.

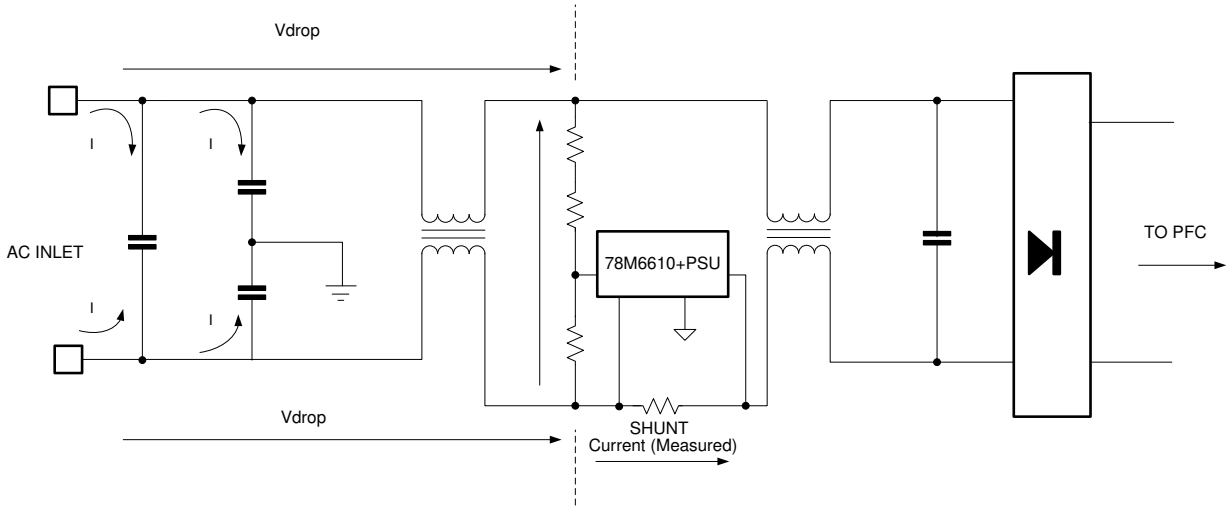


Figure 2-6: Typical Measurement Location in Power Supplies

2.9.1 X+Y Capacitor Compensation

The 78M6610+PSU, and therefore the measurement point, is usually located between the inlet and the diode bridge. This stage is where the EMI filters are usually located as shown in Figure 2-6.

In this case the current flowing through the filter (X+Y) capacitors preceding the measurement cannot be measured and is compensated for by the 78M6610+PSU. The current in flowing into these capacitors is at 90° phase respect to the voltage; therefore it has no effect on the power measurement. The effect is prominent in the current reading, in particular at light loads. Compensation is required in order to achieve higher accuracy.

A fixed coefficient value can be set for compensation, however due to the tolerance of the filter capacitors (in the +/-20% range) a calibration routine is included in the firmware. Calibration of the X+Y capacitor coefficient facilitates higher accuracy in the measurement of the current

2.9.2 I/R Voltage Drop Compensation

The PCB traces have a certain resistance that at high loads causes a voltage drop from the inlet to the measurement point. The voltage drop causes an error in the voltage and power measurements. The correction is proportional to the current measured. A coefficient proportional to the input stage resistance is available and tunable by the user. Usually this coefficient is set by the user for a specific hardware and does not require calibration.

2.10 External Temperature Monitor

The ATEMP1 and ATEMP2 inputs are dedicated to the acquisition of an external temperature. These inputs are single ended with a range of +/-250 mV referenced to the 3.3VDC supply (V_{3P3A}). The converted value is multiplied by a user programmable gain and the results are reported in the EXTEMP registers as a voltage drop from V_{3P3}.

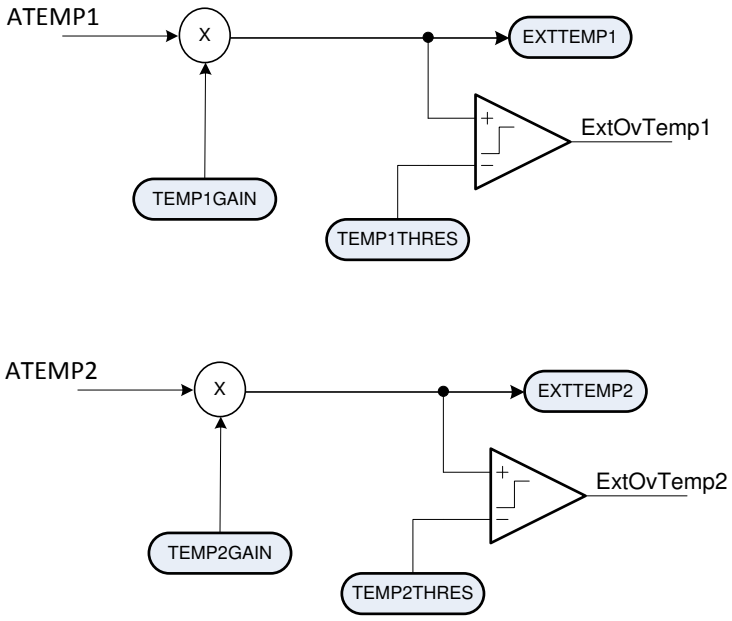


Figure 2-7: External Temperature Monitor

The output of the multiplier block is also compared with the value contained in a user-programmable register to generate a corresponding alarm once that limit value is exceeded.

2.11 Voltage Sag and Surge Detection

The 78M6610+PSU implements a voltage sag detection function, which can generate an alarm when the line voltage drops below a programmable threshold.

The firmware calculates on a sample-by-sample basis the trailing mean square of the input voltage:

$$V_{MS} = \frac{f_{line}}{2 \times f_{sample}} \times \sum_{n=-int(\frac{f_{sample}}{2 \times f_{line}})}^{0} {v_n}^2$$

At each sample interval the V_{MS} value is compared to a programmable threshold contained in the Vsag register. If V_{MS} falls below the threshold, the firmware sets the Vsag bit in the Alarms register. If Vsag is enabled in the AlarmMask2 register, the $\overline{\text{ACCRIT}}$ pin will also be asserted low. If the Vsag bit is set in the AlarmsSticky register, then Alarms.Vsag will remain set and $\overline{\text{ACCRIT}}$ will remain low until the Vsag alarm is cleared via the AlarmReset register or the 78M6610+PSU is reset. If AlarmsSticky.Vsag is cleared, then Alarms.Vsag will be cleared and $\overline{\text{ACCRIT}}$ set high as soon as the V_{MS} monitor is greater than the programmable threshold.

The sample count for sag detection is automatically adjusted by the firmware to maintain coverage over half of the AC cycle. Sag detection is disabled by default and can be enabled by writing a non-zero value to the VSAG register. If the VSAG register is set to 0, the sag feature is disabled.

The sag detection can be used to monitor or record the quality of the power line or utilize the sag alarm pin to notify external devices (for example a host microprocessor) of a pending power-down. The external device can then enter a power-down mode (for example saving data or recording the event) before a Power outage. Figure 2-8 shows a typical sag event.

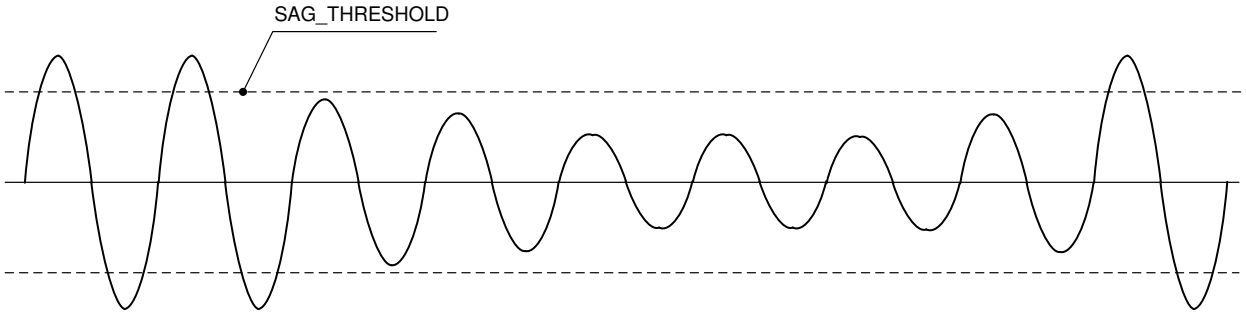


Figure 2-8: Typical Sag Event

2.12 Relay Control

The firmware includes relay control logic and provides a digital output RELAYCTRL for controlling a relay.

The relay control may operate in either an autonomous mode or in a slave mode. The operating mode is selected by the setting of the AUTORELAY bit in the COMMAND register. A bit in the ALARMS register reports the state of the RELAYCTRL output.

2.12.1 Autonomous Mode

When autonomous relay control mode is enabled, the 78M6610+PSU firmware controls the state of RELAYCTRL output, based upon the input line voltage.

At power on, RELAYCTRL output is inactive. When the RMS voltage is within specified upper and lower turn-on thresholds (RelayOnMin, RelayOnMax) for a specified time (RelayOnTime), RELAYCTRL output will be activated. Should the RMS voltage exceed the specified turn-off thresholds (RelayOffMin, RelayOffMax) for a specified time (RelayOffTime), RELAYCTRL output will be deactivated. The turn-on and turn-off thresholds are specified separately, as are delay times, to provide hysteresis to prevent unwanted switching of the relay due to short-term fluctuations in voltage.

The autonomous mode can be used to automatically control the in-rush current relay as shown in Figure 2-9.

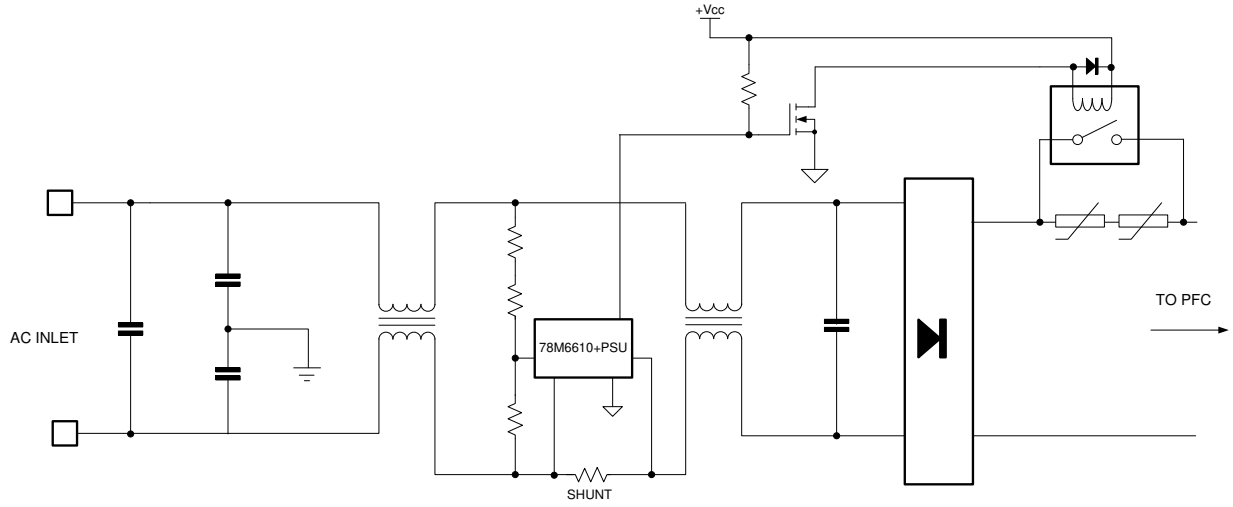


Figure 2-9: Relay Control for In-rush Current Limitation Circuitry

2.12.2 Slave Mode

When slave mode relay control is selected, the RELAYCTRL output is manually controlled by setting or clearing the RELAY_ON bit in the AlarmSet and AlarmReset registers.

2.12.3 Activation Delay

The relay control logic allows setting a delay time for energizing and de-energizing the relay. The delay time for energizing and de-energizing the relay is relative to the zero crossing of the Voltage as shown in Figure 2-10.

The time specified in the registers is expressed in the number of high-rate samples.

The default timings are:
Energized delay time (RelayOnDelay) = 0x000000 sample counts
De-Energized delay time (RelayOffDelay) = 0x000000 sample counts

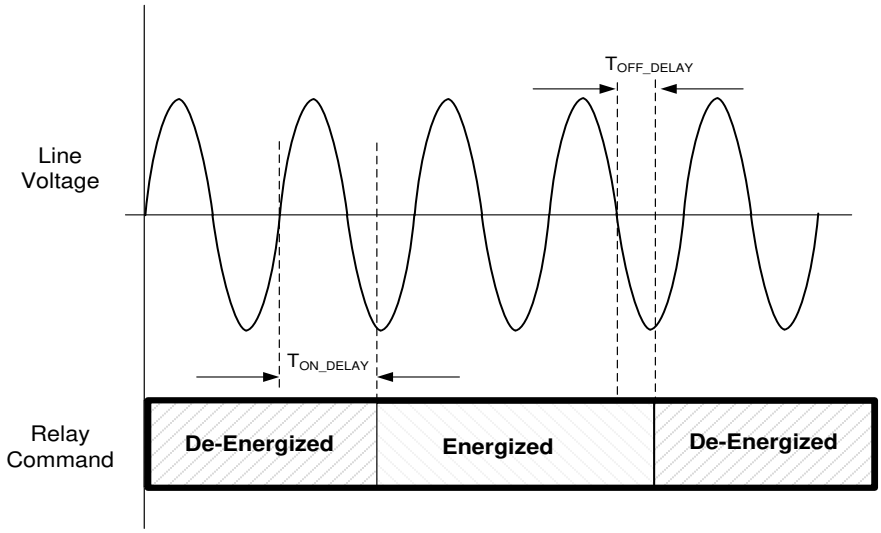


Figure 2-10: Relay Control

Table 2-1: Relay Configuration Register and Sequence Delay Register

Function	Register		Default Value	Comments
	Name	Address		
TON_Delay	RelayOnDelay	0x6b	0	Line Relay Activation Time Delay
TOFF_Delay	RelayOffDelay	0x6c	0	Line Relay De-Activation Time Delay

2.13 On-Chip Calibration Routines

The 78M6610+PSU includes current and voltage and temperature calibration routines. These routines modify gain and offset coefficients. The device also includes routines for the calibration of the X+Y capacitor and R resistance compensation coefficients.

The user can set and start a calibration routine through the Command register. When the calibration process completes, command register bits 23:16 (set to 0xCA to issue a calibration command) are cleared along with bits associated with channels that calibrated successfully. Any channels that failed will have their corresponding bit left set. After completion of the calibration, the new coefficients can be saved into flash memory as defaults by issuing the Save to Flash Command (0xACC2xx).

2.13.1 Voltage and Current Gain Calibration

In order to calibrate the voltage and current channels, a stable AC supply must be applied to the channel to be calibrated. The value corresponding to the applied AC supply (usually measured using a power meter) must be entered in the relevant target register (VTarget, ITarget). Figure 2-11 shows a typical calibration setup.

To start the calibration, the calibration command must be written to the Command register.

Initially, the value of the gain is set to unity for the selected channels. RMS values are then calculated on all inputs and averaged over the number of measurement cycles set by the register CalCyc. The new gain is calculated by dividing the appropriate Target register value by the averaged measured value. The new gain is then written to the select Gain registers unless an error occurred.

On completion, the command bits are cleared in the Command register, leaving only the system setup bits. In case of a failed calibration, the corresponding bit in the command register is left set.
During calibration, the line-lock mode should be set. Once completed, the calibration routines will store the new gain coefficients in the relevant registers. In order to save the new coefficients into flash memory as defaults, it is necessary to issue the Save to Flash Command (0xACC2xx).

2.13.2 Offset Calibration

The FW provide build in routines for calibration of the offset registers (Ioffs, Voffs).

To calibrate offset, all DC signals should be removed from all inputs although it is possible to do the calibration in the presence of AC signals. In the command, the user also specifies which channel(s) to calibrate. Target registers are not used for Offset calibration.

During the calibration process, each input is accumulated over the entire calibration interval as specified by the CalCycs register. The result is divided by the total number of samples and written to the appropriate offset register if selected in the calibration command. Using the Offset Calibration command will set the HPF coefficients (HPFcoefV, HPFcoefI) to zero thereby fixing the offset registers (Ioffs, Voffs) to their calibrated values. In order to save the new coefficients into flash memory as defaults, it is necessary to issue the Save to Flash Command (0xACC2xx).

2.13.3 X+Y Capacitor and R Compensation Coefficient Calibration

Most applications use a line input filter to minimize the EM emissions as shown in Figure 2-11. The current in the filter capacitors (Icap) preceding the 78M6610+PSU cannot be measured. In order to obtain high accuracy of the current measurement it should be compounded in the total current (Irms) calculation.

Fixed compensation coefficient values can the used, knowing the filter capacitors value. However due to the tolerance of the filter capacitors (often ±20%), in order to obtain higher accuracy in the current measurement, it could required to utilize a specific coefficient for each system. The 78M6610+PSU provides a calibration routine for the X+Y capacitor compensation coefficient.

The routine X-Y compensation coefficient calibration, utilizes both measured voltage and frequency and the target current measured using an external power meter as in Figure 2-11.

To start the command, the user writes the calibration command, setting bits XYR and I, and other needed options such as line-lock. On completion, the XYcomp parameter will be written with an estimate for the bulk capacitance. Once completed, the calibration routines will store the new gain coefficients in the relevant registers. During the calibration process, each input is accumulated over the entire calibration interval as specified by the CalCycs register.

This routine is not recursive; the user may need to re-issue the calibration command until the current reading matches the target current.

After completion of the calibration, in order to save the new coefficients into flash memory as defaults, it is necessary to issue the Save to Flash Command (0xACC2xx).

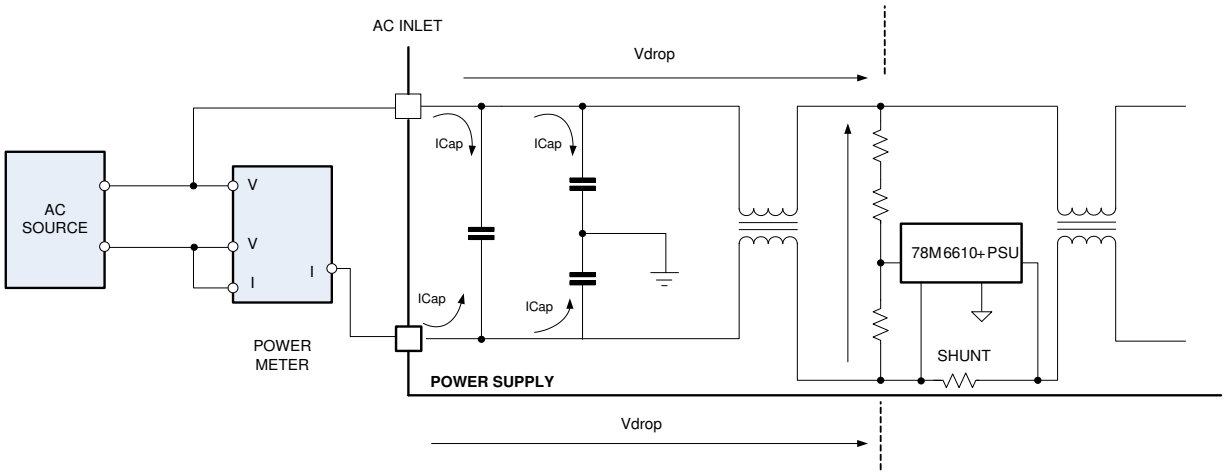


Figure 2-11: Typical Calibration Setup

2.13.4 On-Chip Temperature Calibration

To calibrate the on-chip temperature sensor, the user must first write only the “T” command bit to a “1” (all other bits 0). This command prevents the firmware from overwriting TempC register. Next the user must write the known chip temperature to TempC. Finally the user writes the Calibration Command to 0xCA0400 (Calibrate Temperature). This will cause the Toffs parameter to be updated with a new offset based on the known temperature supplied by the user. In order to save the new coefficients into flash memory as defaults, it is necessary to issue the Save to Flash Command (0xACC2xx).

2.13.5 External Temperature Calibration

To calibrate External Temperature, the user must first write only the “X” command bit to a “1” (all other bits 0). This prevents the firmware from overwriting ExtTemp. Next the user must write the known external temperature reading to ExtTemp. Finally the user writes the Calibration Command to 0xCA0100 (Calibrate External Temperature). This will cause the Xgain parameter to be updated with a new gain based on the known external temperature value supplied by the user. In order to save the new coefficients into flash memory as defaults, it is necessary to issue the Save to Flash Command (0xACC2xx).

3 Data Access and Configurability

The 78M6610+PSU has several user accessible registers that are used for configuring the device and to access results data. These registers are read (output), write (input), or read/write type, such as the Command register. These registers are accessible through the serial interfaces available on-chip (UART, SPI, and I^2C).

Warning

Writing to reserved registers or to unspecified memory locations could result in malfunctions or unexpected results.

Note

The documented address locations apply to the UART interface. For SPI or I^2C addressing, one must divide the address by 3.

3.1 Register Descriptions

Data Types

The input and output registers have different data types, depending on their assignment and functions. Table 3-1 shows the different data types.

The notation used indicates whether the number is signed, unsigned, or bit-mapped and the location of the binary point.

- U Indicates an unsigned value.
- S Indicates a signed value.
- . If present, indicates a fixed point number
- nn If to the right of the decimal, indicates the number of bits to the right of the binary point. If no decimal is present, indicates the total bits in the number.

Example: S.21

Bit Position											
23	22	21	.	20	19	18	17	…	2	1	0
$S(-2^2)$	2^1	2^0		2^{-1}	2^{-2}	2^{-3}	2^{-4}	…	2^{-19}	2^{-20}	2^{-21}

Table 3-1: Data Type Description

Data Type	Description
UINT24	A 24-bit unsigned integer having a range of 0 to 16777215. Typically used for counters
INT24	A 24-bit signed integer with a range of -8388608 to +8388607.
USI24	A 24-bit unsigned scaled integer (scaled by the user).
SSI24	A 24-bit signed scaled integer (scaled by the user).
U.24	A 24-bit unsigned fixed-point value with the binary point to the left of bit 23 with a range of 0 to $1-2^{-24}$.
U.23	A 24-bit unsigned fixed-point number with the binary point to the left of bit 22 and with a range of 0 to $1-2^{-23}$.
U.22	A 24-bit unsigned fixed-point number with the binary point to the left of bit 21 and with a range of 0 to $2-2^{-22}$.
U.21	A 24-bit unsigned fixed point number with the binary point to the left of bit 20 and with a range of 0 to $4-2^{21}$.
S.23	A 24-bit signed fixed point number with the binary point to the left of bit 22 and with a range of -1.0 to $1-2^{-23}$.
S.21	A 24-bit signed fixed-point number with a binary point to the left of bit 20 and with a range of -4.0 to $4-2^{-21.}$
S.16	A 24-bit signed fixed-point number with a binary point to the left of bit 16 and with a range of -128 to +128
Boolean (B24)	A variable containing 24 independent single-bit values.

3.2 Scaling Registers (Iscale, Vscale, Pscale, Tscale, Fscale)

The scaling registers can be used to set the full-scale values and choosing the resolution of related parameters and results.

For voltage and current inputs, full scale is defined as +/-250 mV (DC or Peak). The voltage input is usually scaled down from the AC inlet using a sensing element: resistor divider, voltage transformer, etc.

The current input is connected to current sensing element, generally a low value resistive shunt or current transformer (CT).

The Iscale and Vscale parameters need to be set in order to match the full scale range of the current and voltage inputs with the full scale range of the sensor.

Examples

Voltage: A voltage divider produces an output of 250 mV (peak) with 230 V (peak) applied at its input. A resolution of 1 mV is needed. In this case, the value of VSCALE register should be:

VSCALE = 230 * 1000 = 230000

Current: A current shunt produces a voltage drop of 250 mV (peak) at 30 A (peak). A resolution of 1 mA is needed. In this case the value of ISCALE register should be:

ISCALE = 30 * 1000 = 30000

Power: To set the power scaling register PSCALE it is necessary to multiply the full-scale voltage by the full-scale current and by the desired resolution. For 1 mW resolution:

PSCALE: 230 volts x 30 amps x 1000 = 6900000 mw. The value of Pscale register should be set to 6900000.

The scaling registers for Line Frequency, Power Factor, and Temperature do not set full scale values. They only set resolution. For example, setting Tscale to 1000 the value of the temperature is represented in 1/1000 of Degree Celsius. For example, by setting the Tscale register to 1000, a temperature of 27°C is reported as 27000 in the Temperature register.

Note

All 78M6610+PSU registers are 24 bits and most are signed. The largest signed integer is +/- 8388608. In case of larger numbers, a lower resolution must be chosen. For example, 10 mW versus 1 mW is case of PSCALE register.

Table 3-2: Registers with Scalable Values

Scaling Register	Registers Affected by Scaling
Iscale	Irms Ifund Iharm Ihi Ilo Ipeak Imax Itarget
Vscale	Vrms Vfund Vharm Vhi Vlo Vpeak Vsurge Vsag Vdrop Vmin Vmax Vtarget RelayOnMin RelayOnMax RelayOffMin RelayOffMax
Pscale	Power VA VAR Paverage Pfund Pharm Qfund Qharm Pmax
PFscale	PF
Tscale	Temperature Tmin Tmax Xtemperature Xmin Xmax
Fscale	Frequency Fmin Fmax

3.3 Output Registers

The output registers provide access to the measurement results. Unless otherwise specified, these registers are read-only. Divide the address by 3 for I^2C or SPI access.

Table 3-3: Output Registers

Address (Hex)	Variable Name	Data Type	Description
0x00	Command	B24	Command Register (see Command Register Section)
0x03	FW version	UINT24	Firmware release date in hex format (0x00YMDD)
0x12	Temperature	S.16	Chip Temperature (-128°C to +128°C, binary point to left of bit 16)
0x15	VA	SSI24	Apparent Power (LSB weight determined by Pscale)
0x18	VAR	SSI24	Reactive Power (LSB weight determined by Pscale)
0x1B	Vrms	USI24	RMS Voltage (LSB weight determined by Vscale)
0x1E	Irms	USI24	RMS Current (LSB weight determined by Iscale)
0x21	Watt	SSI24	Active Power (LSB weight determined by Pscale)
0x24	PAverage	SSI24	Active Power Averaged over 30s Window (LSB determined by Pscale)
0x27	PF	SSI24	Power Factor (LSB weight determined by PFscale)
0x2A	Frequency	USI24	Line Frequency (LSB weight determined by Fscale)
0x30	Alarms	B24	Alarm Status Registers
0x33	Vfund	USI24	RMS Voltage (Fundamental) (LSB weight determined by Vscale)
0x36	Ifund	USI24	RMS Current (Fundamental) (LSB weight determined by Iscale)
0x39	Pfund	SSI24	Active Power (Fundamental) (LSB weight determined by Pscale)
0x3C	Qfund	SSI24	Reactive Power (Fundamental) (LSB weight determined by Pscale)
0x3F	VAfund	SSI24	Apparent Power (Fundamental) (LSB weight determined by Pscale)
0x42	Vharm	USI24	RMS Voltage (Harmonic) (LSB weight determined by Vscale)
0x45	Iharm	USI24	RMS Current (Harmonic) (LSB weight determined by Iscale)
0x48	Pharm	SSI24	Active Power (Harmonic) (LSB weight determined by Pscale)
0x4B	Qharm	SSI24	Reactive Power (Harmonic) (LSB weight determined by Pscale)
0x4E	VAharm	SSI24	Apparent Power (Harmonic) (LSB weight determined by Pscale)
0x57	ILow	USI24	Lowest RMS Current Recorded Since Reset (LSB determined by Iscale)
0x5A	IHigh	USI24	Highest RMS Current Recorded Since Reset (LSB determined by Iscale)
0x5D	Ipeak	USI24	Highest Current in Last Accumulation Interval (LSB determined by Iscale)
0x60	VLow	USI24	Lowest RMS Voltage Recorded Since Reset (LSB determined by Vscale)
0x63	VHigh	USI24	Highest RMS Voltage Recorded Since Reset (LSB weight determined by Vscale)
0x66	Vpeak	USI24	Highest Voltage in Last Accumulation Interval (LSB weight determined by Vscale)
0xA8:C9	–	UINT24	Event Counters for Alarms