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78Q8430 10/100 Ethernet MAC and PHY

Simplifying System Integration™

DATA SHEET

March 2009

DESCRIPTION

The Teridian 78Q8430 is a 10/100 Fast Ethernet controller supporting multi-media offload. The device is optimized for host processor offloading and throughput enhancements for demanding multi-media applications found in Set Top Box, IP Video and Broadband Media Appliance applications. The 78Q8430 seamlessly interfaces to non-PCI processors through a simplified pseudo SRAM-like Host Bus Interface supporting 32/16/8 bit data bus widths. Supported features include IEEE802.3x flow control and full IEEE802.3 and 802.3u standards compliance.

Supporting 10Base-T and 100Base-TX, the transceiver provides Auto MDI-X cable cross-over correction, AUTO Negotiation, Link Configuration and full/half duplex support with full duplex flow control. The line interface requires only a dual 1:1 isolation transformer. Numerous packet processing and IP address resolution control functions are incorporated, including an extensive set of Error Monitoring, Reporting and Troubleshooting features. The 78Q8430 provides optimal 10/100 Ethernet connectivity in demanding video streaming and mixed-media applications.

BENEFITS

- Support for IEEE-802.3, IEEE-802.3u and IEEE-802.3-2000 Annex 31.B
- Low host CPU utilization/overhead with minimal software driver overhead and small driver memory space requirements
- Improved packet processing, low latency and low host CPU utilization
- Highest performance streaming Video over IP
- Optimized performance in mixed media application such as video, data and voice
- Ease of use, faster development cycles, high throughput
- Optimized power conservation with automatic turn on when needed
- Reduced host CPU utilization and overhead
- Improved packet processing
- Optimized performance in mixed media applications

FEATURES

- Single chip 10Base-T/100Base-TX IEEE-802.3 compliant MAC and PHY
  - Adaptive 32 kB SRAM FIFO memory allocation between Tx and Rx paths
  - Queue independent user settable water marks
  - Per queue status indication
- Address Resolution Controller (ARC)
  - Multiple perfect address filtering: 8 default (max 12)
  - Wildcard address filtering, individual, multicast and broadcast address recognition and filtering
  - Positive/negative filtering and promiscuous mode
- 64 kB JUMBO packet support
- QoS: 4 Transmit priority levels
- Non-PCI pseudo-SRAM Host Bus Interface
  - 8-bit, 16-bit and 32-bit bus width
  - Big/little endian support for 16-bit/32-bit bus widths
  - Asynchronous (100 MHz) and synchronous (50 MHz) bus clock support
- Low power and flexible power supply management
  - Power down/save
  - Wake on LAN (Magic Packet™, OnNow packet)
  - Link status change
- Traffic Offload Engine Functionality
  - Transfer frame: APF & ICMP Echo
  - IP Firewall configuration: drop frames on source IP address
  - IP Checksum
- Available in an industrial temperature range (-40 °C to +85 °C)
- RoHS compliant (6/6) lead-free package

APPLICATIONS

- Satellite, cable and IPTV Set Top Boxes
- Multi Media Residential Gateways
- High Definition 1080p/1080i DTVs
- IP-PVR and video distribution systems
- Digital Video Recorders/Players
- Routers and IADs
- Video over IP system, IP-PBX
- IP Security Cameras / PVRs
- Low latency industrial automation

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Figures

1 Introduction

The Teridian 78Q8430 is a single chip 10Base-T/100Base-TX capable Fast Ethernet Media Access Controller (MAC) and Physical Layer (PHY) transceiver. The device is optimized for video applications, such as the Set Top Box (STB), and easily interfaces to available STB core processors, such as the STi5100, STi5516, STi5514, ARM™ and Intel® based processors. The 78Q8430 is compliant with applicable IEEE-802.3 standards. MAC and PHY configuration and status registers are provided as specified by IEEE-802.3u.

The 78Q8430 operates over Category-5 Unshielded Twisted Pair (Cat-5 UTP) cabling in 100Base-TX applications and over Cat-3 UTP in 10Base-T applications requiring only a dual 1:1 isolation transformer interface to the copper media.

The Ethernet MAC section makes use of a 32 kB deep on-chip SRAM FIFO packet memory to adaptively buffer transmit and receive data. SRAM memory can be dynamically allocated to either the transmit queues or the receive queues as required to optimize throughput.

The host processor accesses the FIFO(s) using a simple asynchronous pseudo-SRAM like host bus interface. A 32 bit wide bus is provided; the bus width can be pin-configured for 8-bit, 16-bit or 32-bit bus width at boot-up. Big endian, little endian and mixed endian options are available in 32-bit operation; little endian is available for 16-bit operation. Different End-in variations are supported through internal circuitry with minimal user intervention required.

The MAC interface logic may assert MEMWAIT during bus transactions, requesting wait states from the host while critical internal data transfer completes. The MAC provides both half duplex and full duplex operation, as well as support for full duplex flow control. Complete, portable device drivers for Linux®, OS20 and VxWorks® are available.

The 78Q8430 operates from a single 3.3 V supply. Power down modes and power saving modes are available. The 78Q8430 defaults to use an on-chip crystal oscillator. In this mode, a 25 MHz reference crystal is connected between the XTLP and XTLN pins. Alternatively, an externally generated 25 MHz clock can be connected to the XTLP pin. The chip will automatically configure itself to use the external clock. In this mode of operation, a crystal is not required.

1.1 Systems Applications

Figure **1** presents an overview of the 78Q8430 in a block diagram.

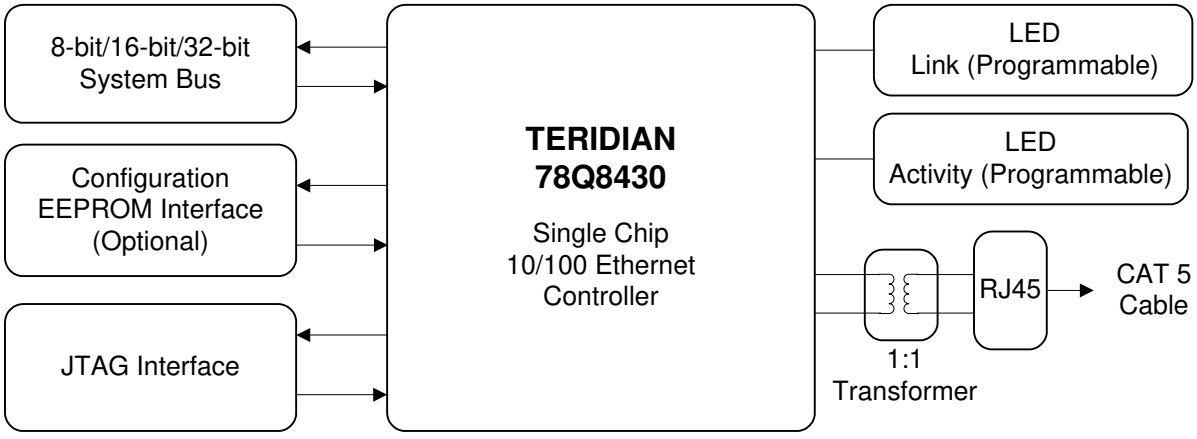

Figure 1: 78Q8430 Block Diagram

1.2 System Level Application Information

This section provides an overview of system level applications in some typical high-volume consumer equipment.

1.2.1 Set Top Box Application

Figure 2 shows a typical application diagram for a set top box.

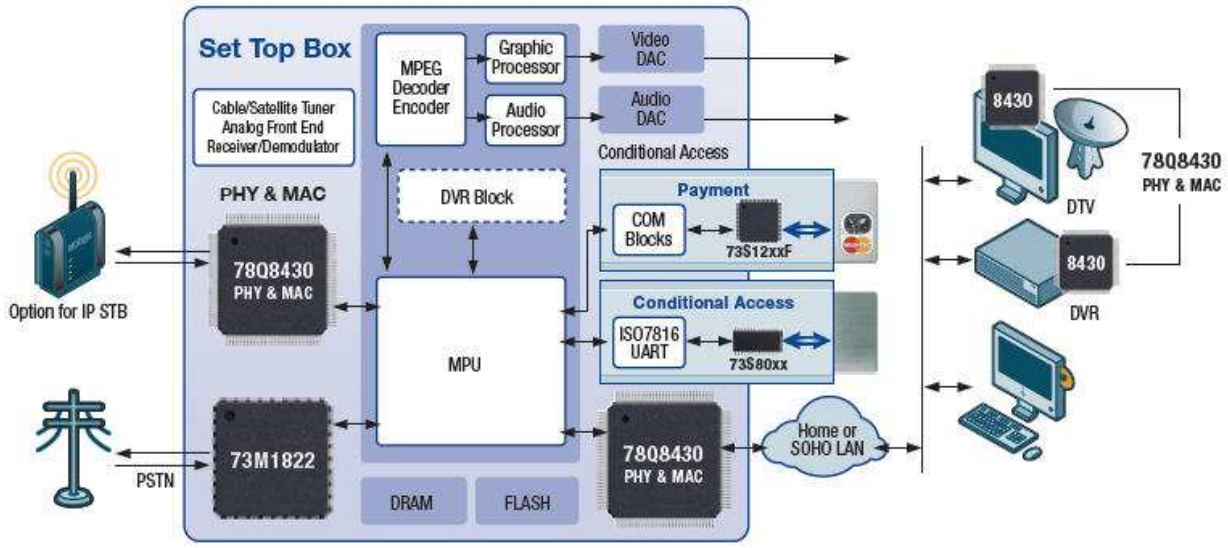

Figure 2: Set Top Box Diagram

1.2.2 IP Security Application

Figure 3 shows a typical application diagram for an IPTV security camera application.

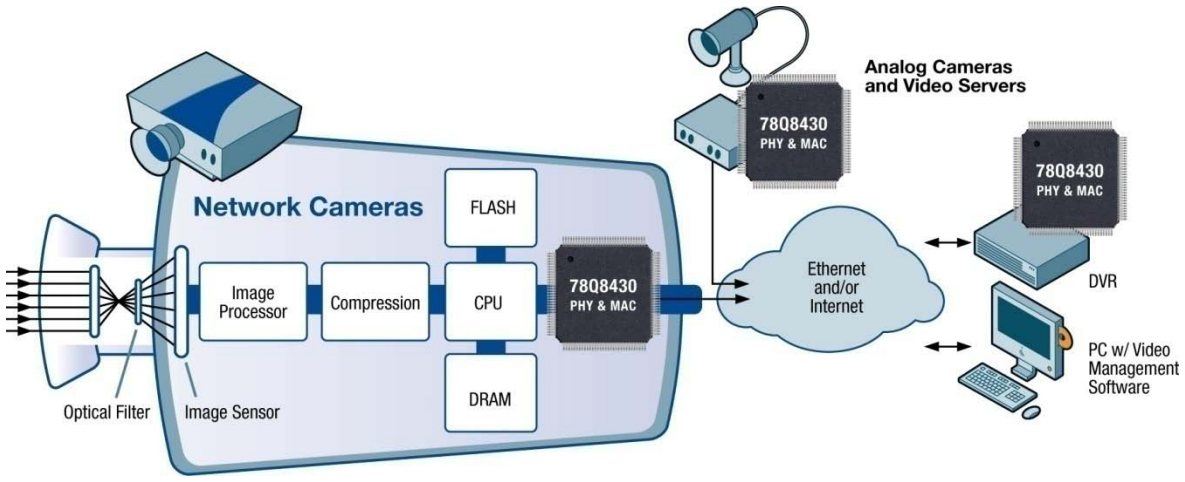

Figure 3: Network Cameras Diagram

1.2.3 IP PBX Application

Figure 4 shows a typical application diagram for an IP PBX application.

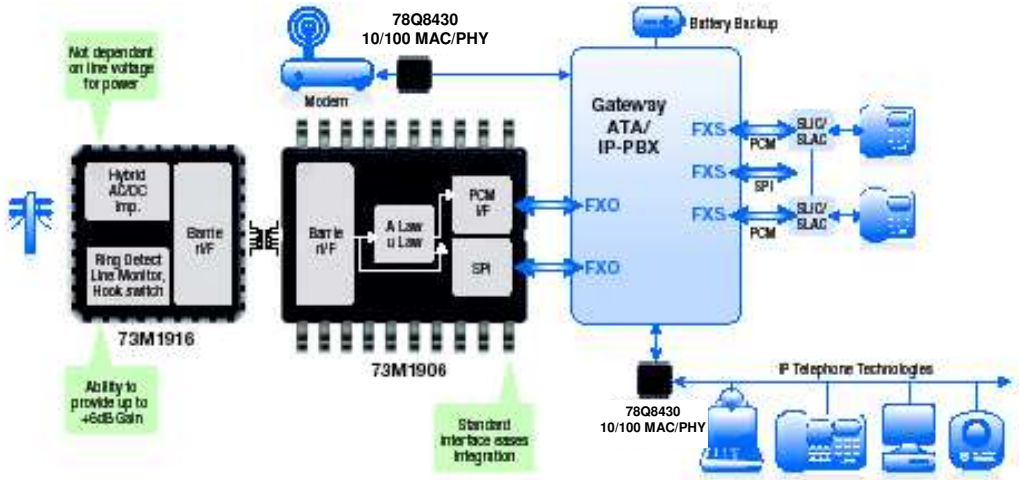

Figure 4: Typical FXO VoIP Application

1.3 Overview

The 78Q8430 is divided into four sections, as shown in Figure 5.

- Generic Bus Interface (GBI) Control Layer
- Queue Memory Layer
- Ethernet Media Access Control (MAC) Layer
- Ethernet Physical (PHY) Layer

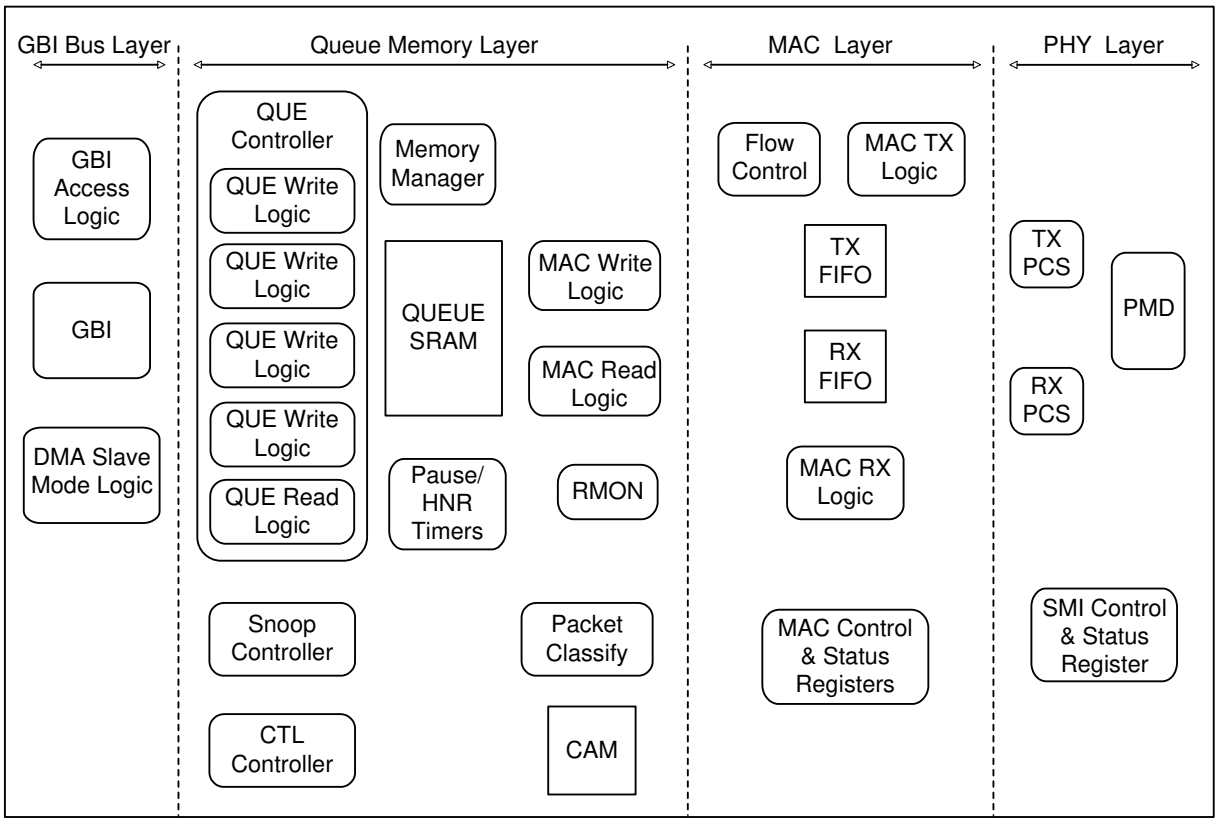

Figure 5: Device Block Diagram

1.4 Application Environments

This section provides an overview of the application environments such as the STMicroelectronics and Embest ARM9™ processors, for which the 78Q8430 provides a seamless interface. Figure 6 shows a simple application diagram for a design using the GBI based 10/100-Mbps Ethernet Controller. By providing a direct connection to the GBI bus, applications requiring Ethernet network access can be realized with a high degree of integration. The figure shows the processor and the Ethernet controller with connected address and data buses. This connection can be either on the motherboard, or via an expansion module. The GBI Controller controls the address and data and the system control signals.

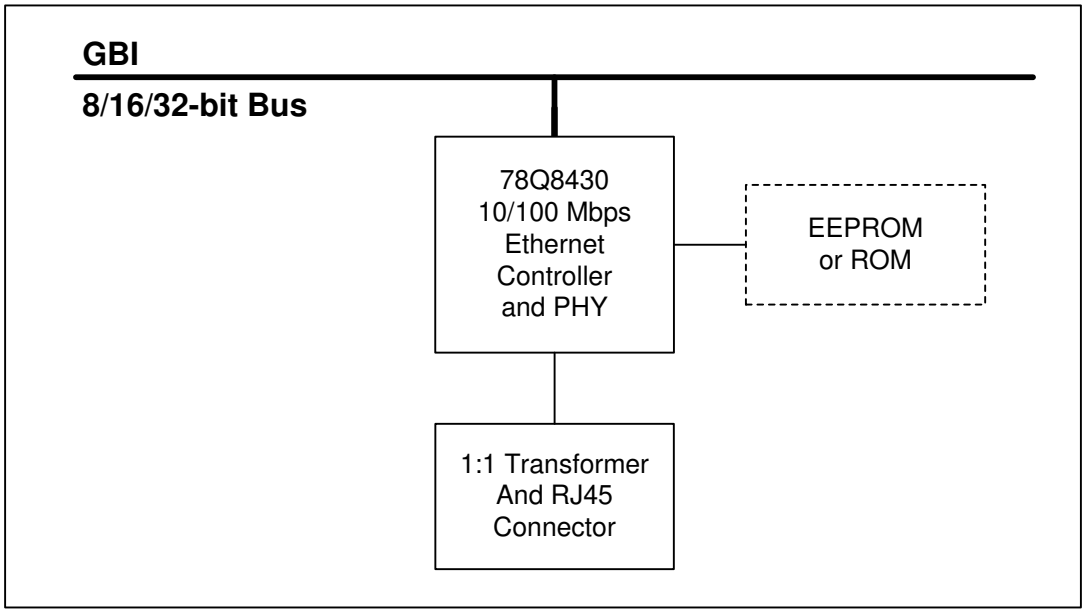

Figure 6: GBI Bus Block Diagram

Figure 6 shows the components that are likely to be used with the 10/100-Mbps Ethernet Controller. The integrated PHY is designed to directly connect to an integrated 1:1 transformer and RJ-45 connector, thereby providing a minimum parts solution.

1.5 Supply Voltages

The 78Q8430 requires a single 3.3 V (+/-5%) supply voltage. No external components are required to generate on-chip bias voltages and currents. High accuracy is maintained through a closed-loop trimmed biasing network. On-chip power converters generate 1.8 V power for core digital logic and memory blocks. The voltage regulator is not affected by the power-down mode.

1.6 Power Management

The 78Q8430 supports both normal and power-saving modes. When the GBI bus is active, it can be in normal mode or Power Management low-power modes.

2 Pinout

The 78Q8430 is available in a 14x14 mm 100-pin LQFP package.

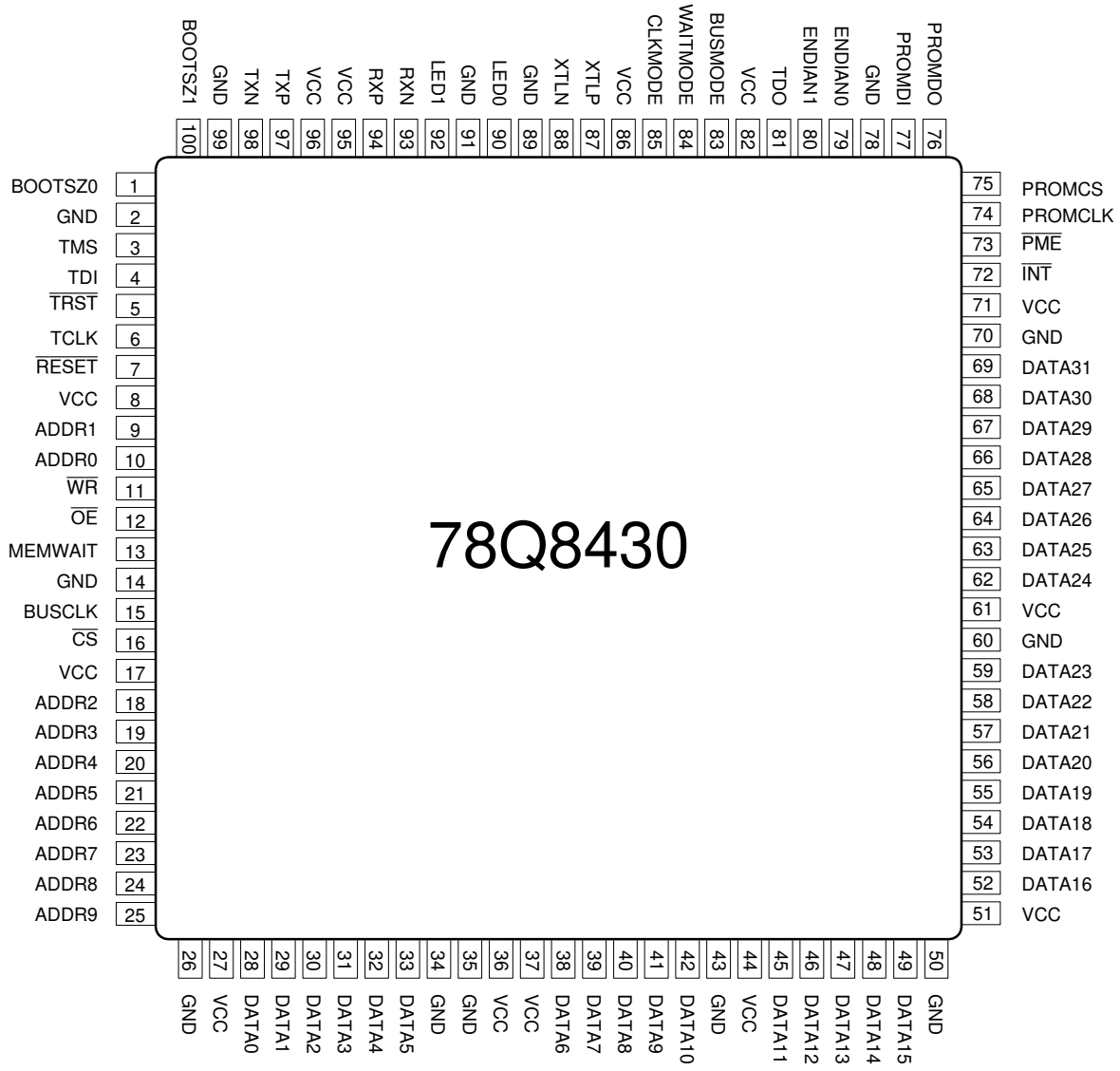

Figure 7: Pinout

3 Pin Description

3.1 Pin Legend

Table 1 lists the different pin types found on the 78Q8430 device. The Type field of the pin description tables refers to one of these types.

Table 1: Pin Legend

Type	Description
A	Analog
IU	TTL-level Input, with Pull-up
IS	TTL-level Input, with Schmitt Trigger
O	TTL-level Output
OD	TTL-level Output (Open Drain)
S	Supply
I	TTL-level Input
ID	TTL-level Input, with Pull-down
B	TTL-level Bidirectional Pin
OZ	TTL-level Output (Tristate)
G	Ground

3.2 Pin Descriptions

The pin descriptions in the following tables are grouped by interface. A pin number, type specification per Table 2 and a functional description is provided for each pin on the 78Q8430 device.

3.2.1 Clock Pins

Table 2: Clock Pin Descriptions

Signal	Pin Number	Type	Description
XTLP	87	A	**Crystal Positive/Negative** To use the internal oscillator, connect a 25 MHz crystal across XTLP and XTLN. To use of an external clock, XTLN is grounded and XTLP is driven with a 25 MHz clock. Provides timing reference for all media dependant interface operations. An internal PLL is used to multiply this clock by four for use as the main system clock in internal clock mode.
XTLN	88		
BUSCLK	15	I	**Peripheral Clock** The source for the main system clock in external clock mode. In synchronous bus mode, all host bus signals are assumed to be synchronous to this clock.

3.2.2 Media Dependent Interface (MDI) Pins

Table 3: MDI Pin Descriptions

Signal	Pin Number	Type	Description
TXP	97	A	**Transmit Output Positive/Negative** Transmitter outputs for both 10BASE-T and 100BASE-TX. MDI-X Mode: Receive Input Positive/Negative Receiver inputs for both 10BASE-T and 100BASE-TX.
TXN	98	A	
RXP	94	A	**Receive Input Positive/Negative** Receiver inputs for both 10BASE-T and 100BASE-TX. MDI-X Mode: Transmit Output Positive/Negative Transmitter outputs for both 10BASE-T and 100BASE- TX.
RXN	93	A	

3.2.3 LED Display (PHY) Pins

The LED pins use standard logic drivers. They output a logic low when the LED is meant to be on and are tri-state when it is meant to be off. The LED cathode should be connected to the output pin and a series resistor from the power supply connected to the LED anode.

Table 4: LED Pin Descriptions

Signal	Pin Number	Type	Description
LED0	90	OZ	**PHY display LED0 (Link OK)** The default for LED0 is Link OK (LED is on for link established).
LED1	92	OZ	**PHY display LED1 (Activity)** The default for LED1 is Link Activity (LED blinks for Rx or Tx data transferred).

3.2.4 EEPROM Pins

Table 5: **EEPROM Interface Pin Descriptions**

Signal	Pin Number	Type	Description
PROM_CS	75	O	**EEPROM Chip Select** Used to frame transmissions to and from an external EEPROM.
PROM_CLK	74	O	**EEPROM Clock** Clock for transmitting to and from an external EEPROM/ROM. This is compatible with the slowest commercial parts, which specify a maximum frequency of 1 MHz.
PROM_DI	77	I	**EEPROM Data In** Data line for transmitting from the external EEPROM to the controller. Must be high with no EEPROM present.
PROM_DO	76	OZ	**EEPROM Data Out** Transfers data from the controller to an external EEPROM/ROM.

3.2.5 GBI Data Pins

Table 6: GBI Data Pin Descriptions

Signal	Pin Number	Type	Description
DATA31	69	B	**Data Bus DATA[31:0]** Bi-directional host bus data. The BOOTSZ pins determine how many of these are actually used. The $\overline{OE}$ input will disable the output drivers to prevent bus collisions.
DATA30	68		
DATA29	67		
DATA28	66		
DATA27	65		
DATA26	64		
DATA25	63		
DATA24	62		
DATA23	59		
DATA22	58		
DATA21	57		
DATA20	56		
DATA19	55		
DATA18	54		
DATA17	53		
DATA16	52		
DATA15	49		
DATA14	48		
DATA13	47		
DATA12	46		
DATA11	45		
DATA10	42		
DATA9	41		
DATA8	40		
DATA7	39		
DATA6	38		
DATA5	33		
DATA4	32		
DATA3	31		
DATA2	30		
DATA1	29		
DATA0	28		

3.2.6 GBI Address Pins

Table 7: GBI Address Pin Descriptions

Signal	Pin Number	Type	Description
ADDR9	25	I	**Address Bus** The address lines are required to be stable for the entire duration of a $\overline{CS}$ cycle. In synchronous bus mode, the address pins are sampled on the first rising edge of BUSCLK that $\overline{CS}$ is asserted low. In asynchronous bus mode, the address pins are sampled as soon as the falling edge of $\overline{CS}$ is synchronized to the internal system clock. In 32-bit bus mode, ADDR[1:0] are ignored. In 16-bit bus mode, ADDR[0] is ignored. In 8-bit bus mode, all ADDR bits are used to reference a register byte.
ADDR8	24	I	
ADDR7	23	I	
ADDR6	22	I	
ADDR5	21	I	
ADDR4	20	I	
ADDR3	19	I	
ADDR2	18	I	
ADDR1	9	I	
ADDR0	10	I	

3.2.7 GBI Control Pins

Table 8: GBI Control Pin Descriptions

Signal	Pin Number	Type	Description
$\overline{RESET}$	7	I	**Reset (active low)** Referred to as hardware reset. Causes all 78Q8430 outputs to enter a high-impedance state, stops all current operations and initializes registers.
$\overline{CS}$	16	I	**Chip Select (active low)** The Processor asserts this signal to initiate a read or write operation.
$\overline{WR}$	11	I	**Write Enable (active low)** The Processor asserts $\overline{WR}$ to indicate a write operation.
OE	12	I	**Output Enable (active low)** The Processor asserts $\overline{OE}$ to enable the 78Q8430 data drivers during a read cycle.
MEMWAIT	13	OZ	**Memory Wait** During a bus cycle the 78Q8430 asserts MEMWAIT to indicate that it is not ready to drive or receive valid data on the DATA lines. The polarity is dependent on the WAITMODE pin. When WAITMODE is high then the pin is asserted high; when WAITMODE is low then the pin is asserted low.
$\overline{INT}$	72	OD	**Interrupt (active low)** The 78Q8430 asserts the $\overline{INT}$ signal low when it detects an interrupt event.
$\overline{PME}$	73	OD	**Power Management Event (active low)** The 78Q8430 asserts the $\overline{PME}$ signal low when it detects a wake-up event.

3.2.8 Mode Pins

Table 9: Chip Mode Pin Descriptions

Signal	Pin Number	Type	Description
BUSMODE	83	I	**BUSMODE, CLKMODE, WAITMODE Configuration** 0,0,0 = Sync bus, ext. system clock, memwait act low 0,0,1 = Sync bus, ext. system clock, memwait act high 0,1,0 = Reserved 0,1,1 = Reserved 1,0,0 = Async bus, ext. system clock, memwait act low 1,0,1 = Async bus, ext. system clock, memwait act high 1,1,0 = Async bus, int. system clock, memwait act low 1,1,1 = Async bus, int. system clock, memwait act high
CLKMODE	85	I	
WAITMODE	84	I	
ENDIAN0	79	I	**Data Bus Endian Select** 0,0 = Big endian (MSB at high bit positions) 0,1 = Bytes are little endian inside 16-bit words 1,0 = Word endian (MSW at low bit positions) 1,1 = Little endian (MSB at low bit positions)
ENDIAN1	80	I	
BOOTSZ1	100	I	**GBI Bus Size** BOOTSZ[1:0]: is strapped to indicate the GBI bus size: 00 = Bus is 32 bits wide 01 = Bus is 16 bits wide. Only DATA[15:0] are used. 10 = Bus is 8 bits wide. Only DATA[7:0] are used. 11 = Reserved
BOOTSZ0	1	I	

Notes:

1. The internal PHY should never be powered down when the internal system clock is selected by the CLKMODE pin (CLKMODE=1)
2. There is no external visibility for the system clock when the internal clock mode is selected. The GBI interface must therefore always be used in asynchronous bus mode.

3.2.9 JTAG Pins

Table 10: JTAG Pin Descriptions

Signal	Pin Number	Type	Description
$\overline{\text{TRST}}$	5	I	**Test Reset (active low)** System provided reset for JTAG logic.
TCLK	6	I	**Test Clock** System provided clock for JTAG logic.
TMS	3	IU	**Test Mode Select** Enables JTAG boundary scan using serial in/serial out ports. Sampled on rising edge of TCLK.
TDI	4	IU	**Test Data In** Serial input port for clocking in test data to be shifted to the output at the end of the boundary scan chain (TDO).
TDO	81	O	**Test Data Out** Serial output port for clocking out test data shifted from the input at the beginning of the boundary scan chain (TDI).

3.2.10 Power Pins

Table 11: Power Pin Descriptions

Signal	Pin Number	Type	Description
VCCA	86 95 96	S	3.3 V supply for the analog transmit section.
VCC	8 17 27 36-37 44 51 61 71 82	S	3.3 V supply for the digital logic section.
GND	2 14 26 34-35 43 50 60 70 78 89 91 99	G	Common ground return.

4 Electrical Specification

4.1 Absolute Maximum Ratings

Operation above the maximum rating may permanently damage the device.

Table 12: Absolute Maximum Ratings

Parameter	Rating
DC Supply Voltage (V_{CC})	-0.5 to 4.0 VDC
Storage Temperature	-65 to 150 °C
Pin Voltage (except TXOP/N and RXIP/N)	-0.3 to (V_{CC}+0.6) VDC
Pin Voltage (TXOP/N and RXIP/N only)	-0.3 to (V_{CC}+1.4) VDC
Pin Current	± 120 mA

4.2 Recommended Operation Conditions

Unless otherwise noted all specifications are valid over these temperatures and supply voltage ranges.

Table 13: Recommended Operating Conditions

Parameter	Rating
DC Voltage Supply (V_{CC})	3.3 ± 0.17 VDC
Ambient Operating Temperature (T_{AMB})	-40 to +85 °C

4.3 DC Characteristics

Table 14: DC Characteristics

Parameter	Symbol	Conditions	Min	Nom	Max	Unit
Supply Current	I_{CC}	V_{CC} = 3.3 V Auto-Negotiation 10BT (Idle) 10BT (Normal Activity) 100BTX	–	– 124 110 230 165	– 150 140 250 190	– mA
Supply Current	I_{CC}	Power-down mode	–	14	45	mA

4.4 Digital I/O Characteristics

Table 15: Digital I/O Characteristics

Parameter	Symbol	Conditions	Min	Nom	Max	Unit
Input Voltage Low	V_{IL}		–	–	0.8	V
Input Voltage High	V_{IH}		2.0	–	–	V
Input Current	I_{IL}, I_{IH}		-1	–	1	µA
Input Capacitance	C_{IN}		–	8	–	pF
Output Voltage Low	V_{OL}	I_{OL} = 8 mA	–	–	0.4	V
Output Voltage High**	V_{OH}	I_{OH} = -8 mA	2.4	–	–	V
Output Transition Time	T_T	C_L = 20 pF I_{OH} = -8 ma (H to Z)	–	–	6	ns
Tri-state Output Leakage Current*	I_Z	Type tri-state only	-1	–	1	µA

**PMEB and INTB are active low outputs requiring external pull-up resistors. V_{OH} for these outputs is not specified.

4.5 Analog Electrical Characteristics

4.5.1 100Base-TX Transmitter

Table 16: MII 100Base-TX Transmit Timing

Parameter	Conditions	Min	Nom	Max	Unit
Peak Output Amplitude ($\|V_P+\|$, $\|V_P-\|$) (see note below)	Best-fit over 14 bit times; 0.4 dB Transformer loss	950	–	1050	mVpk
Output Amplitude Symmetry	$\|V_P+\|$ $\|V_P-\|$	0.98	–	1.02	
Output Overshoot	Percent of V_P+, V_P-	–	–	5	%
Rise/Fall time (t_R, t_F)	10-90% of V_P+, V_P-	3	–	5	ns
Rise/Fall time Imbalance	$\|t_R - t_F\|$	–	–	500	ps
Duty Cycle Distortion	Deviation from best-fit time-grid; 010101... Sequence	–	–	±250	ps
Jitter	Scrambled Idle, Internal Oscillator Mode	–	–	1.4	ns

Note: Measured at the line side of the transformer. Test Condition: Transformer P/N: TLA-6T103. Line Termination: 100 Ω±1%

4.5.2 100Base-TX Transmitter (Informative)

Table 17: MII 100Base-TX Transmitter (Informative)

Parameter	Conditions	Min	Max	Unit
Return Loss	2 < f < 30 MHz 30 < f < 60 MHz 60 < f < 80 MHz	16 $16 - 20\log\left(\frac{f}{30MHz}\right)$ 10	–	dB
Open-Circuit Inductance	-8 < I_{IN} < 8 mA	350	–	µH

Note: The specifications in the preceding table are included for information only. They are mainly a function of the external transformer and termination resistors used for measurements.

4.5.3 100Base-TX Receiver

Table 18: MII 100Base-TX Receiver Timing

Parameter	Conditions	Min	Nom	Max	Unit
Signal Detect Assertion Threshold		600	700	800	mVppd
Signal Detect De-assertion Threshold		300	350	400	mVppd
Differential Input Resistance		–	20	–	kΩ
Jitter Tolerance (pk-pk)		4	–	–	ns
Baseline Wander Tracking		-75	–	+75	%
Signal Detect Assertion Time	Not tested	–	–	1000	µs
Signal Detect De-assertion Time	Not tested	–	–	4	µs

4.5.4 10Base-T Transmitter

Table 19: MII 10Base-T Transmitter Timing

Parameter	Conditions	Min	Nom	Max	Unit
Peak Differential Output Signal (see note below)	All data patterns	2.2	–	2.8	V
Harmonic Content (dB below fundamental)	Any harmonic All ones data Not tested	27	–	–	dB
Link Pulse Width		–	100	–	ns
Start-of-Idle Pulse Width	Last bit 0 Last bit 1	– –	300 350	– –	ns ns

Note: The Manchester-encoded data pulses, the link pulse and the start-of-idle pulse are tested against the templates and using the procedures found in Clause 14 of IEEE 802.3. Measured at the line side of the transformer. Test Condition: Transformer P/N: TLA-6T103. Line Termination: 100 Ω±1%

4.5.5 10Base-T Transmitter (Informative)

Table 20: MII 10Base-T Transmitter (Informative)

Parameter	Conditions	Min	Nom	Max	Unit
Output Return Loss		15	–	–	dB
Output Impedance Balance	1 MHz < freq < 20 MHz	$29 - 17\log\left(\frac{f}{10}\right)$	–	–	dB
Peak Common-mode Output Voltage		–	–	50	mV
Common-mode Rejection	15 V_{PK}, 10.1 MHz sine wave applied to transmitter common-mode. All data sequences.	–	–	100	mV
Common-mode Rejection Jitter	15 V_{PK}, 10.1 MHz sine wave applied to transmitter common-mode. All data sequences.	–	–	1	ns

Note: The specifications in the preceding table are included for information only. They are mainly a function of the external transformer and termination resistors used for measurements

4.5.6 10Base-T Receiver

Table 21: MII 10Base-T Receive Timing

Parameter	Conditions	Min	Nom	Max	Unit
DLL Phase Acquisition Time		–	10	–	BT
Jitter Tolerance (pk-pk)		30	–	–	ns
Input Squelched Threshold		500	600	700	mVppd
Input Unsquelched Threshold		275	350	425	mVppd
Differential Input Resistance		–	20	–	kΩ
Bit Error Ratio		–	10^{-10}	–	
Common-mode Rejection	Square wave 0 < f < 500 kHz Not tested	25	–	–	V

5 Host Interface Timing Specification

5.1 Host Interface

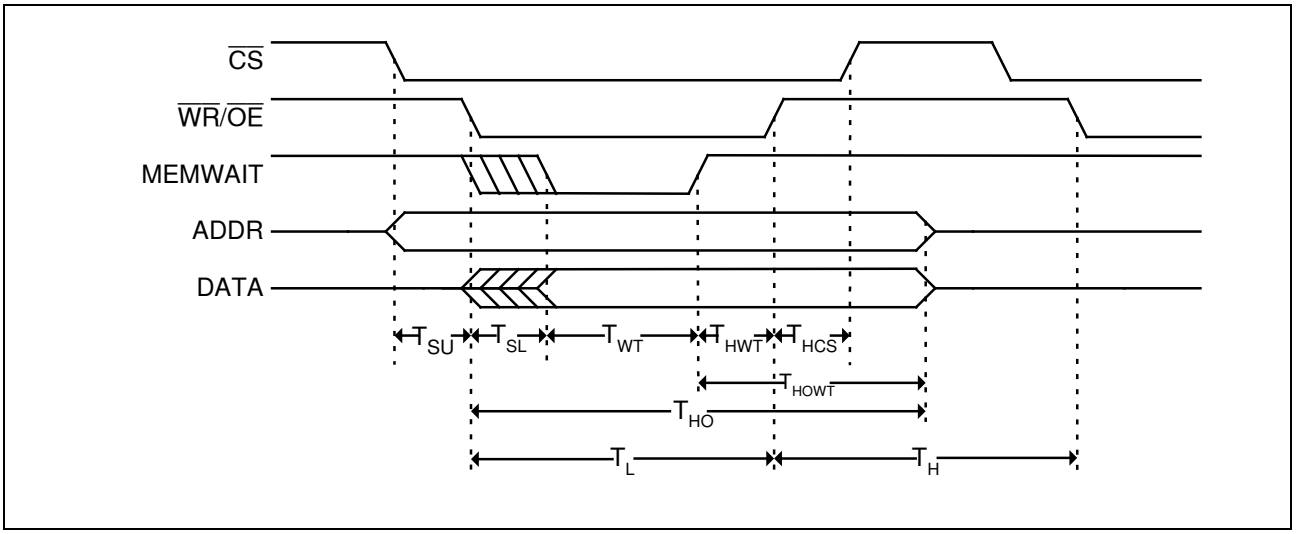

Figure 8: Host Interface Timing Diagram

Name	Description	Requirement	Min	Max
T_{SU}	$\overline{CS}$ and ADDR setup time	$\overline{CS}$ and ADDR must be stable on or before the falling edge of $\overline{WR}/\overline{OE}$.	0 ns	–
T_{SL}	Output settling time	The maximum amount of time that it will take the MEMWAIT, or DATA when there is no MEMWAIT, outputs to become stable after the falling edge of $\overline{WR}/\overline{OE}$.	–	13.7 ns
T_{WT}	Maximum wait time	The maximum amount of time that the MEMWAIT output will held asserted.	–	17 ck
T_{HWT}	Wait hold time	The minimum amount of time that the $\overline{WR}/\overline{OE}$ input must be held past the de-assertion of MEMWAIT.	10 ns	–
T_{HCS}	$\overline{CS}$ hold time	The $\overline{CS}$ input must be stable low for the entire duration of the $\overline{WR}/\overline{OE}$ low cycle.	0 ns	–
T_{HO}	ADDR and DATA hold time	The ADDR and DATA inputs must be stable for no less than this amount of time after the falling edge of $\overline{WR}$.	2.5 ck	–
T_L	$\overline{WR}/\overline{OE}$ min low pulse	The minimum amount of time that the $\overline{WR}/\overline{OE}$ inputs must be held low.	2 ck	–
T_H	$\overline{WR}/\overline{OE}$ min high pulse	The minimum amount of time that the $\overline{WR}/\overline{OE}$ inputs must be held high.	2 ck	–

Note: On read cycles when MEMWAIT is asserted the DATA outputs will be valid before the de-assertion of MEMWAIT.

5.1.1 Synchronous Mode Timing

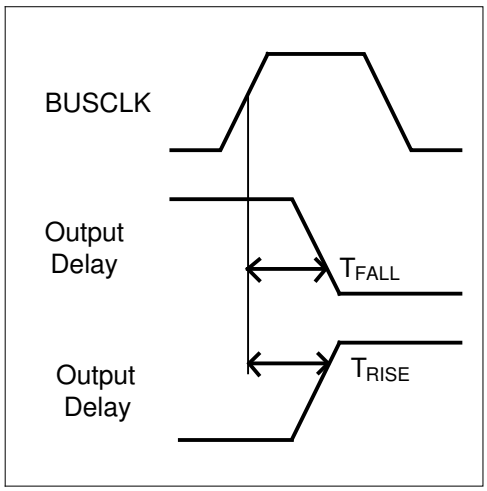

Figure 9: Host Bus Output Timing Diagram

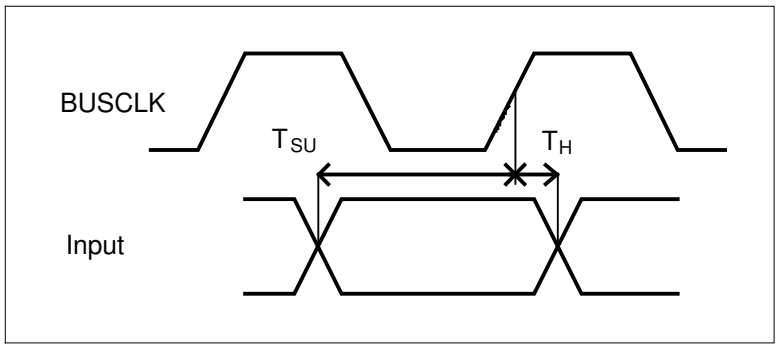

Figure 10: Host Bus Input Timing Diagram

Parameter	Symbol	Min	Nom	Max	Unit
Input Setup Time	T_{SU}	6	–	–	ns
Input Hold Time	T_H	6	–	–	ns
Output Fall Delay	T_{FALL}	–	–	8	ns
Output Rise Delay	T_{RISE}	–	–	8	ns
CSB min low	P_{WL}	1	–	–	clk
CSB min high	P_{WH}	2	–	–	clk

5.1.2 Bus Clock Timing

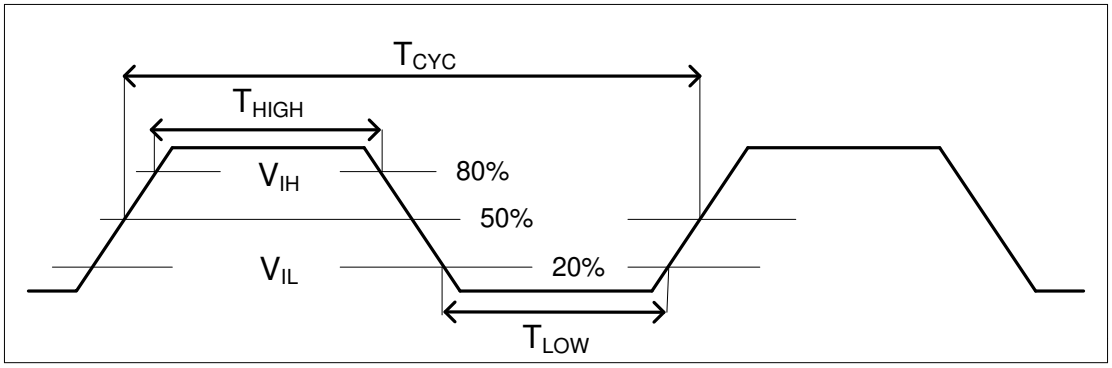

Figure 11: Bus Clock Timing

Parameter	Symbol	Sync 50		Async 100		Units
		Min	Max	Min	Max	
BUSCLK Cycle Time	T_{CYC}	20	–	10	–	ns
BUSCLK Frequency	–	–	50	–	100	MHz
BUSCLK High Time	T_{HIGH}	8	–	3	–	ns
BUSCLK Low Time	T_{LOW}	8	–	3	–	ns
BUSCLK Slew Rate	–	1	3	1	3	V/ns

5.1.3 Reset Timing

Parameter	Symbol	Min	Nom	Max	Units
RESETB Minimum Duration	T_{RESET}	1	–	–	clocks

6 Functional Description

6.1 Internal Block Diagrams

6.1.1 Internal Digital Block

Figure 12 presents an overview of the functional layers of the 78Q8430. On the left side are the signals, which connect to the GBI bus. On the upper and middle right, the blocks that implement the MAC side of the MII are shown. These blocks are connected to the embedded PHY. On the lower right, connections to the EEPROM are shown.

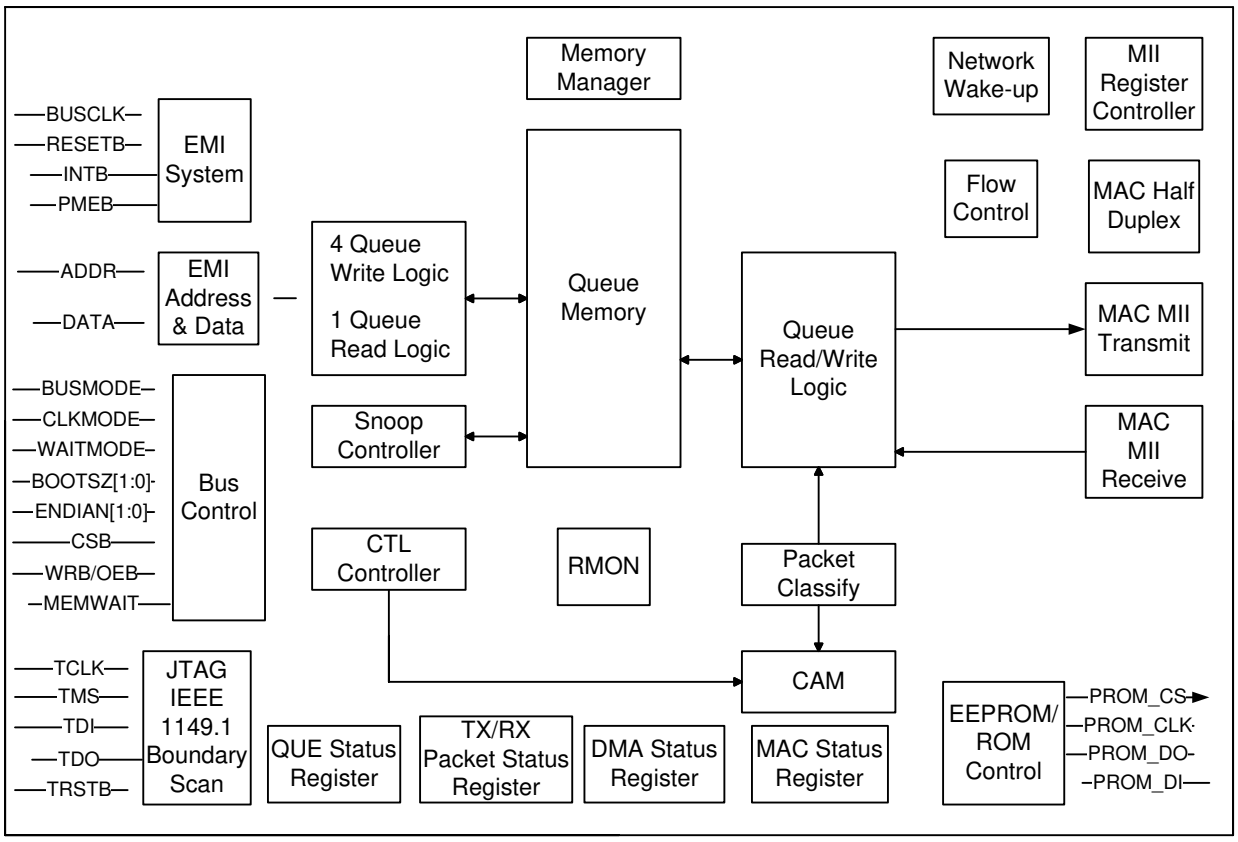

Figure 12: Internal Digital Block Diagram

6.1.2 Internal PHY

Figure 13 shows the functional blocks of the internal 78Q8430 PHY. The signals shown on the left side are the internal MII signals to the MAC. These signals are multiplexed with their respective external pins for use with an external PHY device. The 78Q8430 is not a two-port device. Only one PHY interface can be operational.