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SPS-1616™ Datasheet

Secure Packet Switch

April 4, 2016

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About This Document

Introduction

The *SPS-1616 Datasheet* provides hardware information about the SPS-1616, such as electrical and packaging characteristics. It is intended for hardware engineers who are designing system interconnect applications with the device.

Additional Resources

The *SPS-1616 User Manual* describes the functionality and configuration capabilities of the device. In addition, there are many other resources available that support the SPS-1616. For more information, please contact IDT for support.

Document Conventions and Definitions

This document uses the following conventions and definitions:

- To indicate signal states:
  - Differential signals use the suffix “_P” to indicate the positive half of a differential pair.
  - Differential signals use the suffix “_N” to indicate the negative half of a differential pair.
  - Non-differential signals use the suffix “_N” to indicate an active-low state.
- To define buses, the most significant bit (MSB) is on the left and least significant bit (LSB) is on the right. No leading zeros are included.
- To represent numerical values, either decimal, binary, or hexadecimal formats are used. The binary format is as follows: 0bDDD, where “D” represents either 0 or 1; the hexadecimal format is as follows: 0xDD, where “D” represents the hexadecimal digit(s); otherwise, it is decimal.
- Unless otherwise denoted, a byte refers to an 8-bit quantity; a word refers to a 32-bit quantity, and a double word refers to an 8-byte (64-bit) quantity. This is in accordance with RapidIO convention.
- A bit is set when its value is 0b1. A bit is cleared when its value is 0b0.
- A read-only register, bit, or field is one that can be read but not modified.

This symbol indicates important configuration information or suggestions.

This symbol indicates procedures or operating levels that may result in misuse or damage to the device.

Revision History

April 4, 2016

- Added an R_X2 symbol to Table 20
- Added an HMG part number to Ordering Information

July 25, 2013

- Updated Heat Sink Requirement and Analysis
- Completed several minor improvements

June 12, 2013

- Updated the note associated with VDD3A (pin T18)

June 8, 2012

- Changed the maximum 3.3V supply requirement to 3.47V in Table 6 and note 2 below the table
- Updated the REF_CLK parameter in Table 29 to +/-50 ppm
- Added two cautionary notes about lane reordering to Pin Listing

December 9, 2011

- Loosened the Clock Input signal rise/fall minimum time specification
- Added an additional note to the power sequencing requirements

October 27, 2011

SPS-1616 Datasheet

1 Device Overview

The SPS-1616 (part number 80HSPS1616) is a *RapidIO Specification (Rev. 2.1)* compliant Secure Packet Switch whose functionality is central to routing packets for distribution among DSPs, processors, FPGAs, other switches, or any other RapidIO-based devices. It can also be used in RapidIO backplane switching. The SPS-1616 supports Serial RapidIO (S-RIO) packet switching (unicast, multicast, and an optional broadcast) from any of its 16 input ports to any of its 16 output ports.

2 Features

- RapidIO ports
  - 16 bidirectional S-RIO lanes
  - Port widths of 1x, 2x, and 4x allow up to 20 Gbps per port
  - Port speeds selectable: 6.25, 5, 3.125, 2.5, or 1.25 Gbaud
  - Support Level I defined short or long haul reach, and Level II defined short-, medium-, or long-run reach for each PHY speed
  - Error Management Extensions support
  - Software-assisted error recovery, supporting hot swap
- I^2C Interfaces
  - Provides I^2C port for maintenance and error reporting
  - Master or Slave operation
  - Master allows power-on configuration from external ROM
  - Master mode configuration with external image compressing and checksum
- Switch
  - 80 Gbps peak throughput
  - Non-blocking data flow architecture
  - Configurable for Cut-Through or Store-and-Forward data flow
  - Very low latency for all packet lengths and load conditions
  - Internal queuing buffer and retransmit buffer
  - Standard transmitter- or receiver-controlled flow control
  - Global routing or Local Port routing capability
  - Supports up to 40 simultaneous multicast masks, with broadcast
  - Performance monitoring counters for performance and diagnostics analysis. Per input port and output port counters
- SerDes
  - Transmitter pre-emphasis and drive strength + receiver equalization provides best possible signal integrity
  - Embedded PRBS generation and detection with programmable polynomials support Bit Error Rate testing
- Security Functions
  - Optional encrypt and decrypt mode on four S-RIO ports secures data (see Figure 3)
  - Crypto units compliant with AES-128 CTR (FIPS Pub 197, NIST SP800-38A)
  - Port Disable pins allow hardware enable/disable of all S-RIO ports

- Additional Information
  - Packet Trace/Mirror. Each input port can copy all incoming packets matching user-defined criteria to a “trace” output port.
  - Packet Filter. Each input port can filter (drop) all incoming packets matching user-defined criteria.
  - Device configurable through any of S-RIO ports, I^2C, or JTAG
  - Full JTAG Boundary Scan Support (IEEE1149.1 and 1149.6)
  - Lidless FCBGA Package: 21 x 21 mm, 1.0 mm ball pitch
- Specification Compliancy
  - *RapidIO Specification (Rev. 2.1), Part 1: Input/Output Logical Specification, 08/2009, RTA*
  - *RapidIO Specification (Rev. 2.1), Part 2: Message Passing Logical Specification, 08/2009, RTA*
  - *RapidIO Specification (Rev. 2.1), Part 3: Common Transport Specification, 08/2009, RTA*
  - *RapidIO Specification (Rev. 2.1), Part 6: LP-Serial Physical Layer Specification, 08/2009, RTA*
  - *RapidIO Specification (Rev. 2.1), Part 7: System and Device Interoperability Specification, 08/2009, RTA*
  - *RapidIO Specification (Rev. 2.1), Part 8: Error Management Extensions Specification, 08/2009, RTA*
  - *RapidIO Specification (Rev. 2.1), Part 9: Flow Control Logic Layer Extensions Specification, 08/2009, RTA*
  - *RapidIO Specification (Rev. 2.1), Part 11: Multicast Extensions Specification, 08/2009, RTA*
  - *RapidIO Specification (Rev. 2.1), Annex I: Software/System Bring Up Specification, 08/2009, RTA*
  - *IEEE Std 1149.1-2001 IEEE Standard Test Access Port and Boundary-Scan Architecture*
  - *IEEE Std 1149.6-2003 IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks*
  - *The I^2C-BUS Specification* (v 2.1), January 2000, Philips

3 Block Diagram

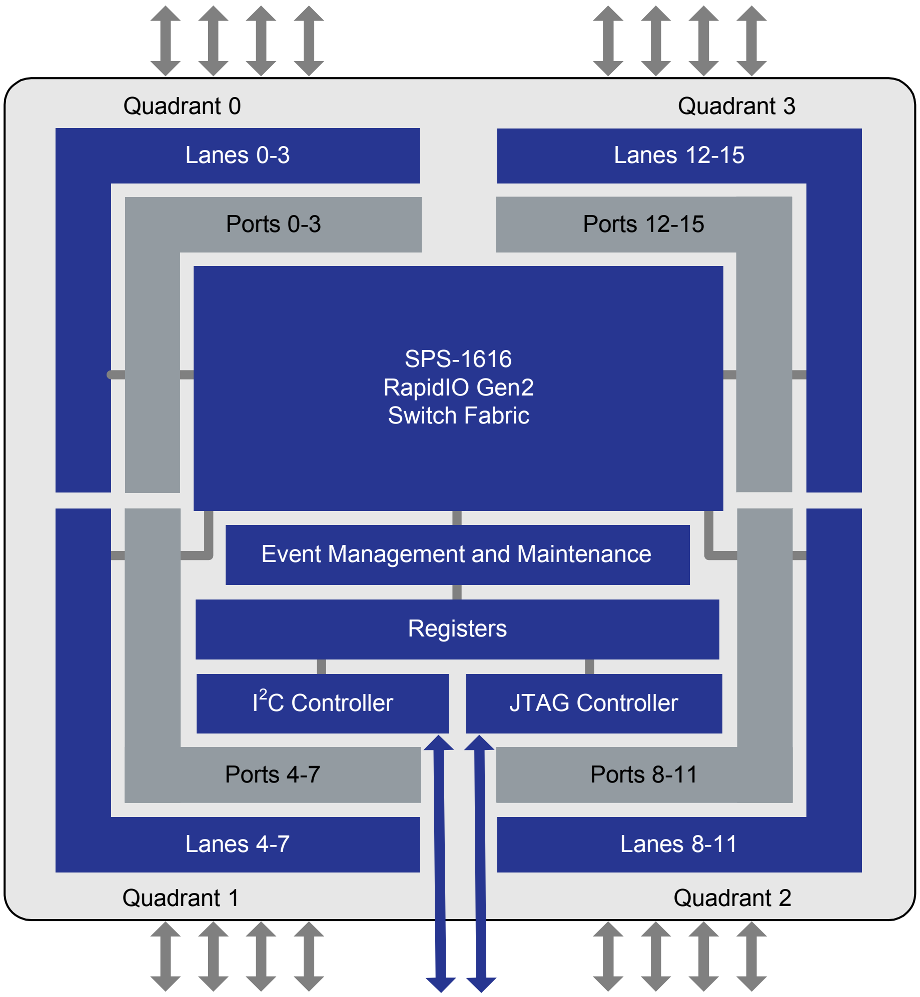

Figure 1: Block Diagram

4 Device Description

The SPS-1616 is a S-RIO-compliant performance-optimized switch. This device is ideally suited for intensive processing applications which require a multiplicity of DSPs, CPUs, and / or FPGAs working together in a cluster. Its very low latency, reliable packet-transfer, and high throughput make it ideal in embedded applications including communications, imaging, or industrial controls. A switched S-RIO architecture allows a flat topology with true peer-to-peer communications. It supports four standard RapidIO levels of priority, and can unicast, multicast, or broadcast packets to destination ports. With link rates to 6.25 Gbaud and transmitter pre-emphasis and receiver equalization, the device can provide up to 20 Gbps per port across 100 cm (40 inches) of FR4 with 2 connectors. This makes the device ideally suited for communicating across backplanes or cables.

The SPS-1616 receives packets from up to 16 ports. The SPS-1616 offers full support for switching as well as enhanced functions:

1. **Switching —** All packets are switched in accordance with the *RapidIO Specification (Rev. 2.1)*, with packet destination IDs (destID) determining how the packet is routed.

   Four main switching options exist:

   a. Unicast: Packets are sent according to the packet's destID to a single destination port in compliance with the *RapidIO Specification (Rev. 2.1)*.

   b. Multicast: Packets with a destID pointing to a multicast mask will multicast to all destination ports provided by the multicast mask. Multicasting is performed in compliance with the *RapidIO Specification (Rev. 2.1)*.

c. Maintenance packets: In compliance with the *RapidIO Specification (Rev. 2.1)*, maintenance packets with hop_count > 0 pass through the switch. Maintenance packets with hop_count = 0 will operate on the switch.

d. Broadcast: Each multicast mask can be configured so all output ports, including the source port, are included among the destination ports for that multicast operation. This feature is IDT-specific.

The SPS-1616 supports a peak throughput of 80 Gbps which is the line rate for 16 Ports in 1x configuration, (each at 5.0 Gbaud = 6.25 Gbaud minus the S-RIO defined 8b/10b encoding), and switches dynamically in accordance with the packet headers and priorities.

2. **Enhanced functions —** Enhanced features are provided for support of system debug. These features which are optional for the user consist of following functions:

a. Packet Trace: The Packet Trace feature provides at-speed checking of the first 160 bits (header plus a portion of any payload) of every incoming packet against user-defined comparison register values. The trace feature is available on all S-RIO ports, each acting independently from one another. If the trace feature is enabled for a port, every incoming packet is checked for a match against up to four comparison registers. If a match occurs, either of two possible user-defined actions may occur:

i) Not only does the packet route normally through the switch to its appropriate destination port, but this same packet is copied to a “debug port” or “trace port.” The trace port itself can be any of the standard S-RIO ports. The port used for the trace port is defined by the user through simple register configuration.

ii) The packet is dropped. If there is no match, the packets route normally through the switch with no action taken. The Packet Trace feature can be used during system bring-up and prototyping to identify specific packet types of interest to the user. It might be used in security applications, where packets must be checked for either correct or incorrect tags in either of the header or payload. Identified (match) packets are then routed to the trace port for receipt by a host processor, which can perform an intervention at the software level.

b. Port Loopback: The SPS-1616 offers internal loopback for each port that can be used for system debug of the high-speed S-RIO ports. By enabling loopback on a port, packets sent to the port’s receiver are immediately looped back at the physical layer to the transmitter - bypassing the higher logical or transport layers.

c. Broadcast: The device switching operation supports broadcast traffic (any input port to all output ports).

d. Security functions: The aforementioned packet trace / filter capabilities allow packets matching trace criteria to be blocked at the input port. This function can, for example, allow untrusted (unknown source or destination) packets to be filtered, malicious or errant maintenance packets to be filtered, or boot packets to be identified to pass to a slave device.

The SPS-1616 can be programmed through any one or combination of S-RIO, I^2C, or JTAG. Note that any S-RIO port can be used for programming. The SPS-1616 can also configure itself on power-up by reading directly from EPROM over I^2C in master mode.

5 Functional Overview

The SPS-1616 is optimized for line card and backplane switching. Its primary function is to switch data plane and control plane data packets using S-RIO between a set of devices that reside on the same line card. In addition, it can bridge communications between multiple on-board (or local) devices and a set of external line cards by providing long run RapidIO backplane interconnects. In this manner, for example, the device can serve as a switch between a set of RF cards and a set of RapidIO based DSPs in a wireless basestation.

The SPS-1616 supports packet switching from its 16 RapidIO ports. Packets can be unicast, multicast, or broadcast. The encoded data rate for each of the lanes are configurable to either 1.25, 2.5, 3.125, 5, or 6.25 Gbaud. The device supports lane groupings such that 1x, 2x, and 4x operation is provided, as defined in the *RapidIO Specification (Rev. 2.1)*.

The SPS-1616 supports the reception of S-RIO maintenance packets (type 8) which are directed to it (that is, a hop count of 0). The device can properly process and forward received maintenance packets with a hop count > 0 as defined in the *RapidIO Specification (Rev. 2.1)*. With the exception of maintenance packets, received packets are transmitted unmodified.

The SPS-1616 supports four priority levels plus Critical Request Flow (CRF), as defined in the *RapidIO Specification (Rev. 2.1), Part 6*. It is programmable by all of the following: S-RIO ports, I^2C, and JTAG Interface.

From a switching perspective the SPS-1616 functions statically. As such, all input to output port mappings are configurable through registers. Unless register configurations are changed, the input to output mappings remains static regardless of the received data. The switching functionality does not dynamically “learn” which destIDs are tied to a port endpoint by examining S-RIO header fields and dynamically updating internal routing tables.

The SPS-1616 supports “Store and Forward” or “Cut-Through” packet forwarding (for more information, see the “Switch Fabric” chapter in the *SPS-1616 User Manual*).

6 Interface Overview

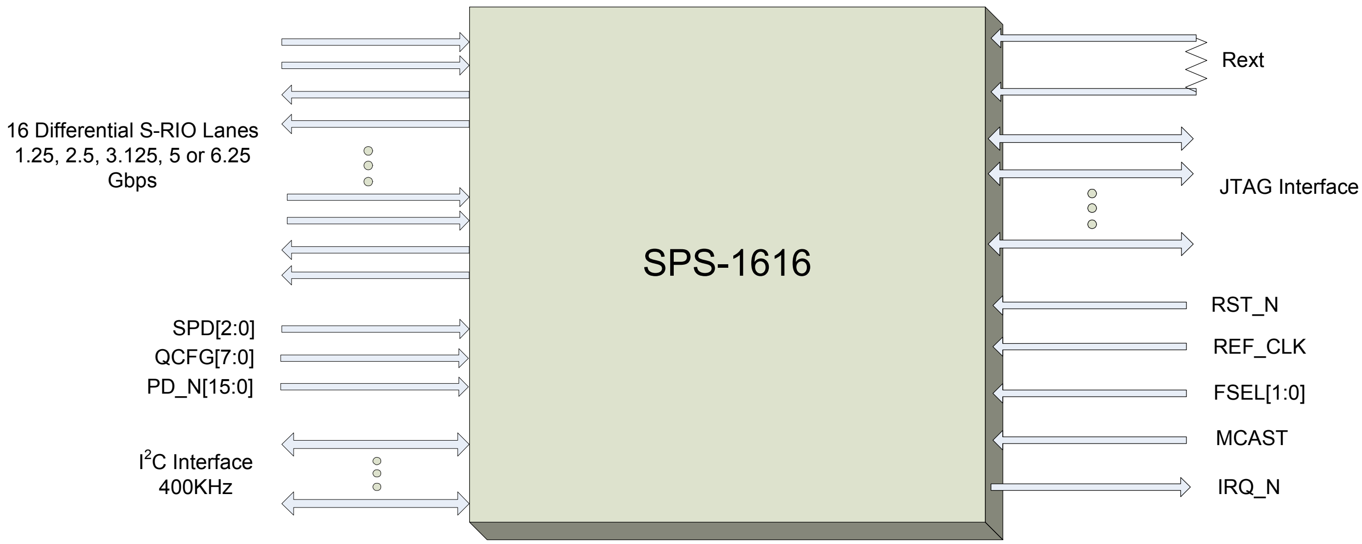

Figure 2: SPS-1616 Interfaces

S-RIO Ports

The S-RIO ports are the main communication ports on the chip. These ports are compliant with the *RapidIO Specification (Rev. 2.1)*. For more information, see the *RapidIO Specification (Rev. 2.1)*.

The device provides up to 16 S-RIO lanes. The encoded data rate for each of the lanes is configurable to either 1.25, 2.5, 3.125, 5, or 6.25 Gbaud as defined in the *RapidIO Specification (Rev. 2.1), Part 6*.

I^2C Bus

This interface can be used instead of the standard S-RIO or JTAG ports to program the chip and to check the status of registers - including the error reporting registers. It is fully compliant with the I^2C specification, it supports master and slave modes and supports both Fast and Standard-mode buses [1]. For more information, see I^2C Bus.

JTAG TAP Port

This TAP interface is IEEE1149.1 (JTAG) and 1149.6 (AC Extest) compliant [11, 12]. It can be used instead of the standard S-RIO or I^2C ports to program the chip and to check the status of registers - including the error reporting registers. It has 5 pins. For more information, see JTAG Interface.

Interrupt (IRQ_N)

An interrupt output is provided in support of Error Handling functionality. This output can flag a host processor if error conditions occur within the device. For more information, see the “Event Management" chapter in the *SPS-1616 User Manual*.

Reset (RST_N)

A single Reset pin is used for full reset of the SPS-1616, including setting all registers to power-up defaults. For more information, see the "Reset and Initialization" chapter in the *SPS-1616 User Manual*.

Clock (REF_CLK_P/N)

The single system clock (REF_CLK_P/N) is a 156.25-MHz differential clock.

Rext (REXT_N/P)

These pins establish the drive bias on the SerDes output. An external bias resistor is required. The two pins must be connected to one another with a 9.1k Ohm resistor. This provides robust SerDes stability across process and temperature.

Speed Select (SPD[2:0])

These pins define the S-RIO port speed at RESET for all ports. SPD[2:0] can be configured as follows:

- 000 = 1.25 Gbaud
- 001 = 2.5 Gbaud
- 01X = 5 Gbaud
- 100 = Reserved
- 101 = 3.125 Gbaud
- 11X = 6.25 Gbaud

For more information, see Speed Select Pins SPD[2:0].

Quadrant Config (QCFG[7:0])

These pins define the S-RIO port width (x1, x2, x4) at RESET for all ports. QCFG[1:0] defines port width for Quadrant 0, QCFG[3:2] defines port width for Quadrant 1, QCFG[5:4] defines port width for Quadrant 2, and QCFG[7:6] defines port width for Quadrant 3. For more information, see Quadrant Configuration Pins QCFG[7:0].

Port Disable (PD[15:0]_N)

These pins define the active state of the specific port at RESET. PD15_N defines port 15 and PD0_N defines port 0.

Frequency Select (FSEL[1:0])

FSEL1 pin defines the input reference clock, and FSEL0 pin defines the internal clock frequency, full or half rate.

Multicast (MCAST)

The Multicast-Event Control Symbol Trigger (MCAST) pin provides an optional mechanism to trigger the generation of a Multicast-Event Control Symbol. The multicast-event control symbol allows a user-defined system event to be multicast throughout a system (for example, synchronously reset a system or its internal timers).

7 Configuration Pins

Speed Select Pins SPD[2:0]

There are three port-speed selection pins that select the initial speed of the RapidIO ports (see Table 1). The RESET setting can be overridden by programming the PLL n Control 1 Register and Lane n Control Register (for more information, see “Lane and Port Speeds” in the *SPS-1616 User Manual*).

Table 1 Port Speed Selection Pin Values

Value on the Pins (SPD2, SPD1, SPD0)	Port Rate (Gbaud)
000	1.25
001	2.5
01X	5.0
100	Reserved
101	3.125
11X	6.25

Quadrant Configuration Pins QCFG[7:0]

There are eight quadrant configuration selection pins, QCFG[7:0], or two pins per quadrant. These pins select the device's RapidIO port width, and its lane to port mapping, as displayed in the following figures.

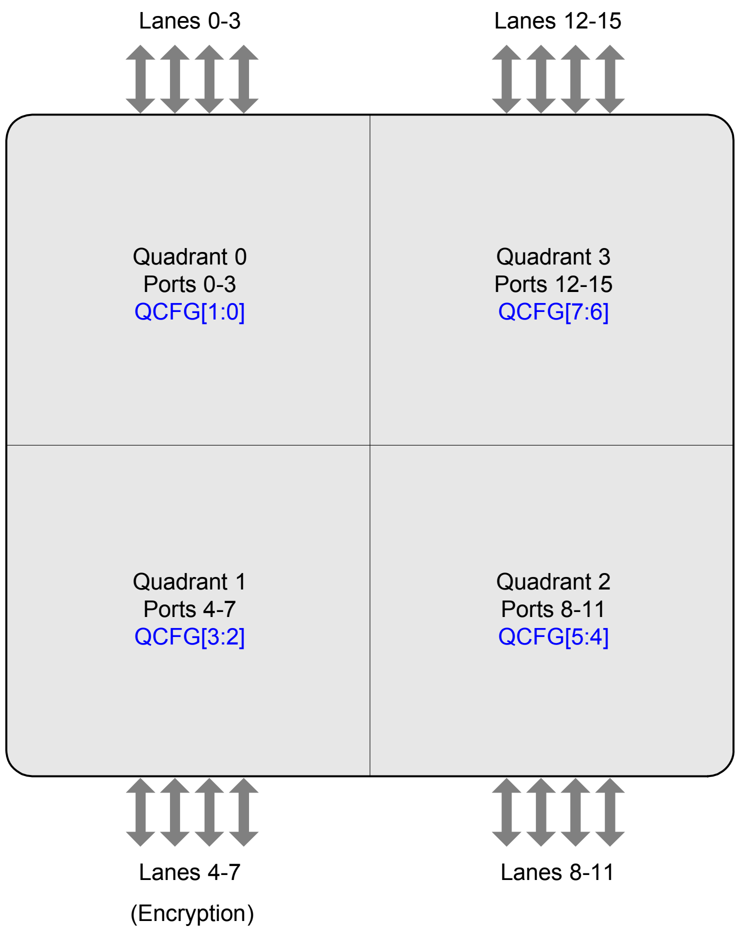

Figure 3: Quadrant Configuration using QCFG[7:0]

Figure 4 shows the relationship between the Quadrant, Port, and Lane settings, based on the configuration of the device's QCFG[1:0] pins.

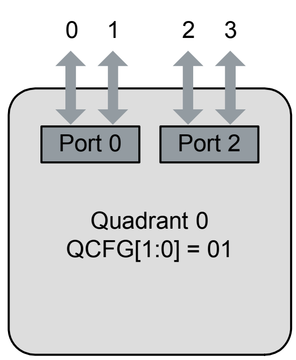

Figure 4: Quadrant 0 Configuration Example — QCFG[1:0] = 01

7 Configuration Pins

The following table describes the complete lane-to-port mapping options for the SPS-1616 based on the setting of the QCFG[7:0] pins.

Table 2 Lane to Port Mapping

Quadrant/ Quad	QCFG Pins	QCFG Pin Setting	PLL	Port Width	Mapping	
					Port	Lane(s)
0	QCFG[1:0]	00	0, 4	4x	0	0–3
				-	1, 2, 3	-
		01	0, 4	2x	0	0–1
				2x	2	2–3
			-	-	1, 3	-
		10	0, 4	2x	0	0–1
				1x	2	2
				1x	3	3
				-	1	-
		11	0, 4	1x	0	0
				1x	1	1
				1x	2	2
				1x	3	3
1	QCFG[3:2]	00	1, 5	4x	4	4–7
				-	5, 6, 7	-
		01	1, 5	2x	4	4–5
				2x	6	6–7
			-	-	5, 7	-
		10	1, 5	2x	4	4–5
				1x	6	6
				1x	7	7
				-	5	-
		11	1, 5	1x	4	4
				1x	5	5
				1x	6	6
				1x	7	7

Table 2 Lane to Port Mapping (Continued)

Quadrant/ Quad	QCFG Pins	QCFG Pin Setting	PLL	Port Width	Mapping	
					Port	Lane(s)
2	QCFG[5:4]	00	2, 6	4x	8	8–11
				-	9, 10, 11	-
		01	2, 6	2x	8	8–9
				2x	10	10–11
			-	-	9, 11	-
		10	2, 6	2x	8	8–9
				1x	10	10
				1x	11	11
				-	9	-
		11	2, 6	1x	8	8
				1x	9	9
				1x	10	10
				1x	11	11
3	QCFG[7:6]	00	3, 7	4x	12	12–15
				-	13, 14, 15	-
		01	3, 7	2x	12	12–13
				2x	14	14–15
			-	-	13, 15	-
		10	3, 7	2x	12	12–13
				1x	14	14
				1x	15	15
				-	13	-
		11	3, 7	1x	12	12
				1x	13	13
				1x	14	14
				1x	15	15

8 Absolute Maximum Ratings

Table 3 Absolute Maximum Rating[1]

Symbol	Parameter	Rating		Unit
		Minimum	Maximum	
V_{DD3}	V_{DD3} voltage with respect to GND	-0.5	3.6	V
V_{DD}	V_{DD} voltage with respect to GND	-0.5	1.2	V
V_{DDT}	V_{DDT} voltage with respect to GNDS (V_{DDS} = 0V)	-0.5	1.2	V
	V_{DDT} voltage with respect to GNDS (V_{DDS} = 1.0V)	-0.5	1.4	V
V_{DDA} and V_{DDS}	V_{DDA} AND V_{DDS} voltage with respect to GNDS	-0.5	1.2	V
T_{BIAS}[2]	Temperature under bias	-55	125	C
T_{STG}	Storage temperature	-65	150	C
T_{JN}	Junction temperature	-	125	C
I_{OUT} (for V_{DD3} = 3.3V)	DC output current	-	30	mA
I_{OUT} (for V_{DD3} = 2.5V)	DC output current	-	30	mA

Notes:

1. Stresses greater than those listed under Absolute Maximum Ratings can cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect reliability.
2. Ambient Temperature under DC Bias, no AC conditions. Can not exceed maximum Junction temperature.
3. IDT recommends not to exceed ripple voltage of 50 mV max on $V_{DDT}/V_{DDS}/V_{DDA}$ and 50 mV/100 mV (maximum) on V_{DD}/V_{DD3} respectively.

9 Recommended Operating Conditions

Table 4 Recommended Operating Conditions[1]

Symbol[2]	Parameter	Rating		Unit
		Minimum	Maximum	
V_{DD3}-supplied interfaces[3 5]	Input or I/O terminal voltage with respect to GND	-0.3	V_{DD3} + 0.3	V
V_{DD}	V_{DD} voltage with respect to GND	0.95	1.05	V
V_{DDA} and V_{DDS}[4]	V_{DDA} AND V_{DDS} voltage with respect to GNDS	0.95	1.05	V
V_{DDT}	V_{DDT} voltage with respect to GNDS	1.14	1.26	V
V_{DD3} and V_{DD3A}	V_{DD3} voltage (3.3 V) with respect to GND	3.14	3.47	V
	V_{DD3} voltage (2.5 V) with respect to GND	2.4	2.6	V

Notes:

1. The following power-up sequence is necessary in order for the device to function properly: The SerDes voltage (V_{DDS}) needs to power-up first followed by SerDes voltage (V_{DDT}). V_{DD}, V_{DDA}, and $V_{DD3(a)}$ can be powered up in any order. The device is not sensitive to supply rise and fall times, and thus these are not specified.
2. V_{DDT}, V_{DDA}, and V_{DDS} share a common ground (GNDS). Core supply and ground are V_{DD} and GND respectively.
3. V_{DD3} can be operated at either 3.3V or 2.5V simply by providing that supply voltage. For those interfaces operating on this supply, this datasheet provides input and output specifications at each of these voltages.
4. V_{DDS} and V_{DDA} can be tied to a common power plane. V_{DD} (core, digital supply) should have its own power plane. If the same voltage regulator is used for V_{DDS}/V_{DDA} and V_{DD}, the V_{DDS}/V_{DDA} plane should be isolated to prevent noise from the V_{DD} plane to couple onto the V_{DDS}/V_{DDA} plane.
5. This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. The voltage on any Input or I/O pin cannot exceed its corresponding supply voltage during power supply ramp up.

10 AC Test Conditions

Table 5 AC Test Conditions (V_{DD3} = 3.3V / 2.5V): JTAG, I^2C, RST

Input Pulse Levels	GND to 3.0V / GND to 2.4V
Input Rise / Fall Times	2 ns
Input Timing Reference Levels	1.5V / 1.25V
Output Reference Levels	1.5V / 1.25V
Output Load	See Figure 5

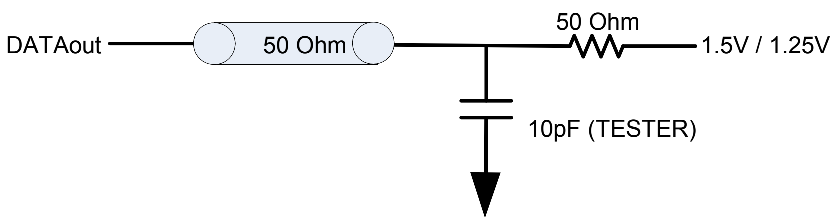

Figure 5: AC Output Test Load (JTAG)

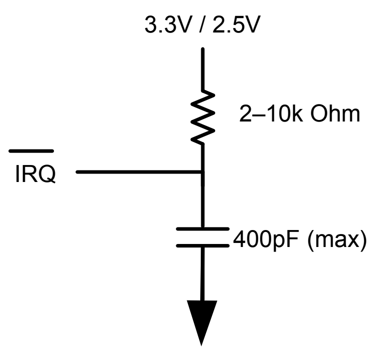

Figure 6: AC Output Test Load (IRQ)

Note: The IRQ_N pin is an open-drain driver. IDT recommends a weak pull-up resistor (2-10k Ohm) be placed on this pin to V_{DD3}.

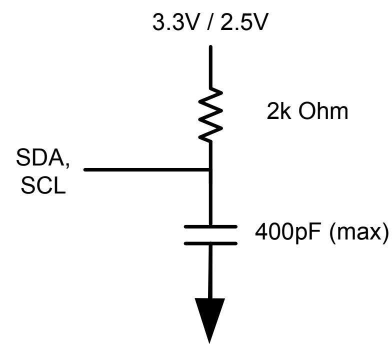

Figure 7: AC Output Test Load (I^2C)

Note: The SDA and SCL pins are open-drain drivers. For information on the appropriate selection of pull-up resistors for each, see the *Philips I^2C Specification* [1].

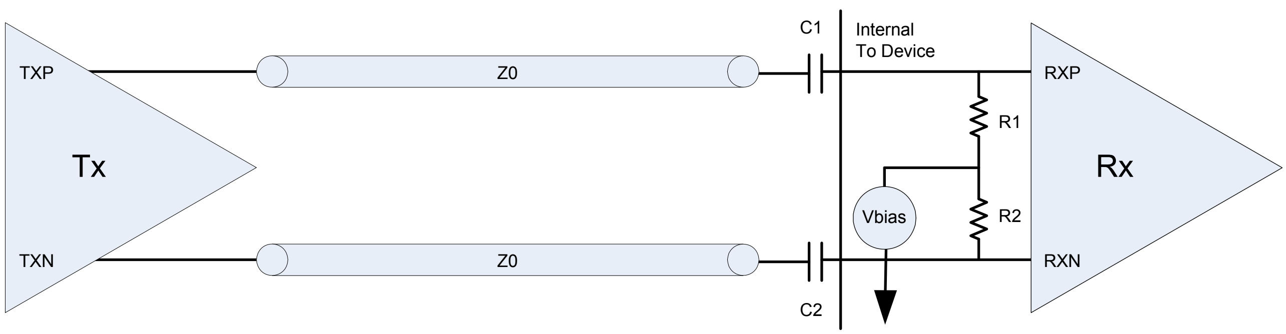

Figure 8: S-RIO Lanes Test Load

The characteristic impedance Z0 should be designed for 100 Ohms differential. An inline capacitor C1 and C2 at each input of the receiver provides AC-coupling and a DC-block. The IDT recommended values are 75 - 200nF for each. Thus, any DC bias differential between the two devices on the link is negated. The differential input resistance at the receiver is 100 Ohms, as defined in the *RapidIO Specification (Rev. 2.1)*. Thus, R1 and R2 are 50 Ohms each. Note that V_{BIAS} is the internal bias voltage of the device's receiver.

11 Power Consumption

Heat generated by the packaged IC and increase in voltage supplies have an adverse effect on the device power consumption. In order to control its functional and maximum design temperature limits, IDT recommends at a minimum to have adequate airflow. The typical and maximum power numbers provided below take into consideration the following characteristics, Theta Ja = 11°C/W with 2m/s of airflow. For more information on thermal analysis, see Thermal Characteristics.

An estimate of the device power figure for an application usage can be determined by using the device's "Power Calculator" modeling tool available on the IDT secure site.

The *typical* power condition refers to nominal voltage for all rails and is 4.2W in total for all ports enabled as 16 1x at 6.25 Gbaud under 50% switch load.

The *maximum* power condition refers to maximum voltage for all rails and is 7.2W in total for all ports enabled as 16 1x at 6.25 Gbaud under 100% switch load.

Table 6 Power Consumption

Line Rate Gbaud	Current/ Power	Power Supplies											
		Core Supply (V_{DD})		SerDes Supply (V_{DDS})		SerDes Supply Xmt (V_{DDT})		PLL Supply (V_{DDA})		I/O Supply (V_{DD3})		Total	
		Typ 1.0V	Max 1.05V	Typ 1.0V	Max 1.05V	Typ 1.2V	Max 1.26V	Typ 1.0V	Max 1.05V	Typ 3.3V	Max 3.47V	Typ Power	Max Power
6.25	Amps	2.53	4.73	0.84	1.00	0.46	0.55	0.27	0.30	0.015	0.032		
	Watts	2.53	4.97	0.84	1.05	0.55	0.69	0.27	0.32	0.050	0.12	4.24	7.15
5.0	Amps	2.43	4.52	0.76	0.90	0.46	0.55	0.27	0.30	0.015	0.032		
	Watts	2.43	4.75	0.76	0.95	0.55	0.69	0.27	0.32	0.050	0.12	4.06	6.83
3.125	Amps	2.36	4.37	0.69	0.82	0.46	0.55	0.27	0.30	0.015	0.032		
	Watts	2.36	4.59	0.69	0.86	0.55	0.69	0.27	0.32	0.050	0.12	3.92	6.58
2.5	Amps	2.31	4.28	0.65	0.77	0.46	0.55	0.27	0.30	0.015	0.032		
	Watts	2.31	4.49	0.65	0.81	0.55	0.69	0.27	0.32	0.050	0.12	3.83	6.43
1.25	Amps	2.27	4.15	0.58	0.70	0.46	0.55	0.27	0.30	0.015	0.032		
	Watts	2.27	4.36	0.58	0.74	0.55	0.69	0.27	0.32	0.050	0.12	3.72	6.23

Notes:

1. Typical conditions: V_{DD}, V_{DDS}, V_{DDA} = 1.0V, V_{DDT} = 1.2V, V_{DD3} = 3.3V at Ambient Temperature of 60°C (Theta Ja = 11°C/W @ 2m/s airflow).
2. Maximum conditions: V_{DD}, V_{DDS}, V_{DDA} = 1.05V, V_{DDT} = 1.26V, V_{DD3} = 3.47V at max Junction Temperature (125°C).

12 I2C Bus

The SPS-1616 is compliant with the I2C specification [1]. This specification provides the functional information and electrical specifications associated with the I2C bus, including signaling, addressing, arbitration, AC timing, and DC specifications. The SPS-1616 supports both master mode and slave mode, which is selected by MM_N pin.

The I2C bus consists of the Serial Data (SDA) and Serial Clock (SCL) pins. It can be used to attach a CPU or a configuration memory. The I2C Interface supports Fast/Standard (F/S) mode (400/100 kHz).

I2C Master Mode and Slave Mode

The SPS-1616 support both master mode and slave mode. The operating mode is selected by the MM_N static configuration pin. For more information, see Signaling.

I2C Device Address

The device address for the SPS-1616 is fully pin-defined by 10 external pins while in slave mode. This provides full flexibility in defining the slave address to avoid conflicting with other I2C devices on a bus. The SPS-1616 can be operated as either a 10-bit addressable device or a 7-bit addressable device based on another external pin, address select (ADS). If the ADS pin is tied to V_{DD3}, then the SPS-1616 operates as a 10-bit addressable device and the device address will be defined as ID[9:0]. If the ADS pin is tied to GND, then the SPS-1616 operates as a 7-bit addressable device with the device address defined by ID[6:0]. The addressing mode must be established at power-up and remain static throughout operation. Dynamic changes will result in unpredictable behavior.

Table 7 I2C Static Address Selection Pin Configuration

Pin	I2C Address Bit (pin_addr)
ID9	9 (don't care in 7-bit mode)
ID8	8 (don't care in 7-bit mode)
ID7	7 (don't care in 7-bit mode)
ID6	6
ID5	5
ID4	4
ID3	3
ID2	2
ID1	1
ID0	0

All of the SPS-1616's registers are addressable through I2C. These registers are accessed using 22-bit addresses and 32-bit word boundaries through standard reads and writes. These registers also can be accessed through the S-RIO and JTAG Interfaces.

Signaling

Communication with the SPS-1616 on the I²C bus follows these three cases:

1. Suppose a master device wants to send information to the SPS-1616:
   – Master device addresses SPS-1616 (slave)
   – Master device (master-transmitter), sends data to SPS-1616 (slave- receiver)
   – Master device terminates the transfer
2. If a master device wants to receive information from the SPS-1616:
   – Master device addresses SPS-1616 (slave)
   – Master device (master-receiver) receives data from SPS-1616 (slave- transmitter)
   – Master device terminates the transfer
3. If SPS-1616 polls configuration image from external memory
   – SPS-1616 addresses the memory
   – Memory transmits the data
   – SPS-1616 gets the data

All signaling is fully compliant with I²C (for signaling information, see the Philips *I²C Specification*) [1]. Standard signaling and timing waveforms are displayed below.

Connecting to Standard-, Fast-, and Hs-mode Devices

The SPS-1616 supports Fast/Standard (F/S) modes of operation. Per I²C specification, in mixed speed communication the SPS-1616 supports Hs- and Fast-mode devices at 400 Kbps, and Standard-mode devices at 100 Kbps. For information on speed negotiation on a mixed speed bus, see the I²C specification.

SPS-1616-Specific Memory Access (Slave Mode)

There is a SPS-1616-specific I²C memory access implementation. This implementation is fully I²C compliant. It requires the memory address to be specified during writes. This provides directed memory accesses through the I²C bus. Subsequent reads begin at the address specified during the last write.

The write procedure requires the 3 bytes (22 bits) of memory address to be provided following the device address. Thus, the following are required: device address – one or two bytes depending on 10-bit / 7-bit addressing, memory address – 3 bytes yielding 22 bits of memory address, and a 32-bit data payload – 4-byte words. To remain consistent with S-RIO standard maintenance packet memory address convention, the I²C memory address provided must be the 22 MSBs. Since I²C writes to memory apply to double-words (32 bits), the two LSBs are "don't care" as the LSBs correspond to word and byte pointers.

The read procedure has the memory address section of the transfer removed. Thus, to perform a read, the proper access would be to perform a write operation and issue a repeated start after the acknowledge bit following the third byte of memory address. Then, the master would issue a read command selecting the SPS-1616 through the standard device address procedure with the R/W bit high. Note that in 10-bit device address mode (ADS=1), only the two MSBs need be provided during this read. Data from the previously loaded address would immediately follow the device address protocol. A stop or repeated start can be issued anytime during the write data payload procedure, but must be before the final acknowledge; that is, canceling the write before the write operation is completed and performed. Also, the master would be allowed to access other devices attached to the I²C bus before returning to select the SPS-1616 for the subsequent read operation from the loaded address.

Read/Write Figures

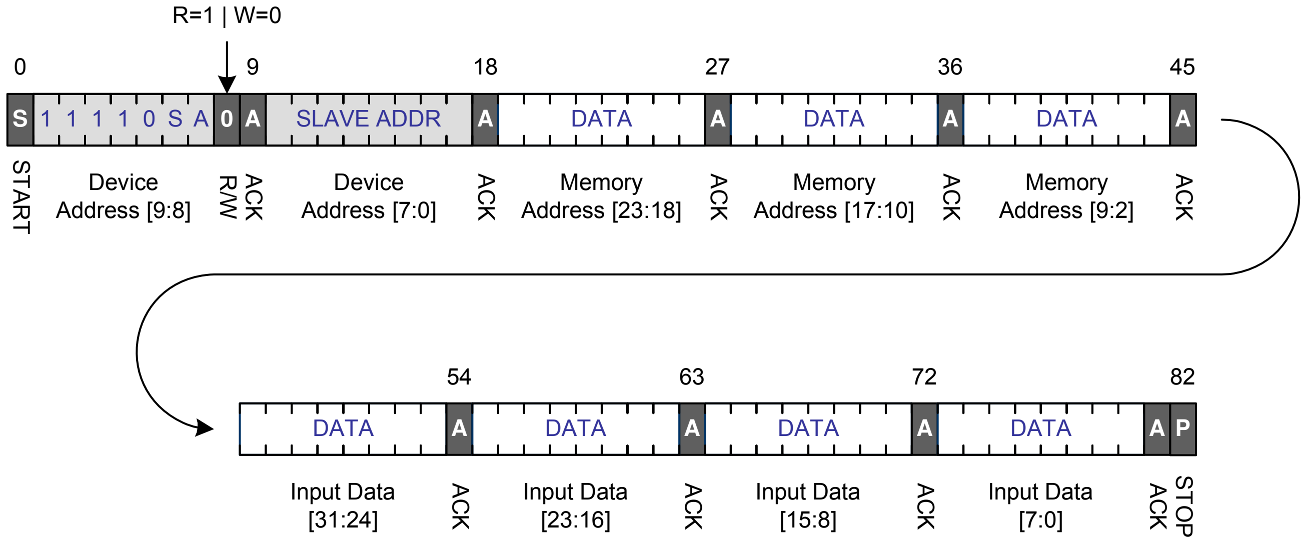

Figure 9: Write Protocol with 10-bit Slave Address (ADS is 1)

I²C writes to memory align on 32-bit word boundaries, thus the 24 address MSBs must be provided while the two LSBs associated with word and byte pointers are "don't care", and therefore are not transmitted.

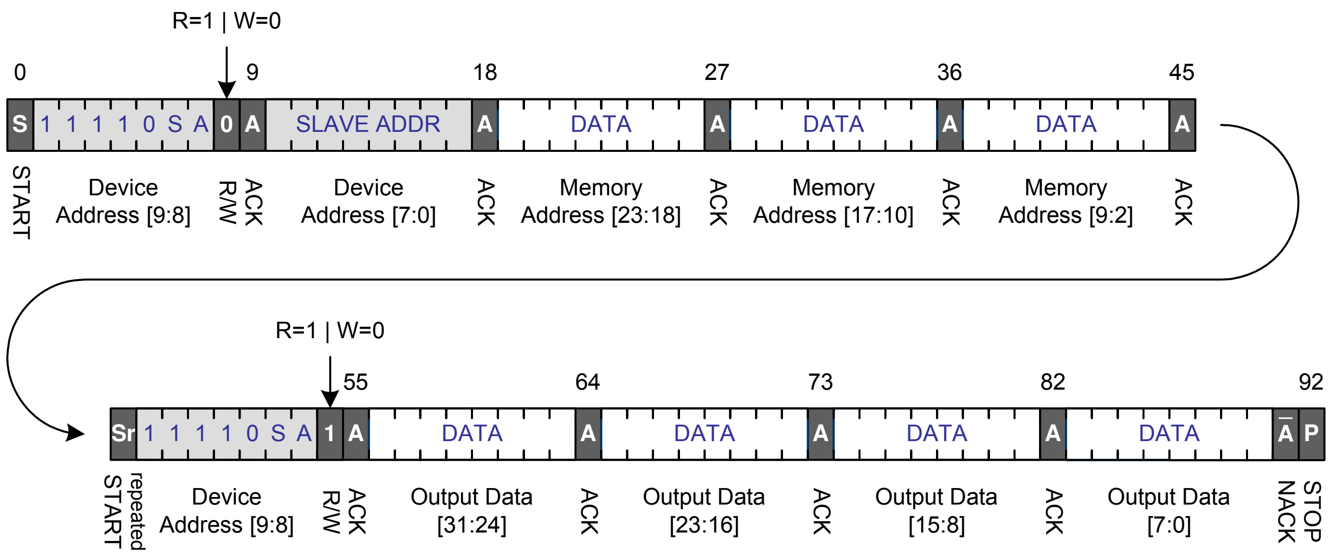

Figure 10: Read Protocol with 10-bit Slave Address (ADS is 1)

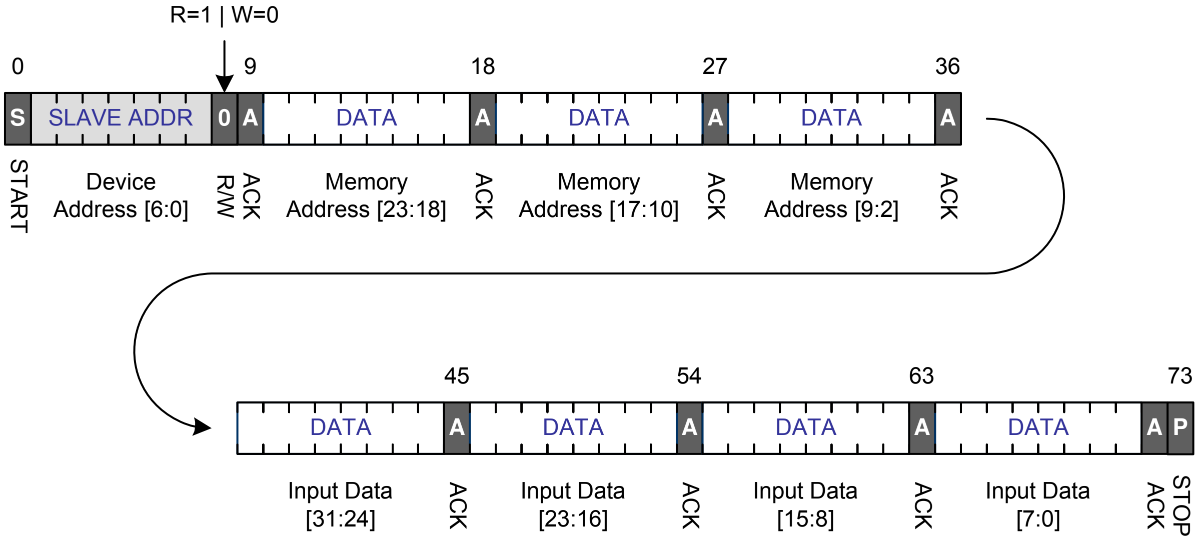

Figure 11: Write Protocol with 7-bit Slave Address (ADS is 0)

I^{2}C writes to memory align on 32-bit word boundaries, thus the 24 address MSBs must be provided while the two LSBs associated with word and byte pointers are "don't care", and therefore are not transmitted.

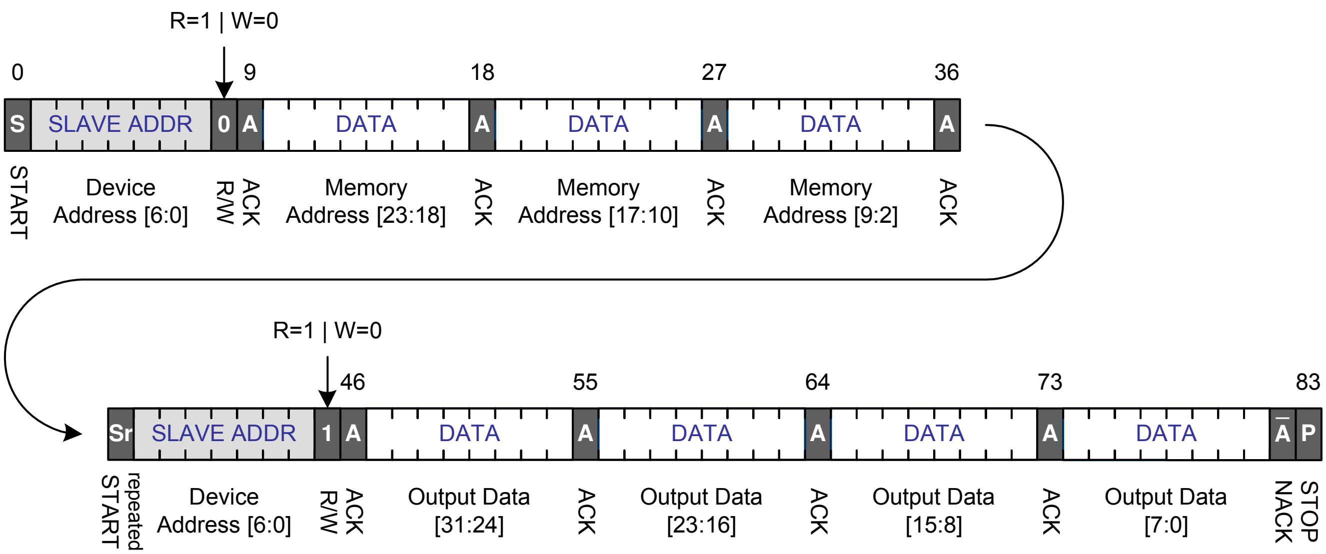

Figure 12: Read Protocol with 7-bit Slave Address (ADS is 0)

SPS-1616 Configuration and Image (Master mode)

There is both a power-up master and a command master mode. If powered up in master mode, the SPS-1616 polls configuration image from external memory after the device reset sequence has completed. Once the device has completed its configuration sequence, it will revert to slave mode. Through a configuration register write, the device can be commanded to enter master mode, which provides more configuration sequence flexibility. For more information, see the "I^{2}C Interface" chapter in the *SPS-1616 User Manual*.

I^2C DC Electrical Specifications

Note that the ADS and ID pins will all run off the V_{DD3} (3.3V/2.5V) power supply, and these pins are required to be fixed during operation. Thus, these pins must be statically tied to the 3.3V/2.5V supply or GND.

Table 8 to Table 10 list the SDA and SCL electrical specifications for F/S-mode I^2C devices.

At recommended operating conditions with V_{DD3} = 3.3V ± 5%.

Table 8 I^2C DC Electrical Specifications (3.3V)

Parameter	Symbol	Min	Max	Unit
Input high voltage level	V_{IH}	0.7 x V_{DD3}	$V_{DD3(max)}$ + 0.5	V
Input low voltage level	V_{IL}	-0.5	0.3 x V_{DD3}	V
Hysteresis of Schmitt trigger inputs	V_{HYS}	0.05 x V_{DD3}	-	V
Output low voltage	V_{OL}	0	0.4	ns
Output fall time from $V_{IH(min)}$ to $V_{IL(max)}$ with a bus capacitance from 10pF to 400pF	t_{OF}	20 + 0.1 x C_b	250	ns
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0	50	ns
Input current each I/O pin (input voltage is between 0.1 x V_{DD3} and 0.9 x V_{DD3} (max))	I_I	-10	10	uA
Capacitance for each I/O pin	C_I	-	10	pF

At recommended operating conditions with V_{DD3} = 2.5V ± 100mV.

Table 9 I^2C DC Electrical Specifications (2.5V)

Parameter	Symbol	Min	Max	Unit
Input high voltage level	V_{IH}	0.7 x V_{DD3}	$V_{DD3(max)}$ + 0.1	V
Input low voltage level	V_{IL}	-0.5	0.3 x V_{DD3}	V
Hysteresis of Schmitt trigger inputs	V_{HYS}	0.05 x V_{DD3}	-	V
Output low voltage	V_{OL}	0	0.4	ns
Output fall time from $V_{IH(min)}$ to $V_{IL(max)}$ with a bus capacitance from 10pF to 400pF	t_{OF}	20 + 0.1 x C_b	250	ns
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0	50	ns
Input current each I/O pin (input voltage is between 0.1 x V_{DD3} and 0.9 x V_{DD3} (max))	I_I	-10	10	uA
Capacitance for each I/O pin	C_I	-	10	pF