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12-Port Serial RapidIO® Switch

Datasheet 80KSW0004

1 Device Overview

The CPS-12, device number IDT80KSW0004, is a serial RapidIO (sRIO) switch whose functionality is central to routing packets for distribution among DSPs, processors, FPGAs, other switches, or any other sRIO-based devices. It may also be used in serial RapidIO backplane switching. The CPS-12 supports serial RapidIO packet switching (unicast, multicast, and an optional broadcast) from any of its 12 input ports to any of its 12 output ports.

2 Features

- **Interfaces - sRIO**
  - *12 bidirectional serial RapidIO (sRIO) lanes v 1.3*
  - *Port Speeds selectable: 3.125Gbps, 2.5Gbps, or 1.25Gbps*
  - *All lanes support short haul or long haul reach for each PHY speed*
  - *Configurable port count to up to twelve 1x ports, three 4x ports, or combinations of 1x and 4x ports (ex. eight 1x ports and one 4x port)*
  - *Lanes can be configured as individual non-redundant 1x ports, as part of a redundant 1x port, or as part of a 4x port*
  - *Support for two separate port rates for each quad*
  - *Supports standard 4 levels of priority*
  - *Error management support*
- **Interfaces - I^2C**
  - *Provides I^2C port for maintenance and error reporting*
  - *Master or Slave Operation*
  - *Master allows power-on configuration from external ROM*
  - *Master mode configuration with external image compressing and checksum*
- **Performance**
  - *30 Gbps of peak switching bandwidth*
  - *Non-blocking data flow architecture within each sRIO priority*
  - *Very low latency for all packet length and load condition*
  - *Internal queuing buffer and retransmit buffer*
  - *Standard receiver based physical layer flow control*
- **Features**
  - *Configurable for Cut Through or Store And Forward data flow*
  - *Device configurable through any of sRIO ports, I^2C, or JTAG*
  - *Packet Trace. Each port provides the ability to match the first 160 bits of any packet against up to 4 programmable comparison values to copy the packet to a programmable output trace port*
  - *Packet Filter. Each port also provides the ability to filter the packet based on comparisons against these same 4 programmable values mentioned above.*
  - *Supports up to 10 simultaneous multicast masks*
  - *Broadcast support*
  - *Port Loopback Debug Feature*
  - *Software assisted error recovery, supporting hot swap*
  - *Ports may be individually turned off to reduce power*
  - *PMON counters for monitor and diagnostics. Per input port and output port counters.*
  - *SerDes physical diagnostic registers*
  - *Embedded PRBS generation and detection with programmable polynomials support Bit Error Rate (BER) testing*
  - *0.13um technology*
  - *Low power dissipation*
  - *Full JTAG Boundary Scan Support (IEEE1149.1 & 1149.6)*
  - *Package: 324-ball grid array, 19mm x 19mm, 1.0mm ball pitch*

3 Block Diagram

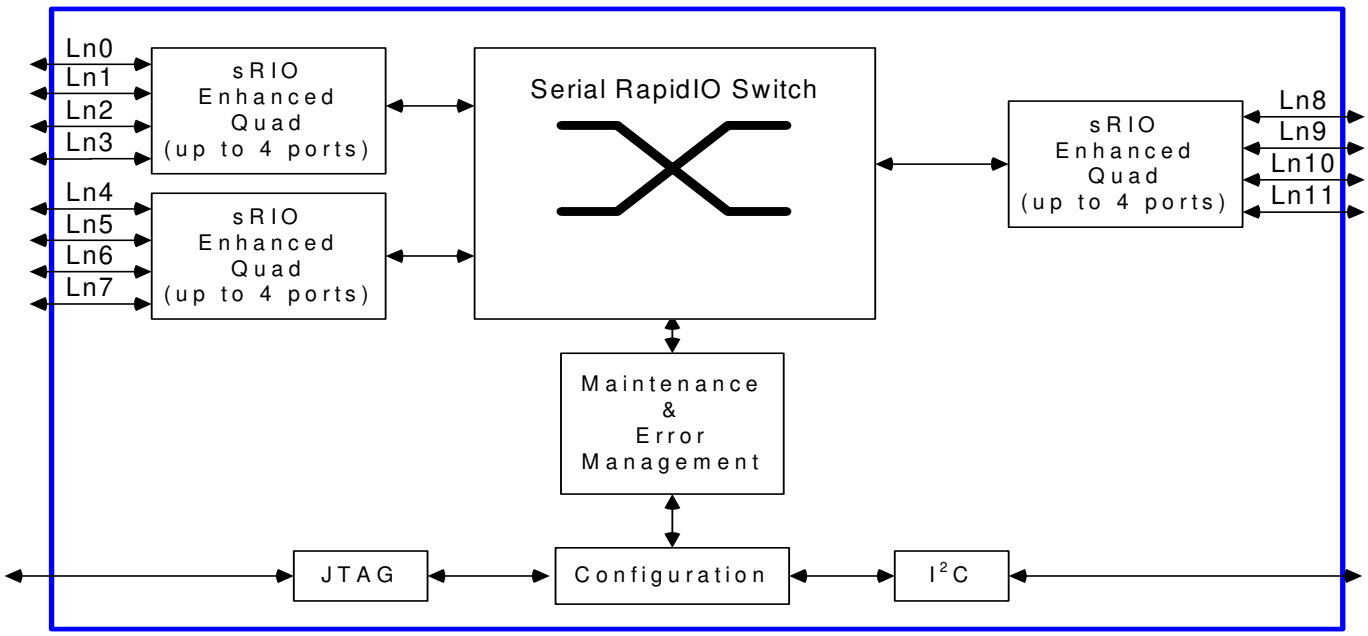

Figure 1 Block diagram

DSC 5697

4 Device Description

The CPS-12 is optimized for DSP cluster applications at board level. Its main function is to have a backplane interface which can connect to a backplane switch or directly to multiple RF cards. On the line card side it can also connect to multiple ports. It supports up to 12 ports which are configurable as line card, or backplane ports. It is an end-point free (switch) device in an sRIO network.

The CPS-12 receives packets from up to 12 ports. The CPS offers full support for normal switching as well as enhanced functions:

1) Normal Switching: All packets are switched in accordance with standard serial RapidIO specifications, with packet destination IDs determining how the packet is routed.

Three major options exist within this category:

a. Multicast: If a Multicast ID is received, the CPS-12 performs a multicast as defined in the sRIO multicast registers.
b. Unicast: All other operations are performed as specified in sRIO.
c. Maintenance packets: As specified by sRIO.

The sRIO Switch supports a peak throughput of 30 Gbps which is the line rate for 12 ports in 1x configuration, each at 2.5 Gbps (3.125 Gbps minus the sRIO-defined 8b10b encoding), and switches dynamically in accordance with the packet headers and priorities.

2) Enhanced functions

Enhanced features are provided for support of system debug. These features which are optional for the user consist of two major functions:

a. Packet Trace: The Packet Trace feature provides at-speed checking of the first 160 bits (header plus a portion of any payload) of every incoming packet against user-defined comparison register values. The trace feature is available on all serial RapidIO ports, each acting independently from one another. If the trace feature is enabled for a given port, every incoming packet is checked for a match against up to 4 comparison registers. In the event of a match, either of two possible user defined actions may take place:
   i) not only does the packet route normally through the switch to its appropriate destination port, but this same packet is replicated and sent to a “trace port.” The trace port itself may be any of the standard serial RapidIO ports. The port used for the trace port is defined by the user through simple register configuration.
   ii) the packet is dropped.

   If there is no match, the packets route normally through the switch with no action taken.

   The Packet Trace feature can be used during system bring-up and prototyping to identify particular packet types of interest to the user. It might be used in security applications, where packets must be checked for either correct or incorrect tags in either of the header or payload. Identified (match) packets are then routed to the trace port for receipt by a host processor, which can perform an intervention at the software level.
b. Port Loopback: The CPS-12 offers internal loopback for each port that may be used for system debug of the high speed sRIO ports. By enabling loopback on a given port, packets sent to the port’s receiver are immediately looped back at the physical layer to the transmitter - bypassing the higher logical or transport layers.
c. Broadcast: Each multicast mask can be configured so that the source port is included among the destination ports fo that multicast operation.

The CPS-12 can be programmed through any one or combination of sRIO, I^2C, or JTAG. Note that any sRIO port may be used for programming. The CPS-12 can also configure itself on power-up by reading directly from ROM over I^2C in master mode.

5 Applications

Central switch based wireless processing

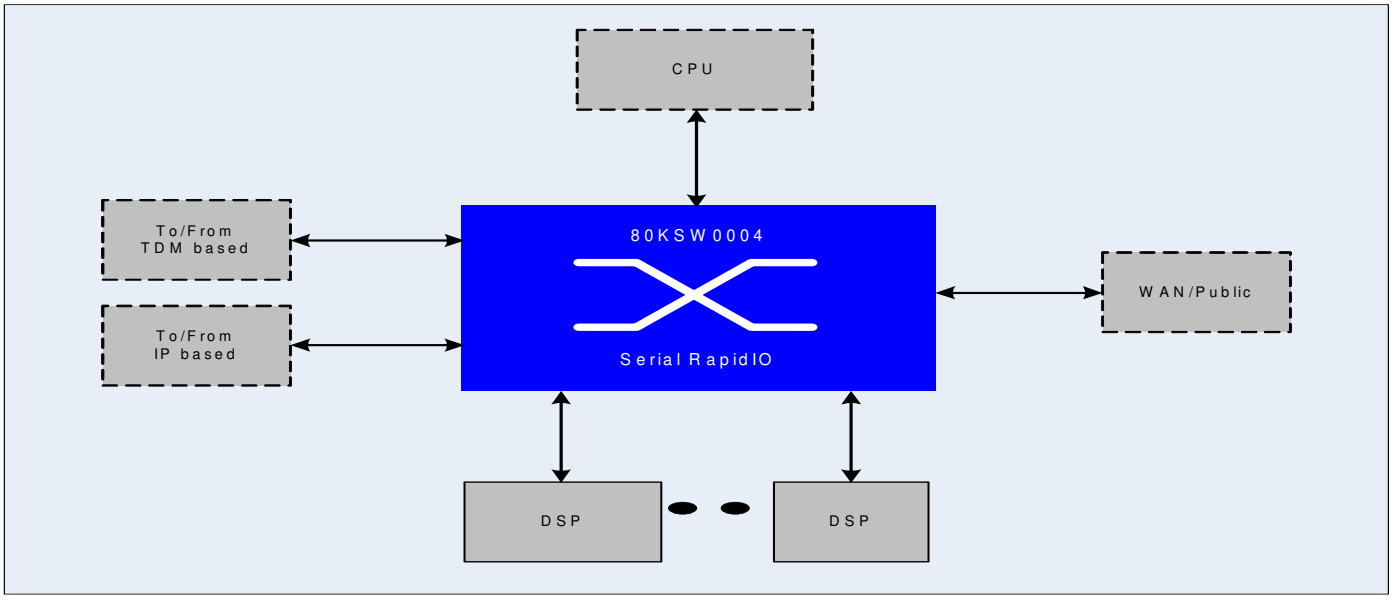

Figure 2 Application Overview

Note: The CPS-12 provides direct support for backplane connections using the serial RapidIO standard. The addition of an appropriate bridge (e.g., CPRI ↔ sRIO) allows for further backplane flexibility, accommodating designs based on a wide range of standards such as CPRI, OBSAI, GbE or PCIe.

In a macro wireless station, a switch-based raw data combination and distribution architecture is widely adoped. Switch based architecture provides high flexibility and high resource efficiency. The raw data from the Radio Unit is distributed to one or more processing cards by unicast or multicast. Aggregating raw data from processing cards to a buffer-less chain can be done by a fast non-blocking swich.

Media Gateway and general processing

Note: The CPS-12 provides direct support for backplane connections using the serial RapidIO standard.

Though SAR and RTP is usually processed by NP/Processor, DSP is more efficient for TDM conversion and compression. A low jitter switch enables the full utilization of DSP processing power. Priority support, fast switching, and multicasting will differentiate class of traffic to provide QoS.

6 Functional Overview

IDT's CPS-12 is optimized for either board-level DSP/ASIC cluster applications or module-level distributed processing application. Up to 12 serial RapidIO ports fully meet the standard V1.3 specification. The physical lanes may be configured to work at 3.125Gbps, 2.5Gbps or 1.25Gbps and in short haul or long haul.

The CPS-12 switch has a sustained 30Gbps bandwidth. Also three major options exist within this category:

a. Multicast: If a Multicast ID is received, the CPS-12 performs a multicast as defined by the device's configurable sRIO multicast mask registers. Also optional for broadcast.
b. Unicast: All other operations are performed as specified in sRIO.
c. Maintenance packets: As specified in sRIO.

The CPS-12 supports a "Store and Forward" and an optional "Cut Through" packet forward methodology. Refer to "CPS-12 User Manual" for details.

The CPS-12 can be programmed through a CPU or a DSP connected to one of the sRIO ports of the device or with a CPU connected to an I^2C or JTAG bus. It can also work along with a I^2C configuration memory. This option is added to allow the CPS-12 to work in "remote stand alone" mode.

Each sRIO port provides a packet trace capability. For any packet received by a port, a comparison between the first 160 bits and up to four configurable values can be performed. A match against any of these parameters will result in a copy of the packet and a route of the packet to a configurable ouput port. This feature can be used as a tactical function to track user data or in a debug environment to test how specific packets are moving through the platform.

Each sRIO port also provides a packet filter capability. For any packet received by a port, a comparison between the first 160 bits and up to the same four configurable values mentioned above can be performed. A match against any of these parameters will result in the packet being filtered.

7 Interface Overview

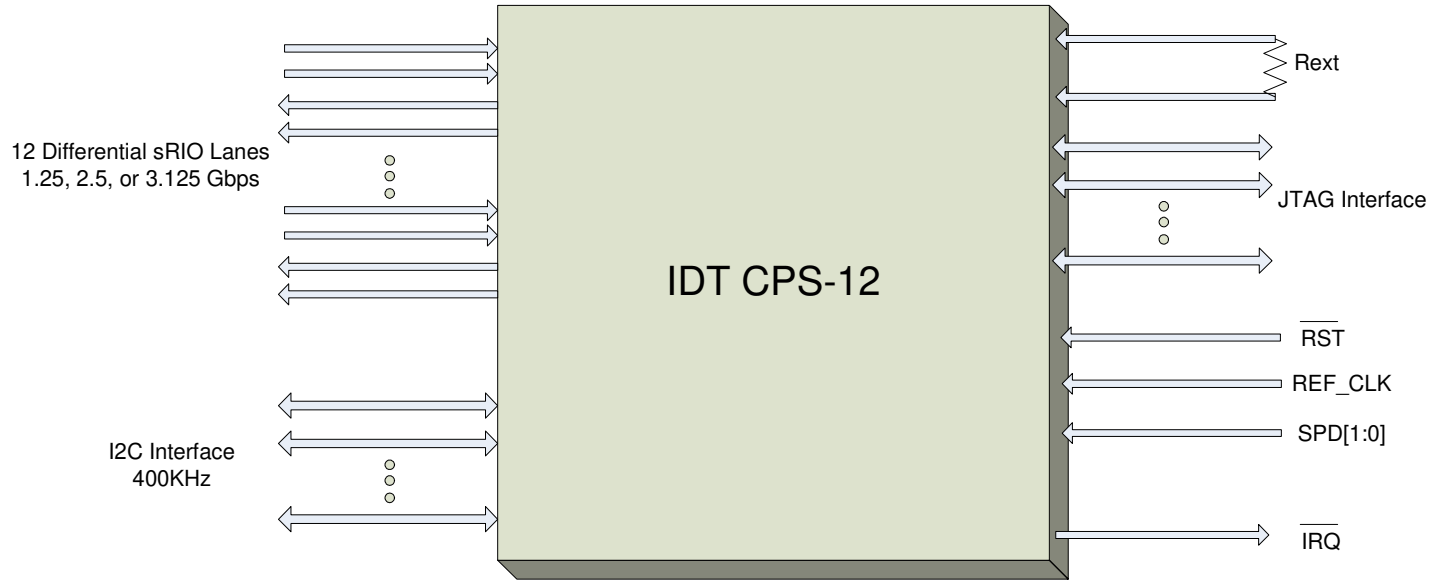

Figure 3 Diagram of the CPS-12 Interfaces

sRIO Ports

The sRIO interfaces are the main communication ports on the chip. These ports are compliant with the serial RapidIO v. 1.3 specifications. Please refer to the serial RapidIO specifications for full detail [2-10].

The device provides 12 differential dual simplex transceivers dedicated to sRIO I/O. These can be independently configured to run in various configurations as 1x- or 4x-ports. The CPS-12 supports a maximum of 3 times 4x-ports, or 12 times 1x-ports, as well as combinations of both 1x- and 4x-ports.

The device has a proprietary implementation which we refer to as an “Enhanced Quad.” An Enhanced Quad can be operated in standard sRIO mode like the standard quads. Additionally the Enhanced Quad can be register-configured to run as 4 independent 1x-ports - any of which can be enabled at a given time. In this manner, the user has the flexibility to use one, multiple, or all four lanes in 1x-mode. For example, lanes 0 - 3 are programmable into one 4x- or four 1x-ports. This is unlike the standard sRIO port implementation that, when configured as a 1x-port, renders the remaining 3 possible connections unused.

The device control of each of lane parameters (data rate, transmitter pre-emphasis, drive strength) can be separately configured, such that the characteristics for lanes 0 and 1 can be different from those for lanes 2 and 3 in one quad. The ability to control reset and init of lanes 0 and 1 versus lanes 2 and 3 separately is also provided. So each 2 lanes (lanes 0, 1 and lanes 3,4) at the granularity of the half quad can be programmed to run independently at 1.25, 2.5, or 3.125Gbps and handle long or short haul serial transmission per RIO serial specification.

I²C Bus

This interface may be used as an alternative to the standard sRIO or JTAG ports to program the chip and to check the status of registers - including the error reporting registers. It is fully compliant with the I²C specification, it supports master mode and slave mode, also supports both Fast-mode and Standard-mode buses [1]. Refer to the "I²C" section for full detail.

JTAG TAP Port

This TAP interface is IEEE1149.1 (JTAG) and 1149.6 (AC Extest) compliant [10, 11]. It may also be used as an alternative to the standard sRIO or I²C ports to program the chip and to check the status of registers - including the error reporting registers. It has 5 pins. Refer to the JTAG chapter for full detail.

Interrupt ($\overline{\text{IRQ}}$)

An interrupt output is provided in support of Error Management functionality. This output may be used to flag a host processor in the event of error conditions within the device. Refer to the Error Handling chapter for full detail.

Reset

A single Reset pin is used for full reset of the CPS-12, including setting all registers to power-up defaults. Refer to the Reset & Intialization chapter for full detail.

Clock

The single system clock (REF_CLK+ / -) is a 156.25MHz differential clock.

Rext (Rextn & Rextp)

These pins are used to establish the drive bias on the SerDes output. An external bias resistor is required. The two pins must be connected to one another with a 12k Ohm resistor. This provides CML driver stability across process and temperature.

SPD[1:0]

Speed Select Pins. These pins define the sRIO port speed at RESET for all ports. The RESET setting may be overridden by subsequent programming of the QUAD_CTRL register. SPD[1:0] = {00 = 1.25G, 01 = 2.5G, 10 = 3.125G, 11 = RESERVED}. These pins must remain STATICALLY BIASED before power-up.

8 Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM} (V_{DD3})	V_{DD3} Terminal Voltage with Respect to GND	-0.5 to 3.6	V
V_{TERM}(2) (V_{DD3}-supplied interfaces)	Input or I/O Terminal Voltage with Respect to GND	-0.3 to V_{DD3}+0.3	V
V_{TERM} (V_{DD})	V_{DD} Terminal Voltage with Respect to GND	-0.5 to 1.5	V
V_{TERM}(2) (V_{DD}-supplied interfaces)	Input or I/O Terminal Voltage with Respect to GND	-0.3 to V_{DD}+0.3	V
V_{TERM} (V_{DDS})	V_{DDS} Terminal Voltage with Respect to GNDS	-0.5 to 1.5	V
V_{TERM}(2) (V_{DDS}-supplied interfaces)	Input or I/O Terminal Voltage with Respect to GNDS	-0.3 to V_{DDS}+0.3	V
V_{TERM} (V_{DDA})	V_{DDA} Terminal Voltage with Respect to GNDS	-0.5 to 1.5	V
V_{TERM}(2) (V_{DDA}-supplied interfaces)	Input or I/O Terminal Voltage with Respect to GNDS	-0.3 to V_{DDA}+0.3	V
T_{BIAS}(3)	Temperature Under Bias	-55 to +125	C
T_{STG}	Storage Temperature	-65 to +150	C
T_{JN}	Junction Temperature	+125	C
I_{OUT} (For V_{DD3} = 3.3V)	DC Output Current	30	mA
I_{OUT} (For V_{DD3} = 2.5V)	DC Output Current	30	mA

Table 1 Absolute Maximum Rating

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. Power sequencing is not necessary; however, the voltage on any Input or I/O pin cannot exceed its corresponding supply voltage during power supply ramp up.
3. Ambient Temperature under DC Bias. No AC Conditions.

9 Recommended Temperature and Operating Voltage[1]

Grade	Ambient Temperature	Ground[2]	Supply Voltage[4]
Commercial	0°C to 70°C	GND = 0V GNDS = 0V	V_{DD} = 1.2 +/- 5% V_{DDS} = 1.2 +/- 5% V_{DD3}[3] = 3.3 +/- 5% or 2.5V +/- 100mV V_{DDA} = 1.2 +/- 5%
Industrial	-40°C to 85°C	GND = 0V GNDS = 0V	V_{DD} = 1.2 +/- 5% V_{DDS} = 1.2 +/- 5% V_{DD3}[3] = 3.3 +/- 5% or 2.5V +/- 100mV V_{DDA} = 1.2 +/- 5%

Table 2 Recommended Temperature and Operating Voltage

NOTES:

1. Power sequencing is not necessary; however, the voltage on any Input or I/O pin cannot exceed its corresponding supply voltage during power supply ramp up. The device is not sensitive to supply rise and fall times, and thus these are not specified.

2. V_{DD3}, V_{DDA}, and V_{DDS} share a common ground (GNDS). Core supply and ground are V_{DD} and GND respectively.

3. V_{DD3} may be operated at either 3.3V or 2.5V simply by providing that supply voltage. For those interfaces operating on this supply, this datasheet provides input and output specifications at each of these voltages.

4. V_{DDS} & V_{DDA} may be tied to a common power plane. V_{DD} (core, digital supply) should have its own supply and plane.

10 AC Test Conditions

Input Pulse Levels	GND to 3.0V / GND to 2.4V
Input Rise / Fall Times	2ns
Input Timing Reference Levels	1.5V / 1.25V
Output Reference Levels	1.5V / 1.25V
Output Load	Figures 4

Table 3 AC Test Conditions (V_{DD3}=3.3V / 2.5V): JTAG, I^2C, RST

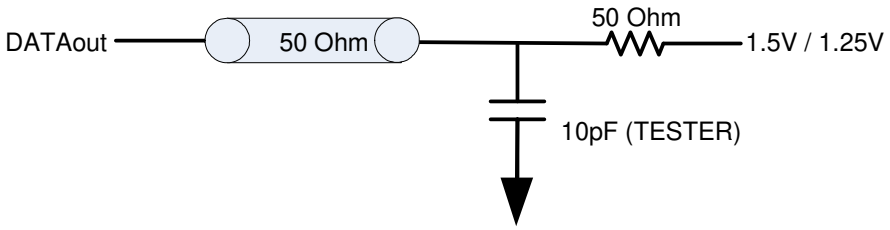

Figure 4 AC Output Test Load (JTAG)

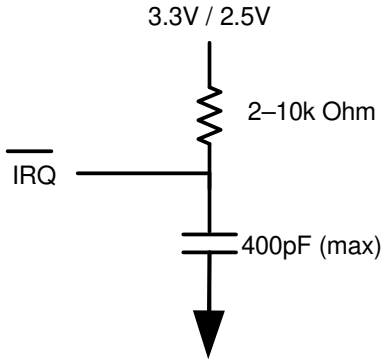

Figure 5 AC Output Test Load (IRQ)

NOTE: The $\overline{IRQ}$ pin is an open-driver. IDT recommends a weak pull-up resistor (2-10k Ohm) be placed on this pin to $V_{DD}3$.

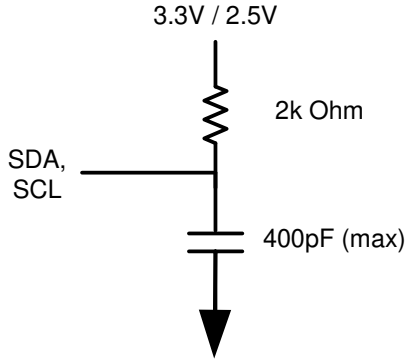

Figure 6 AC Output Test Load (I^2C)

NOTE: The SDA and SCL pins are open-drain drivers. Refer to the Philips I^2C specification [1] for appropriate selection of pull-up resistors for each.

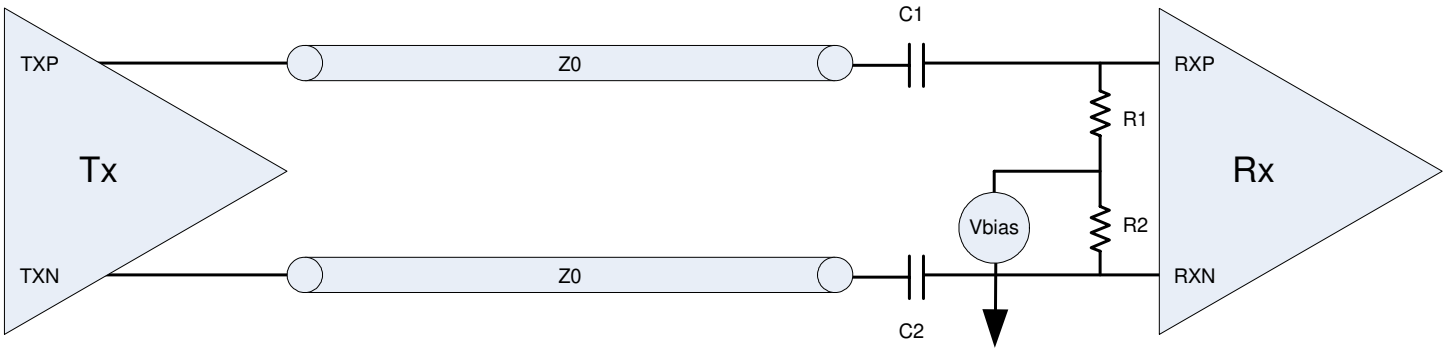

Figure 7 sRIO Lanes Test Load

The characteristic impedance Z0 should be designed for 100 Ohms. An inline capacitor C1 and C2 at each input of the receiver provides AC-coupling and a DC-block. The IDT recommended and test value is 100nF for each. Thus, any DC bias differential between the two devices on the link is negated. The differential input resistance at the receiver is designed to be 100 Ohms (per sRIO specification). Thus, R1 and R2 are 50 Ohms each. Note that V_{BIAS} is the internal bias voltage of the device's receiver.

11 Device Performance Figures

Performance Figures

The following table lists the CPS-12's performance figure. Figures provided here are guaranteed by design and characterization, but are not production tested.

Description	Min	Typ	Max	Units	Comments
Switch Throughput (Peak)	-	-	30	Gbps	
Switch Throughput (Sustained)	-	28	-	Gbps	Value shown is for device configured for 3 4X ports, each running at 3.125Gbps, 276 byte packets at priority 0. Please contact IDT technical support for figures related to a specific usage case and traffic conditions.
Switch Latency Jitter (70% switch load)[2]	-	60	-	ns	Latency Jitter for the switch lock is the sum of the Physical layer jitter plus one maintenance packet of contention delay for a given output port. Worst case for the physical layer is the jitter caused by the port sync process. This requires 6 32-bite control symbols plus 2 cycles times the port rate. The figures shown here are for priority 2 packets under 70% switch loading with an even mix of packets of each priority. It assumes that no maintenance packets contend on the output port.
Soft Reset to Receipt of Valid Packets	-	-	26	us	This includes reset time as well as link establishment.
Hard Reset to Receipt of Valid Packets	-	-	26	us	This includes reset time as well as link establishment.
Multicast Map Update Delay	25	-	2000	cycles[3]	

Table 4 80KSW0004 Performance Figures

NOTES:

1. Values are guaranteed by characterization, but are not production tested.

2. For those specifications associated with an sRIO transaction, it should be noted that the upper limit to a specification may be dictated by sRIO priority handling. For example, a maintenance read packet having lower priority may be held off until higher priority packets in queue are serviced. The user should take into consideration this additional priority-induced delay when examining these specifications. I^2C and JTAG configuration register access transactions are always deterministic and follow these specifications identically.

3. "Cycles" refer to internal core clock cycles which are two times the external reference clock (REF_CLK) frequency = 312.5 MHz.

Switch Latency in "Store-and-Forward" mode

Pay Load Size	1.25GHz		2.5GHz		3.125GHz	
	1X	4X	1X	4X	1X	4X
8 Byte	456 ns	343 ns	277 ns	225 ns	246 ns	209 ns
16 Byte	517 ns	360 ns	311 ns	231 ns	267 ns	213 ns
32 Byte	652 ns	435 ns	375 ns	272 ns	320 ns	239 ns
64 Byte	902 ns	500 ns	501 ns	305 ns	422 ns	263 ns
128 Byte	1425 ns	722 ns	757 ns	417 ns	630 ns	352 ns
256 Byte	2451 ns	1071 ns	1273 ns	590 ns	1035 ns	492 ns
Multicast Event Control Symbol	115 ns	105 ns	60 ns	55 ns	50 ns	45 ns

Table 5 Switch Latency Table (Store-and-Forward mode)

1) Values are guaranteed by characterization, but are not production tested.

2) For those specifications associated with an sRIO transaction, it should be noted that the upper limit to a specification may be dictated by sRIO priority handling. For example, a maintenance read packet having lower priority may be held off until higher priority packets in queue are serviced. The user should take into consideration this additional priority-induced delay when examining these specifications. I^2C and JTAG transactions are always deterministic and follow these specifications identically.

3) Switch latency is a statistical function, which typically increases with increased traffic loading on the switch. Values shown in Table 5 are for single input port to single output port with matching input and output port rates in "Store-and-Forward" mode, no other switch loading. The switch latency in "Store-and-Forward" packet forward methodology is also a strong function of port rate. For specific values under other specific application usage scenarios and traffic conditions, please contact IDT technical support.

Switch Latency in "Cut-Through" mode

Pay Load Size	1.25GHz		2.5GHz		3.125GHz	
	1X	4X	1X	4X	1X	4X
8 Byte	366 ns	322 ns	244 ns	216 ns	208 ns	199 ns
16 Byte	363 ns	324 ns	234 ns	215 ns	206 ns	197 ns
32 Byte	365 ns	316 ns	232 ns	215 ns	205 ns	198 ns
64 Byte	365 ns	318 ns	234 ns	219 ns	204 ns	198 ns
128 Byte	372 ns	314 ns	233 ns	217 ns	210 ns	196 ns
256 Byte	371 ns	312 ns	238 ns	216 ns	205 ns	195 ns

Table 6 Switch Latency Table (Cut-Through mode)

1) Values shown in Table 6 are typical for single input port to single output port with matching input and output port rates in "Cut-Through" mode, no other switch loading. For specific values under other specific application usage scenarios and traffic conditions, please contact IDT technical support.

Note:

In "Store-and-Forward" mode and "Cut-Through" mode when trace and filter are enabled at the same time, the latency for packets sent to the trace port will increase by the time taken to send 20 bytes into the port ([20 bytes * 8] * 1/[port_speed * 0.8]). The latency for other traffic flow will be unaffected.

12 Typical Power Figures

Typical power draw for the 80KSW0004 is approximately 2.7W total for all ports enabled as 3 4x @ 3.125G under 50% switch load. The following table provides power figures on a per-block basis. An estimate of the device power figure for a given application usage can be determined by using the "CPS Power Calculator" modeling tool available on www.IDT.com

Description	Type	Units	Supply	Comments
SerDes 1x @ 1.25G	45	mW	V_{DDS}, V_{DDA}	Analog SerDes power consumption (V_{DDS} and V_{DDA}). This does not include the sRIO quad power consumption.
SerDes 1x @ 2.5G	60	mW	V_{DDS}, V_{DDA}	Analog SerDes power consumption (V_{DDS} and V_{DDA}). This does not include the sRIO quad power consumption.
SerDes 1x @ 3.125G	75	mW	V_{DDS}, V_{DDA}	Analog SerDes power consumption (V_{DDS} and V_{DDA}). This does not include the sRIO quad power consumption.
SerDes 4x @ 1.25G	200	mW	V_{DDS}, V_{DDA}	Analog SerDes power consumption (V_{DDS} and V_{DDA}). This does not include the sRIO quad power consumption.
SerDes 4x @ 2.5G	220	mW	V_{DDS}, V_{DDA}	Analog SerDes power consumption (V_{DDS} and V_{DDA}). This does not include the sRIO quad power consumption.
SerDes 4x @ 3.125G	245	mW	V_{DDS}, V_{DDA}	Analog SerDes power consumption (V_{DDS} and V_{DDA}). This does not include the sRIO quad power consumption.
JTAG Block Enable	100	mW	V_{DD}, V_{DD3}	Configuration Register Access only. Max interface speed(10MHz).
I2C Block Enable	20	mW	V_{DD}, V_{DD3}	Configuration Register Access only. Max interface speed (400KHz).
Switch Block (max traffic)	312	mW	V_{DD}	Switch block only. All ports enabled and sending traffic at max aggregate throughput for the switch block.
Standy Power @1.25G	1286	mW	V_{DD}	Part powered up, reset, all links up (reset configuration), no traffic
Standy Power @1.25G	214	mW	V_{DD3}	Part powered up, reset, all links up (reset configuration), no traffic
Standy Power @1.25G	383, 270	mW	V_{DDS}, V_{DDA}	Part powered up, reset, all links up (reset configuration), no traffic
Quiescent Power	1200	mW	V_{DD}	Minimum possible operational power draw. All ports disable, I2C and JTAG signals static.
Quiescent Power	214	mW	V_{DD3}	Minimum possible operational power draw. All ports disable, I2C and JTAG signals static.
Quiescent Power	37, 32	mW	V_{DDS}, V_{DDA}	Minimum possible operational power draw. All ports disable, I2C and JTAG signals static.
Reset Power	324	mW	V_{DD}	Peak power during RESET of the device.
Reset Power	210	mW	V_{DD3}	Peak power during RESET of the device.
Reset Power	35, 27	mW	V_{DDS}, V_{DDA}	Peak power during RESET of the device.
Peak sustained Power	1858	mW	V_{DD}	All sRIO ports enabled at maximum speed, maximum traffic to the switch.
Peak sustained Power	214	mW	V_{DD3}	All sRIO ports enabled at maximum speed, maximum traffic to the switch.
Peak sustained Power	512, 349	mW	V_{DDS}, V_{DDA}	All sRIO ports enabled at maximum speed, maximum traffic to the switch

Table 7 Typical Power Figures

Condition: Vdd = 1.2V, Vdds = 1.2V, Vdda = 1.2V, Vdd3 = 3.3V @ Room temperature 25°C

Maximum peak sustained power draw for the 80KSW0004 is 3.5W total (2.23W for V_{DD}, 0.61W for V_{DDS}, 0.42W for V_{DDA} and 0.26W for V_{DD3}) for all ports enabled as 12 1x @ 3.125G under 100% switch load at the max operational voltage specification(1.2V+5%=1.26V, 3.3V+5%=3.45V) across full temperature and process range.

13 I²C-Bus

The CPS-12 is compliant with the I²C specification [1]. This specification provides all functional detail and electrical specifications associated with the I²C bus. This includes signaling, addressing, arbitration, AC timing, DC specifications, and other details.

The I²C bus is comprised of Serial Data (SDA) and Serial Clock (SCL) pins. It can be used to attach a CPU or a configuration memory. The I²C interface supports Fast/Standard (F/S) mode (400/ 100 kHz).

I²C master mode and slave mode

The CPS-12 device supports both master mode and slave mode. It's selected by MM static configuration pin. Refer to following for signaling and operation.

I²C Device Address

The device address for the CPS-12 is fully pin-defined by 10 external pins while in slave mode. This provides full flexibility in defining the slave address to avoid conflicting with other I²C devices on a given bus. The CPS-12 may be operated as either a 10-bit addressable device or a 7-bit addressable device based on another external pin, address select (ADS). If the ADS pin is tied to Vdd, then the CPS-12 operates as a 10-bit addressable device and the device address will be defined as ID[9:0]. If the ADS pin is tied to GND, then the CPS-12 operates as a 7-bit addressable device with the device address defined by ID[6:0]. The addressing mode must be established at power-up and remain static throughout operation. Dynamic changes will result in undetermined behavior.

Pin	I²C Address Bit (pin_addr)
ID0	0
ID1	1
ID2	2
ID3	3
ID4	4
ID5	5
ID6	6
ID7	7 (don't care in 7-bit mode)
ID8	8 (don't care in 7-bit mode)
ID9	9 (don't care in 7-bit mode)

Table 8 I²C static address selection pin configuration

All of the CPS-12's registers are addressable through I²C. These registers are accessed via 22-bit addresses and 32-bit word boundaries though standard reads and writes. These registers may also be accessed through the sRIO and JTAG interfaces.

Signaling

Communication with the CPS-12 on the I²C bus follows these three cases:

1) Suppose a master device wants to send information to the CPS-12:
- Master device addresses CPS-12 (slave)
- Master device (master-transmitter), sends data to CPS-12 (slave- receiver)
- Master device terminates the transfer

2) If a master device wants to receive information from the CPS-12:
- Master device addresses CPS-12 (slave)
- Master device (master-receiver) receives data from CPS-12 (slave- transmitter)
- Master device terminates the transfer.

3) If CPS-12 polls configuration image from external memory
   - CPS-12 addresses the memory.
   - Memory transmits the data.
   - CPS-12 gets the data.

All signaling is fully compliant with I^2C. Full detail of signaling can be found in the Philips I^2C specification [1]. Standard signalling and timing waveforms are shown below.

Interfacing to Standard-, Fast-, and Hs-mode Devices

The CPS-12 supports Fast / Standard (F/S) modes of operation. Per I^2C specification, in mixed speed communication the CPS-12 supports Hs- and Fast-mode devices at 400 kbit/s, and Standard-mode devices at 100 kbit/s. Please refer to the I^2C specification for detail on speed negotiation on a mixed speed bus.

CPS-12 Specific Memory Access (Slave mode)

There is a CPS-12 specific I^2C memory access implementation. This implementation is fully I^2C compliant. It requires the memory address to be explicitly specified during writes. This provides directed memory accesses through the I^2C bus. Subsequent reads always begin at the address specified during the last write.

The write procedure requires the 3-Bytes (22-bits) of memory address to be provided following the device address. Thus, the following are required: device address – one or two bytes depending on 10-bit / 7-bit addressing, memory address – 3 bytes yielding 22-bits of memory address, and a 32-bit data payload – 4 byte words. To remain consistent with sRIO standard maintenance packet memory address convention, the I^2C memory address provided must be the 22MSBs. Since I^2C writes to memory apply to double words (32-bits), the 2 LSBs are DON'T CARE as the LSBs correspond to word and byte pointers.

The read procedure has the memory address section of the transfer removed. Thus, to perform a read, the proper access would be to perform a write operation and issue a repeated start after the acknowledge bit following the third byte of memory address. Then, the master would issue a read command selecting the CPS-12 through the standard device address procedure with the R/W bit high. Note that in 10-bit device address mode (ADS=1), only the two MSBs need be provided during this read. Data from the previously loaded address would immediately follow the device address protocol. It is possible to issue a stop or repeated start anytime during the write data payload procedure, but must be before the final acknowledge (i.e. canceling the write before the actual write operation is completed and performed). Also, the master would be allowed to access other devices attached to the I^2C bus before returning to select the CPS-12 for the subsequent read operation from the loaded address.

Figures

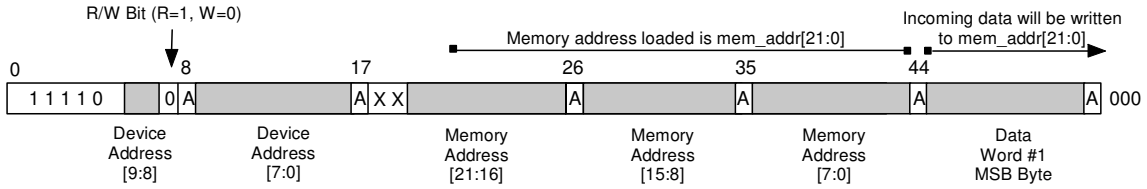

Figure 8 Write protocol with 10-bit Slave Address (ADS =1). I^2C writes to memory align on 32-bit word boundaries, thus the 22 address MSBs must be provided while the 2 LSB's associated with word and byte pointers are DON'T CARE and are therefore not transmitted.

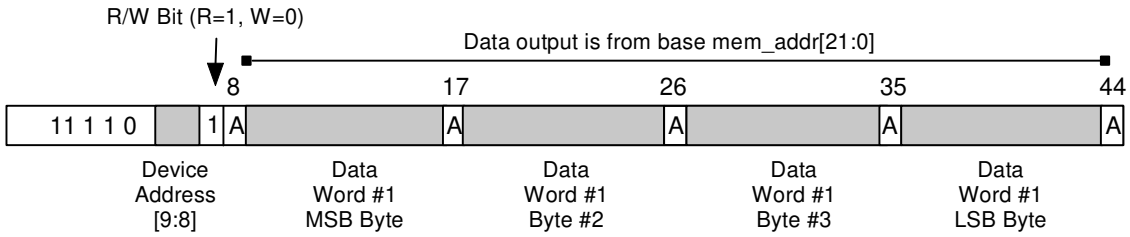

Figure 9 Read Protocol with 10-bit Slave Address (ADS=1)

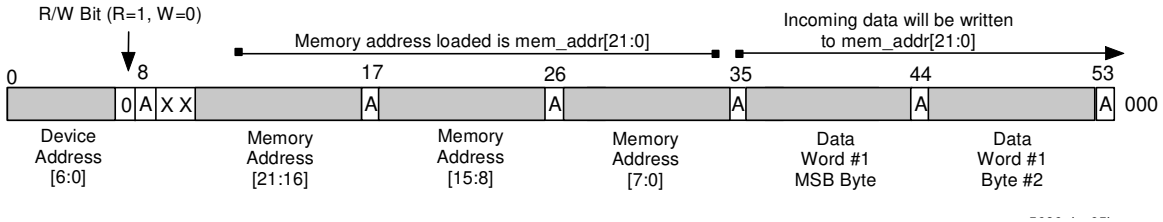

Figure 10 Write protocol with 7-bit Slave Address (ADS=0). I²C writes to memory align on 32-bit word boundaries, thus the 22 address MSBs must be provided while the 2 LSB's associated with word and byte pointers are DON'T CARE and are therefore not transmitted.

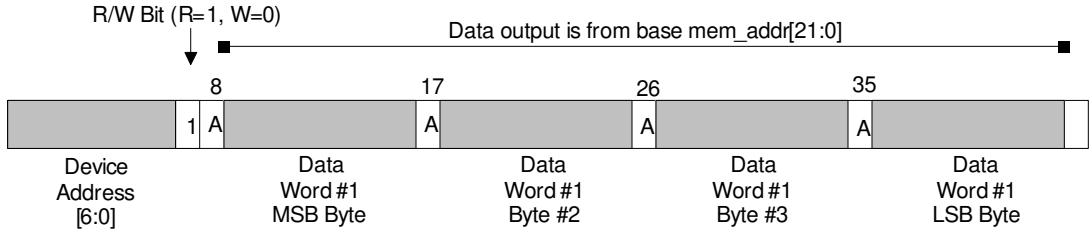

Figure 11 Read protocol with 7-bit Slave Address (ADS=0)

CPS-12 configuration and image (Master mode)

There is both a power up master and a command master mode. If powered up in master mode, the CPS-12 polls configuration image from external memory after the device reset sequence has completed. Once the device has completed its configuration sequence, it will revert to slave mode. Through a config register write, the device can be commanded to enter master mode, which provides more configuration sequence flexibility. Refer to "CPS-12 User Manual" for details.

I²C DC Electrical Specifications

Note that the ADS and ID pins will all run off the core (1.2V) power supply, and these pins are required to be fixed during operation. Thus, these pins must be statically tied to the 1.2V supply or GND.

Tables 9 through 11 below list the SDA and SCL electrical specifications for F/S-mode I²C devices:

At recommended operating conditions with V_{DD3} = 3.3V ± 5%

Parameter	Symbol	Min	Max	Unit
Input high voltage level	V_{IH}	0.7 x V_{DD3}	$V_{DD3\,(MAX)}$+ 0.5	V
Input low voltage level	V_{IL}	-0.5	0.3 x V_{DD3}	V
Hysteresis of Schmitt trigger inputs:	Vhys	0.05 x V_{DD3}	-	
Low level output voltage	V_{OL}	0	0.2 x V_{DD3}	V
Output fall time from $V_{IH(MIN)}$ to $V_{IL(MAX)}$ with a bus capacitance from 10pF to 400pF	t_{OF}	20 + 0.1 x C_b	250	ns
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0	50	ns
Input current each I/O pin (input voltage is between 0.1 x V_{DD3} and 0.9 x $V_{DD3\,(MAX)}$)	I_I	-10	10	uA
Capacitance for each I/O pin	C_I	-	10	pF

Table 9 I^2C SDA & SCL DC Electrical Specifications

At recommended operating conditions with V_{DD3} = 2.5V ± 100mV

Parameter	Symbol	Min	Max	Unit
Input high voltage level	V_{IH}	0.7 x V_{DD3}	$V_{DD3(MAX)}$ + 0.1	V
Input low voltage level	V_{IL}	-0.5	0.3 x V_{DD3}	V
Hysteresis of Schmitt trigger inputs:	Vhys	0.05 x V_{DD3}	-	
Low level output voltage	V_{OL}	0	0.2 x V_{DD3}	V
Output fall time from $V_{IH(MIN)}$ to $V_{IL(MAX)}$ with a bus capacitance from 10pF to 400pF	t_{OF}	20 + 0.1 x C_b	250	ns
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0	50	ns
Input current each I/O pin (input voltage is between 0.1 x V_{DD3} and 0.9 x $V_{DD3\,(MAX)}$)	I_I	-10	10	uA
Capacitance for each I/O pin	C_I	-	10	pF

Table 10 I^2C SDA & SCL DC Electrical Specifications

I²C AC Electrical Specifications

Signal	Symbol	Reference Edge	Standard Mode		Fast Mode		Unit
			Min	Max	Min	Max	
I²C(1,4)							
SCL	f_{SCL}	none	0	100	0	400	kHz
	$t_{HD;STA}$		4.0	—	0.6	—	µs
	t_R		—	1000	—	300	µs
	t_F		—	300	—	300	µs
SDA(2,3)	$t_{SU;DAT}$	SCL rising	250	—	100	—	µs
	$t_{HD;DAT}$		0	3.45	0	0.9	µs
	t_R		—	1000	10	300	µs
	t_F		—	300	10	300	µs
Start or repeated start condition	$t_{SU;STA}$	SDA falling	4.7	—	0.6	—	µs
	$t_{SU;STO}$		4.0	—	0.6	—	µs
Stop condition	$t_{SU;STO}$	SDA rising	4.0	—	0.6	—	µs
Bus free time between a stop and start condition	t_{BUF}		4.7	—	1.3	—	µs
Capacitive load for each bus line	C_b		—	400	—	400	pF

Table 11 Specifications of the SDA and SCL bus lines for F/S-mode I²C -bus devices

NOTES:

1. For more information, see the I²C-Bus specification by Philips Semiconductor [1].
2. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{RMAX} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-mode I²C-bus specification) before the SCL line is released.

I²C Timing Waveforms

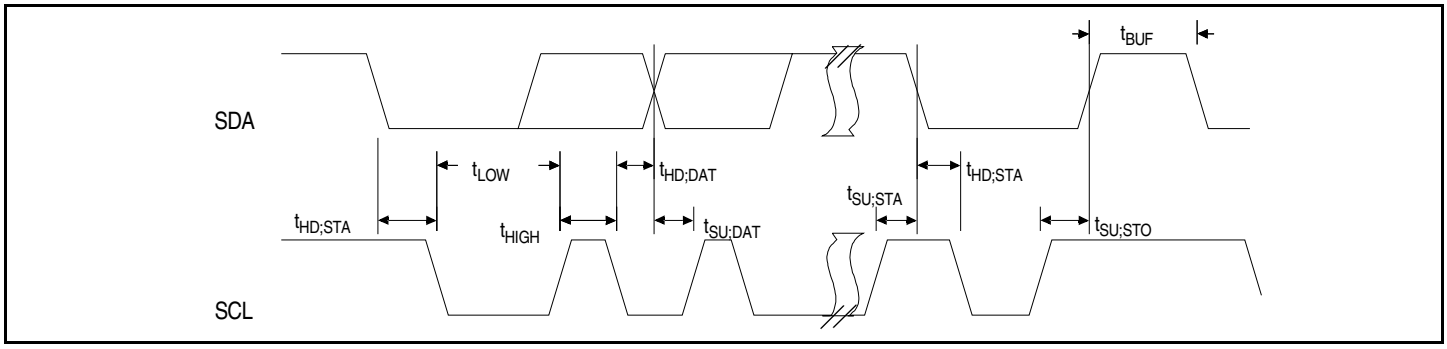

Figure 12 I²C Timing Waveforms

14 Interrupt ($\overline{IRQ}$) Electrical Specifications

At recommended operating conditions with V_{DD3} = 3.3V ± 5%

Parameter	Symbol	Min	Max	Unit
Low level output voltage (I_{OL} = 4mA, V_{DD3} = Min.)	V_{OL}	0	0.4	V
Output fall time from $V_{IH(min)}$ to $V_{IL(max)}$ with a bus capacitance from 10pF to 400pF	t_{OF}	-	25	ns
Input current each I/O pin (input voltage is between 0.1 x V_{DD3} and 0.9 x V_{DD3} (max))	I_I	-10	10	uA
Capacitance for $\overline{IRQ}$	C_I	-	10	pF

Table 12 $\overline{IRQ}$ Electrical Specifications (V_{DD3} = 3.3V ± 5%)

At recommended operating conditions with V_{DD3} = 2.5V ± 100mV

Parameter	Symbol	Min	Max	Unit
Low level output voltage (I_{OL} = 2mA, V_{DD3} = Min.)	V_{OL}	0	0.4	V
Output fall time from $V_{IH(min)}$ to $V_{IL(max)}$ with a bus capacitance from 10pF to 400pF	t_{OF}	-	25	ns
Input current each I/O pin (input voltage is between 0.1 x V_{DD3} and 0.9 x V_{DD3} (max))	I_I	-10	10	uA
Capacitance for $\overline{IRQ}$	C_I	-	10	pF

Table 13 $\overline{IRQ}$ Electrical Specifications (V_{DD3} = 2.5V ± 100mV)

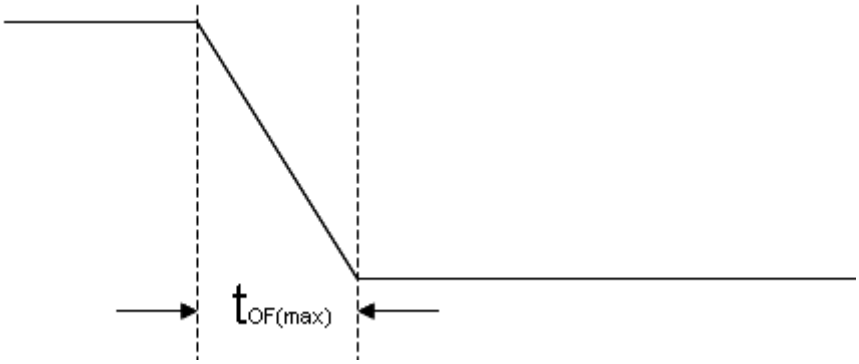

Figure 13 $\overline{IRQ}$ Timing Diagram

The $\overline{IRQ}$ pin is an open-drain driver. IDT recommends a weak pull-up resistor (2-10k Ohm) be placed on this pin to V_{DD3}. The $\overline{IRQ}$ pin goes active low when any special error filter error flag is set, and is cleared when all error flags are reset. Please refer to the device user's manual for full detail.

15 Serial RapidIO Ports

Overview

The CPS-12's SERDES are in full compliance to the RapidIO AC specifications for the LP-Serial physical layer [5]. This section provides those specifications for reference. The electrical specifications cover both single and multiple-lane links. Two transmitters (short run and long run) and a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple chip-to-chip interconnect to driving two connectors across a backplane. A single receiver specification is given that will accept signals from both the short run and long run transmitter specifications.

The short run transmitter setting should be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The CPS-12 can drive beyond the specification distance of at least 50 cm at all baud rates. Please use IDT's Simulation Kit IO models to determine reach and signal quality for a given PCB design.

Signal Definitions

LP-Serial links uses differential signaling. This section defines terms used in the description and specification of differential signals. Differential Peak-Peak Voltage of Transmitter or Receiver shows how the signals are defined. The figure shows waveforms for either a transmitter output (TD and $\overline{TD}$) or a receiver input (RD and $\overline{RD}$). Each signal swings between A Volts and B Volts where A > B. Using these waveforms, the definitions are as follows:

1. The transmitter output signals and the receiver input signals TD, $\overline{TD}$, RD and $\overline{RD}$ each have a peak-to-peak swing of A - B Volts
2. The differential output signal of the transmitter, V_{OD}, is defined as V_{TD}-$V_{\overline{TD}}$.
3. The differential input signal of the receiver, V_{ID}, is defined as V_{RD}-$V_{\overline{RD}}$.
4. The differential output signal of the transmitter and the differential input signal of the receiver each range from A - B to -(A - B) Volts.
5. The peak value of the differential transmitter output signal and the differential receiver input signal is A - B Volts
6. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is 2 * (A - B) Volts

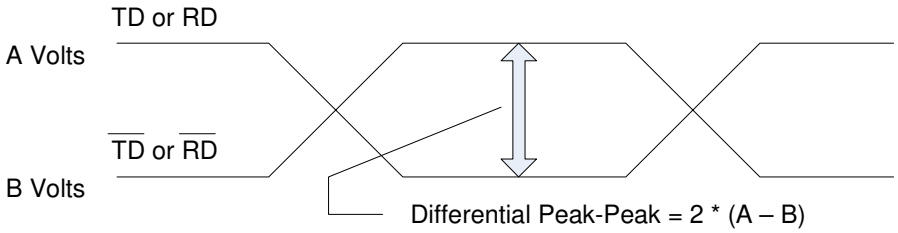

Figure 14 Differential Peak-Peak Voltage of Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5V and 2.0V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{TD}$ is 500 mV p-p. The differential output signal ranges between 500 mV and -500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

Equalization

With the use of high speed serial links, the interconnect media will cause degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The equalization technique implemented in the CPS-12 is Pre-emphasis on the transmitter (under register control).

Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to serial RapidIO. The goal of this standard is that electrical designs for serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case shall be better than

-10 dB for (Baud Frequency)/10 < Freq(f) < 625 MHz, and

-10 dB + 10log(f/625 MHz) dB for 625 MHz <= Freq(f) <= Baud Frequency

The reference impedance for the differential return loss measurements is 100 Ohm resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

The CPS-12 satisfies the specification requirement that the 20%-80% rise/fall time of the transmitter, as measured at the transmitter output, in each case has a minimum value 60 ps.

Similarly the timing skew at the output of an LP-Serial transmitter between the two signals that comprise a differential pair does not exceed 25 ps at 1.25 GB, 20 ps at 2.50GB and 15 ps at 3.125 GB.

Symbol	Parameter	Range		Unit	Notes
		Min	Max		
V_O	Output Voltage	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair.
$V_{DIFF\ PP}$	Differential Output Voltage	500	1000	mV p-p	
J_D	Deterministic Jitter	-	0.17	UI p-p	
J_T	Total Jitter	-	0.35	UI p-p	
S_{MO}	Multiple Output Skew	-	1000	ps	Skew at the transmitter output between lanes of a multilane link
UI	Unit Interval	800	800	ps	+/- 100 ppm

Table 14 Short Run Transmitter AC Timing Specifications - 1.25 GBaud

Symbol	Parameter	Range		Unit	Notes
		Min	Max		
V_O	Output Voltage	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair.
$V_{DIFF\ PP}$	Differential Output Voltage	500	1000	mV p-p	
J_D	Deterministic Jitter	-	0.17	UI p-p	
J_T	Total Jitter	-	0.35	UI p-p	
S_{MO}	Multiple Output Skew	-	1000	ps	Skew at the transmitter output between lanes of a multilane link
UI	Unit Interval	400	400	ps	+/- 100 ppm

Table 15 Short Run Transmitter AC Timing Specifications - 2.5 GBaud

Symbol	Parameter	Range		Unit	Notes
		Min	Max		
V_O	Output Voltage	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair.
$V_{DIFF\ PP}$	Differential Output Voltage	500	1000	mV p-p	
J_D	Deterministic Jitter	-	0.17	UI p-p	
J_T	Total Jitter	-	0.35	UI p-p	
S_{MO}	Multiple Output Skew	-	1000	ps	Skew at the transmitter output between lanes of a multilane link
UI	Unit Interval	320	320	ps	+/- 100 ppm

Table 16 Short Run Transmitter AC Timing Specifications - 3.125 GBaud

Symbol	Parameter	Range		Unit	Notes
		Min	Max		
V_O	Output Voltage	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair.
$V_{DIFF\ PP}$	Differential Output Voltage	800	1600	mV p-p	
J_D	Deterministic Jitter	-	0.17	UI p-p	
J_T	Total Jitter	-	0.35	UI p-p	
S_{MO}	Multiple Output Skew	-	1000	ps	Skew at the transmitter output between lanes of a multilane link
UI	Unit Interval	800	800	ps	+/- 100 ppm

Table 17 Long Run Transmitter AC Timing Specifications - 1.25 GBaud

Symbol	Parameter	Range		Unit	Notes
		Min	Max		
V_O	Output Voltage	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair.
$V_{DIFF\ PP}$	Differential Output Voltage	800	1600	mV p-p	
J_D	Deterministic Jitter	-	0.17	UI p-p	
J_T	Total Jitter	-	0.35	UI p-p	
S_{MO}	Multiple Output Skew	-	1000	ps	Skew at the transmitter output between lanes of a multilane link
UI	Unit Interval	400	400	ps	+/- 100 ppm

Table 18 Long Run Transmitter AC Timing Specifications - 2.5 GBaud

Symbol	Parameter	Range		Unit	Notes
		Min	Max		
V_O	Output Voltage	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair.
$V_{DIFF\ PP}$	Differential Output Voltage	800	1600	mV p-p	
J_D	Deterministic Jitter	-	0.17	UI p-p	
J_T	Total Jitter	-	0.35	UI p-p	
S_{MO}	Multiple Output Skew	-	1000	ps	Skew at the transmitter output between lanes of a multilane link
UI	Unit Interval	320	320	ps	+/- 100 ppm

Table 19 Long Run Transmitter AC Timing Specifications - 3.125 GBaud

For each baud rate at which an LP-Serial transmitter is specified to operate, the output eye pattern of the transmitter falls entirely within the unshaded portion of the Transmitter Output Compliance Mask shown in Transmitter Output Compliance Mask (Figure 15) with the parameters specified in Transmitter Differential Output Eye Diagram Parameters (Table 17) when measured at the output pins of the device and the device is driving a 100 Ohm +/- 5% differential resistive load. The specification allows the output eye pattern of a LP-Serial transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) to only comply with the Transmitter Output Compliance Mask when pre-emphasis is disabled or minimized.

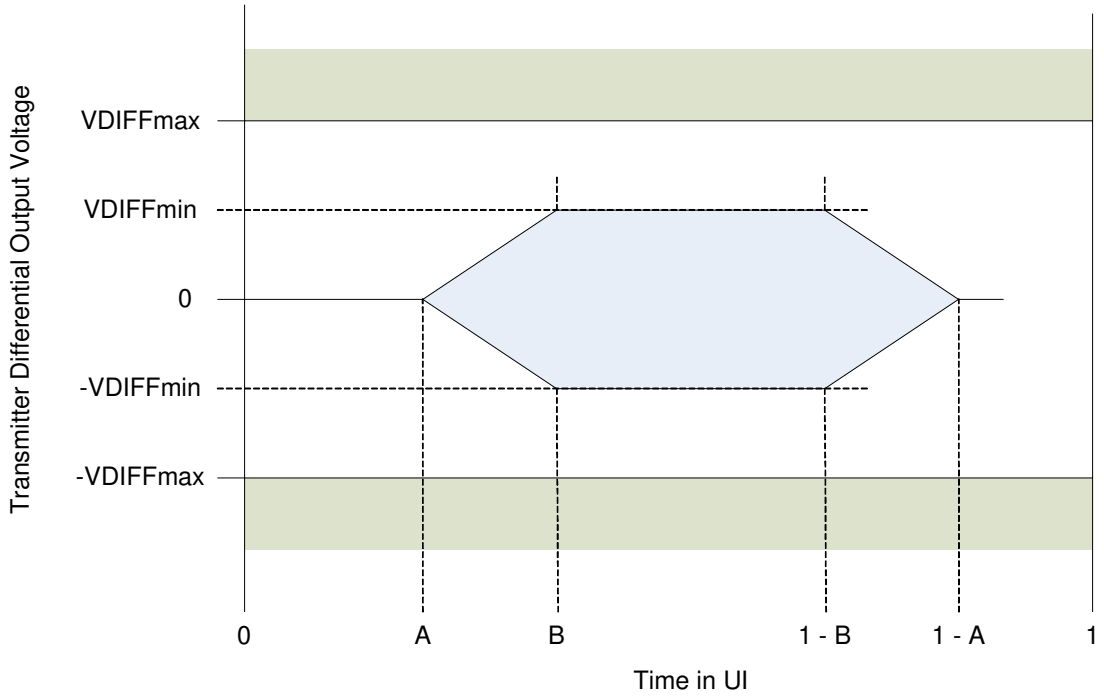

Figure 15 Transmitter Output Compliance Mask

Transmitter Setting	$V_{DIFFmin}$ (mV)	$V_{DIFFmax}$ (mV)	A (UI)	B (UI)
1.25 GBaud Short Range	250	500	0.175	0.39
1.25 GBaud Long Range	400	800	0.175	0.39
2.5 GBaud Short Range	250	500	0.175	0.39
2.5 GBaud Long Range	400	800	0.175	0.39
3.125 GBaud Short Range	250	500	0.175	0.39
3.125 Gbaud Long Range	400	800	0.175	0.39

Table 20 Transmitter Differential Output Eye Diagram Parameters

Receiver Specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section.

The receiver input impedance results in a differential return loss better than 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8)*(Baud Frequency). This includes contributions from on-chip circuitry, the chip package and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100 Ohm resistive for differential return loss and 25 Ohm resistive for common mode.

Symbol	Parameter	Range		Unit	Notes
		Min	Max		
V_{IN}	Differential Input Votlage	200	1600	mV p-p	Measured at receiver
J_D	Deterministic Jitter Tolerance	0.37	-	UI p-p	Measured at receiver
J_{DR}	Combined Deterministic and Random Jitter Tolerance	0.55	-	UI p-p	Measured at receiver
J_T	Total Jitter Tolerance(1)	0.65	-	UI p-p	Measured at receiver
S_{MI}	Multiple Input Skew	-	24	ns	Skew at the receiver input between lanes of a multi-lane link
BER	Bit Error Rate		10^{-12}		
UI	Unit Interval	800	800	ps	+/- 100 ppm

Table 21 Receiver AC Timing Specifications - 1.25 GBaud

NOTE:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 16. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Symbol	Parameter	Range		Unit	Notes
		Min	Max		
V_{IN}	Differential Input Votlage	200	1600	mV p-p	Measured at receiver
J_D	Deterministic Jitter Tolerance	0.37	-	UI p-p	Measured at receiver
J_{DR}	Combined Deterministic and Random Jitter Tolerance	0.55	-	UI p-p	Measured at receiver
J_T	Total Jitter Tolerance(1)	0.65	-	UI p-p	Measured at receiver
S_{MI}	Multiple Input Skew	-	24	ns	Skew at the receiver input between lanes of a multi-lane link
BER	Bit Error Rate		10^{-12}		
UI	Unit Interval	400	400	ps	+/- 100 ppm

Table 22 Receiver AC Timing Specifications - 2.5 GBaud

NOTE:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 16. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Symbol	Parameter	Range		Unit	Notes
		Min	Max		
V_{IN}	Differential Input Votlage	200	1600	mV p-p	Measured at receiver
J_D	Deterministic Jitter Tolerance	0.37	-	UI p-p	Measured at receiver
J_{DR}	Combined Deterministic and Random Jitter Tolerance	0.55	-	UI p-p	Measured at receiver
J_T	Total Jitter Tolerance(1)	0.65	-	UI p-p	Measured at receiver
S_{MI}	Multiple Input Skew	-	22	ns	Skew at the receiver input between lanes of a multi-lane link
BER	Bit Error Rate		10^{-12}		
UI	Unit Interval	320	320	ps	+/- 100 ppm

Table 23 Receiver AC Timing Specifications - 3.125 GBaud

NOTE:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 16. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

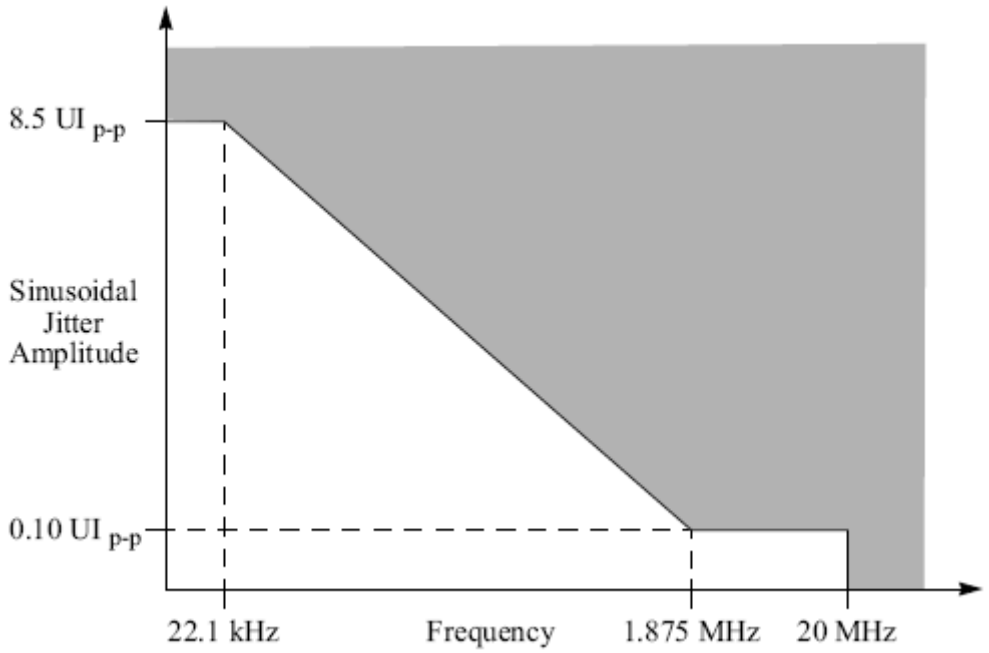

Figure 16 Single Frequency Sinusoidal Jitter Limits