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Contact us

16-Channel

Short Haul E1

Line Interface Unit

IDT82P20516

Version -
December 17, 2009

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FEATURES

◆ **Integrates 16 channels E1 short haul line interface units for 120 Ω E1 twisted pair cable and 75 Ω E1 coaxial cable applications**

◆ **Per-channel configurable Line Interface options**
- Fully integrated and software selectable receive and transmit termination
  - *Option 1: Fully Internal Impedance Matching with integrated receive termination resistor*
  - *Option 2: Partially Internal Impedance Matching with common external resistor for improved device power dissipation*
  - *Option 3: External impedance Matching termination*
- Supports global configuration and per-channel configuration to E1 mode

◆ **Per-channel programmable features**
- Provides E1 short haul waveform templates and user-programmable arbitrary waveform templates
- Provides two JAs (Jitter Attenuator) for each channel of receiver and transmitter
- Supports AMI/HDB3 (for E1) encoding and decoding

◆ **Per-channel System Interface options**
- Supports Single Rail, Dual Rail with clock or without clock and sliced system interface
- Integrated Clock Recovery for the transmit interface to recover transmit clock from system transmit data

◆ **Per-channel system and diagnostic functions**
- Provides transmit driver over-current detection and protection with optional automatic high impedance of transmit interface
- Detects and generates PRBS (Pseudo Random Bit Sequence), ARB (Arbitrary Pattern) and IB (Inband Loopback) in either receive or transmit direction
- Provides defect and alarm detection in both receive and transmit directions.
  - *Defects include BPV (Bipolar Violation) /CV (Code Violation) and EXZ (Excessive Zeroes)*
  - *Alarms include LLOS (Line LOS), SLOS (System LOS), TLOS (Transmit LOS) and AIS (Alarm Indication Signal)*
- Programmable LLOS detection /clear levels. Compliant with ITU and ANSI specifications

- Various pattern, defect and alarm reporting options
  - *Serial hardware LLOS reporting (LLOS, LLOS0) for all 16 channels*
  - *Register access to individual registers or 16-bit error counters*
- Supports Analog Loopback, Digital Loopback and Remote Loopback
- Supports line monitor

◆ **Hitless Protection Switching (HPS) without external Relays**
- Supports 1+1 and 1:1 hitless protection switching
- Asynchronous hardware control (OE, RIM) for fast global high impedance of receiver and transmitter (hot switching between working and backup board)
- High impedance transmitter and receiver while powered down
- Per-channel register control for high impedance, independent for receiver and transmitter

◆ **Clock Inputs and Outputs**
- Flexible master clock (N x 1.544 MHz or N x 2.048 MHz) ($1 \leq N \leq 8$, N is an integer number)
- Integrated clock synthesizer can multiply or divide the reference clock to a wide range of frequencies: 8 KHz, 64 KHz, 2.048 MHz, 4.096 MHz, 8.192 MHz, 19.44 MHz and 32.768 MHz

◆ **Microprocessor Interface**
- Supports Serial microprocessor interface

◆ **Other Key Features**
- IEEE1149.1 JTAG boundary scan
- Two general purpose I/O pins
- 3.3 V I/O with 5 V tolerant inputs
- 3.3 V and 1.8 V power supply
- Package: 484-pin Fine Pitch BGA (19 mm X 19 mm)

◆ **Applicable Standards**
- Bellcore TR-TSY-000009, GR-253-CORE and GR-499-CORE
- ETSI CTR12/13
- ETS 300166 and ETS 300 233
- G.703, G.735, G.736, G.742, G.772, G.775, G.783 and G.823
- O.161

APPLICATIONS

◆ **SDH/SONET multiplexers**

◆ **Central office or PBX (Private Branch Exchange)**

◆ **Digital access cross connects**

◆ **Remote wireless modules**

◆ **Microwave transmission systems**

DESCRIPTION

The IDT82P20516 is a 16-channel high-density E1 short haul Line Interface Unit. Each channel of the IDT82P20516 can be independently configured. The configuration is performed through a Serial microprocessor interface.

In the receive path, through a Single Ended or Differential line interface, the received signal is processed by an adaptive Equalizer and then sent to a Slicer. Clock and data are recovered from the digital pulses output from the Slicer. After passing through an enabled or disabled Receive Jitter Attenuator, the recovered data is decoded using B8ZS/ AMI/HDB3 line code rule in Single Rail NRZ Format mode and output to the system, or output to the system without decoding in Dual Rail NRZ Format mode and Dual Rail RZ Format mode.

In the transmit path, the data to be transmitted is input on TDn in Single Rail NRZ Format mode or TDPn/TDNn in Dual Rail NRZ Format mode and Dual Rail RZ Format mode, and is sampled by a transmit reference clock. The clock can be supplied externally from TCLKn or recovered from the input transmit data by an internal Clock Recovery. A selectable JA in Tx path is used to de-jitter gapped clocks. To meet E1 waveform standards, two E1 templates and one J1 template, as well as an arbitrary waveform generator are provided. The data through the Waveform Shaper, the Line Driver and the Tx Transmitter is output on TTIPn and TRINGn.

Alarms (including LOS, AIS) and defects (including BPV, EXZ) are detected in both receive line side and transmit system side. AIS alarm, PRBS, ARB and IB patterns can be generated /detected in receive / transmit direction for testing purpose. Analog Loopback, Digital Loopback and Remote Loopback are all integrated for diagnostics.

JTAG per IEEE 1149.1 is also supported by the IDT82P20516.
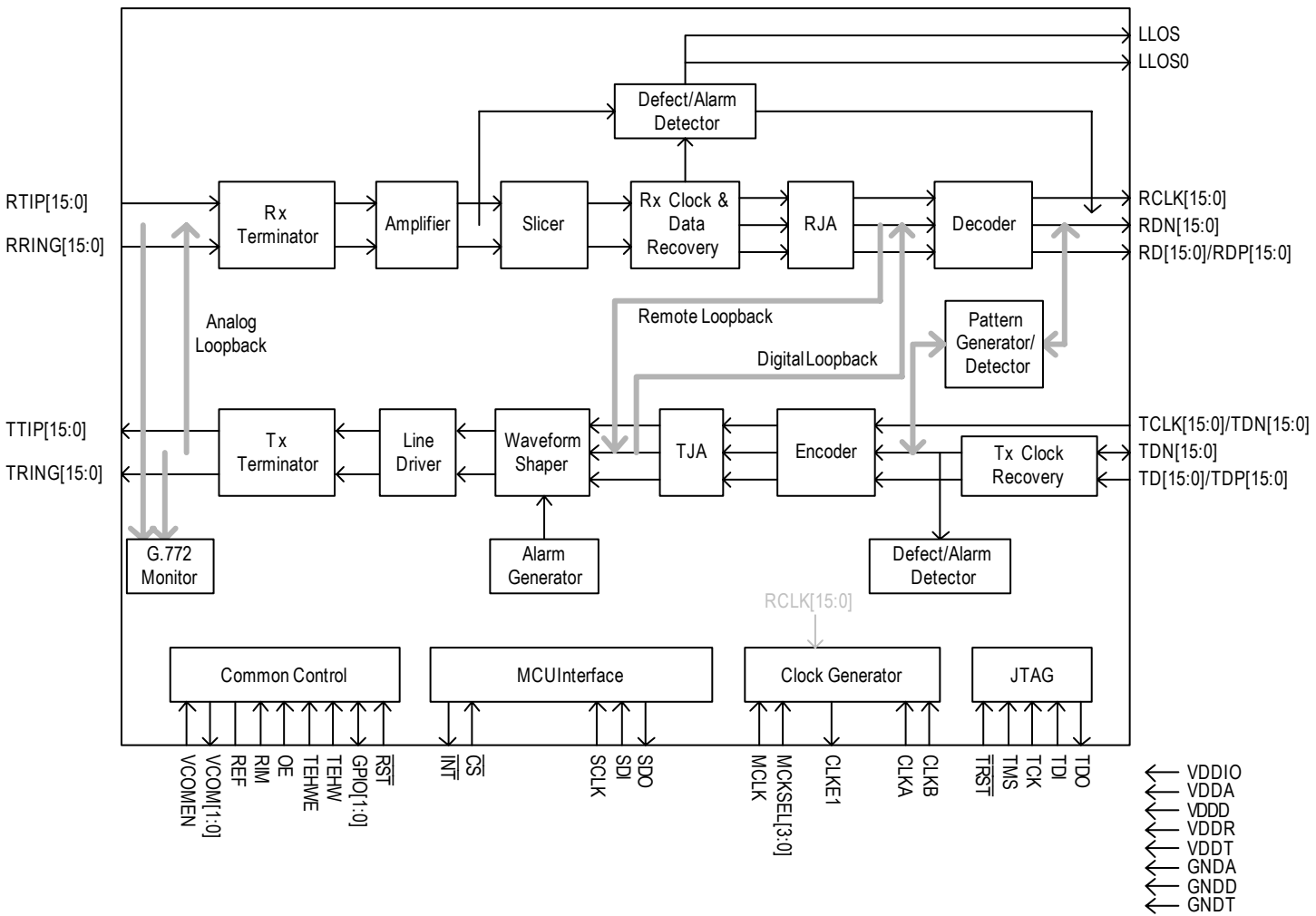
Figure-1   Functional Block Diagram

1   PIN ASSIGNMENT

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A	NC	NC	NC	NC	RD15/RDP15	TDN14	RCLK14	TDN13	RCLK13	TDN12	RCLK12	RCLK11	TDN11	RCLK10	TDN10	RCLK9	TDN9	RCLK8	NC	NC	NC	NC	**A**
B	NC	NC	NC	NC	TCLK15/TDN15	TD14/TDP14	RDN14	TD13/TDP13	RDN13	TD12/TDP12	RDN12	RDN11	TD11/TDP11	RDN10	TD10/TDP10	RDN9	TD9/TDP9	RD8/RDP8	NC	NC	NC	NC	**B**
C	TRING12	NC	NC	NC	TD15/TDP15	GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	TDN8	NC	NC	NC	NC	**C**
D	TTIP12	NC	NC	NC	TDN15	RDN15	TCLK14/TDN14	VDDIO	TCLK13/TDN13	GNDD	TCLK12/TDN12	TCLK11/TDN11	VDDIO	TCLK10/TDN10	VDDIO	TCLK9/TDN9	VDDIO	TD8/TDP8	NC	NC	NC	NC	**D**
E	TRING13	GNDA	GNDA	GNDA	NC	RCLK15	RD14/RDP14	GNDD	RD13/RDP13	VDDIO	RD12/RDP12	RD11/RDP11	GNDD	RD10/RDP10	GNDD	RD9/RDP9	RDN8	TCLK8/TDN8	GNDA	GNDA	NC	TRING11	**E**
F	TTIP13	NC	GNDA	GNDA	VDDD	GNDD	GNDD	VDDD	NC	VDDD	GNDD	VDDIO	VDDD	VDDD	VDDD	VDDD	VDDD	VDDD	GNDA	GNDA	NC	TTIP11	**F**
G	TRING14	NC	RTIP12	RRING12	VDDD	VDDD	GNDD	GNDD	GNDD	GNDD	VDDD	GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	NC	RRING11	RTIP11	NC	TRING10	**G**
H	TTIP14	NC	RTIP13	RRING13	NC	VDDR12	GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	NC	RRING10	RTIP10	NC	TTIP10	**H**
J	TRING15	NC	RTIP14	RRING14	VDDT	VDDT	GNDT	GNDT	GNDT	GNDT	GNDT	GNDT	GNDT	GNDT	VDDR11	VDDT	VDDT	RRING9	RTIP9	NC		TRING9	**J**
K	TTIP15	NC	RTIP15	RRING15	VDDT	VDDT	GNDT	VDDR13	VDDR14	GNDT	GNDT	VDDR9	GNDT	VDDR10	GNDT	VDDT	VDDT	RRING8	RTIP8	NC		TTIP9	**K**
L	TRING0	NC	RTIP0	RRING0	VDDR0	VDDR15	VDDT	GNDT	VDDT	GNDT	GNDT	GNDT	VDDT	GNDT	VDDT	VDDR8	NC	VCOMEN	REF	NC		TRING8	**L**
M	TTIP0	NC	RTIP1	RRING1	VDDT	VDDT	VDDR2	GNDT	VDDR1	VDDT	GNDT	VDDA	GNDA	GNDT	VDDR7	VDDT	VDDA	VCOM1	VCOM0	GNDA		TTIP8	**M**
N	TRING1	NC	RTIP2	RRING2	VDDT	VDDT	VDDR3	GNDT	GNDT	GNDT	GNDT	VDDA	VDDT	NC	VDDT	VDDR6	VDDT	VDDT	RRING7	RTIP7	VDDA	TRING7	**N**
P	TTIP1	NC	RTIP3	RRING3	VDDT	VDDT	GNDT	VDDR4	GNDD	GNDD	NC	GNDD	VDDIO	NC	GNDD	VDDT	VDDR5	NC	RRING6	RTIP6	NC	TTIP7	**P**
R	TRING2	NC	RTIP4	RRING4	VDDT	VDDT	NC	NC	GNDD	VDDIO	VDDIO	VDDD	GNDD	VDDD	VDDD	VDDIO	GNDD	NC	RRING5	RTIP5	NC	TRING6	**R**
T	TTIP2	NC	GNDA	GNDA	NC	NC	VDDIO	VDDD	VDDD	GNDD	GNDD	GNDD	GNDD	GNDD	RDN6	VDDD	GNDD	VDDT	VDDT	GNDA	NC	TTIP6	**T**
U	TRING3	NC	GNDA	GNDA	NC	NC	VDDD	VDDD	GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	GNDD	NC	GNDA	GNDA	NC	TRING5	**U**
V	TTIP3	NC	GNDA	TD1/TDP1	RDN1	TCLK2/TDN2	TCLK3/TDN3	TCLK4/TDN4	RDN0	GPIO0	OE	TEHWE	$\overline{CS}$	CLKB	MCKSEL3	TCLK6/TDN6	TD7/TDP7	RDN7	TD6/TDP6	GNDA	GNDA	TTIP5	**V**
W	TRING4	NC	TCLK1/TDN1	RCLK1	TDN2	TD2/TDP2	RDN2	RDN3	RDN4	TCLK0/TDN0	TMS	TCK	SDI	NC	NC	MCKSEL1	TCLK5/TDN5	RCLK7	RDN5	IC	NC	NC	**W**
Y	TTIP4	RD1/RDP1	TDN1	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	GNDD	NC	NC	**Y**
AA	NC	RD2/RDP2	RCLK2	TD3/TDP3	RD3/RDP3	TD4/TDP4	RCLK4	RD0/RDP0	TDI	GPIO1	$\overline{RST}$	SDO	LLOS0	CLKA	MCKSEL2	TD5/TDP5	RCLK5	RD6/RDP6	TDN7	TCLK7/TDN7	RD7/RDP7	NC	**AA**
AB	TDN3	RCLK3	TDN4	RD4/RDP4	TD0/TDP0	TDN0	RCLK0	$\overline{TRST}$	TDO	TEHW	RIM	SCLK	$\overline{INT}$	LLOS	NC	CLKE1	MCKSEL0	MCLK	TDN5	RD5/RDP5	TDN6	RCLK6	**AB**
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

Figure-2   484-Pin Fine Pitch BGA (Top View)

2   PIN DESCRIPTION

Name	I / O	Pin No. [1]	Description
		Line Interface	
RTIPn RRINGn (n=0~15)	Input	L3, M3, N3, P3, R3, R20, P20, N20, K20, J20, H20, G20, G3, H3, J3, K3 L4, M4, N4, P4, R4, R19, P19, N19, K19, J19, H19, G19, G4, H4, J4, K4	**RTIPn / RRINGn: Receive Bipolar Tip/Ring for Channel 0 ~ 15** The receive line interface supports both Receive Differential mode and Receive Single Ended mode. In Receive Differential mode, the received signal is coupled into RTIPn and RRINGn via a 1:1 transformer or without a transformer (transformer-less). In Receive Single Ended mode, RRINGn should be left open. The received signal is input on RTIPn via a 2:1 (step down) transformer or without a transformer (transformer-less). These pins will become High-Z globally or channel specific in the following conditions: • Global High-Z: - Connecting the RIM pin to low; - Loss of MCLK - During and after power-on reset, hardware reset or global software reset; • Per-channel High-Z - Receiver power down by writing '1' to the R_OFF bit (b5, RCF0,...)
TTIPn TRINGn (n=0~15)	Output	M1, P1, T1, V1, Y1, V22, T22, P22, M22, K22, H22, F22, D1, F1, H1, K1 L1, N1, R1, U1, W1, U22, R22, N22, L22, J22, G22, E22, C1, E1, G1, J1	**TTIPn / TRINGn: Transmit Bipolar Tip /Ring for Channel 0 ~ 15** The transmit line interface supports both Transmit Differential mode and Transmit Single Ended mode. In Transmit Differential mode, TTIPn outputs a positive differential pulse while TRINGn outputs a negative differential pulse. The pulses are coupled to the line side via a 1:2 (step up) transformer or without a transformer (transformer-less). In Transmit Single Ended mode, TRINGn should be left open (it is shorted to ground internally). The signal presented at TTIPn is output to the line side via a 1:2 (step up) transformer. These pins will become High-Z globally or channel specific in the following conditions: • Global High-Z: - Connecting the OE pin to low; - Loss of MCLK; - During and after power-on reset, hardware reset or global software reset; • Per-channel High-Z - Writing '0' to the OE bit (b6, TCF0,...) [2]; - Loss of TCLKn in Transmit Single Rail NRZ Format mode or Transmit Dual Rail NRZ Format mode, except that the channel is in Remote Loopback or transmit internal pattern with XCLK [3]; - Transmitter power down by writing '1' to the T_OFF bit (b5, TCF0,...); - Per-channel software reset; - The THZ_OC bit (b4, TCF0,...) is set to '1' and the transmit driver over-current is detected. Refer to Section 3.3.8 Output High-Z on TTIP and TRING for details.

Note:
1. The pin number of the pins with the footnote 'n' is listed in order of channel (CH0 ~ CH15).
2. The content in the brackets indicates the position and the register name of the preceding bit. After the register name, if the punctuation ',...' is followed, this bit is in a per-channel register. The addresses and details are included in Chapter 5 Programming Information.
3. XCLK is derived from MCLK. It is 2.048 MHz in E1 mode.

Name	I / O	Pin No.	Description
			System Interface
RDn / RDPn (n=0~15)	Output	AA8, Y2, AA2, AA5, AB4, AB20, AA18, AA21, B18, E16, E14, E12, E11, E9, E7, A5	**RDn: Receive Data for Channel 0 ~ 15** When the receive system interface is configured to Single Rail NRZ Format mode, this multiplex pin is used as RDn. The decoded NRZ data is updated on the active edge of RCLKn. The active level on RDn is selected by the RD_INV bit (b3, RCF1,...). When the receiver is powered down, RDn will be in High-Z state or low, as selected by the RHZ bit (b6, RCF0,...). **RDPn: Positive Receive Data for Channel 0 ~ 15** When the receive system interface is configured to Dual Rail NRZ Format mode, Dual Rail RZ Format mode or Dual Rail Sliced mode, this multiplex pin is used as RDPn. In Receive Dual Rail NRZ Format mode, the un-decoded NRZ data is output on RDPn and RDNn and updated on the active edge of RCLKn. In Receive Dual Rail RZ Format mode, the un-decoded RZ data is output on RDPn and RDNn and updated on the active edge of RCLKn. In Receive Dual Rail Sliced mode, the raw RZ sliced data is output on RDPn and RDNn. For Receive Differential line interface, an active level on RDPn indicates the receipt of a positive pulse on RTIPn and a negative pulse on RRINGn; while an active level on RDNn indicates the receipt of a negative pulse on RTIPn and a positive pulse on RRINGn. For Receive Single Ended line interface, an active level on RDPn indicates the receipt of a positive pulse on RTIPn; while an active level on RDNn indicates the receipt of a negative pulse on RTIPn. The active level on RDPn and RDNn is selected by the RD_INV bit (b3, RCF1,...). When the receiver is powered down, RDPn and RDNn will be in High-Z state or low, as selected by the RHZ bit (b6, RCF0,...).
RDNn (n=0~15)	Output	V9, V5, W7, W8, W9, W19, T15, V18, E17, B16, B14, B12, B11, B9, B7, D6	**RDNn: Negative Receive Data for Channel 0 ~ 15** When the receive system interface is configured to Dual Rail NRZ Format mode, Dual Rail RZ Format mode or Dual Rail Sliced mode, this multiplex pin is used as RDNn. (Refer to the description of RDPn for details).
RCLKn (n=0~15)	Output	AB7, W4, AA3, AB2, AA7, AA17, AB22, W18, A18, A16, A14, A12, A11, A9, A7, E6	**RCLKn: Receive Clock for Channel 0 ~ 15** When the receive system interface is configured to Single Rail NRZ Format mode, Dual Rail NRZ Format mode or Dual Rail RZ Format mode, this multiplex pin is used as RCLKn. RCLKn outputs a 2.048 MHz (in E1 mode) clock which is recovered from the received signal. The data output on RDPn/RDNn (in Receive Dual Rail NRZ Format mode, Receive Dual Rail RZ Format mode and Receive Dual Rail Sliced) is updated on the active edge of RCLKn. The active edge is selected by the RCK_ES bit (b4, RCF1,...). In LLOS condition, RCLKn output high or XCLK, as selected by the RCKH bit (b7, RCF0,...) (refer to Section 3.5.3.1 Line LOS (LLOS) for details). When the receiver is powered down, RCLKn will be in High-Z state or low, as selected by the RHZ bit (b6, RCF0,...).
LLOS	Output	AB14	**LLOS: Receive Line Loss Of Signal** LLOS synchronizes with the output of CLKE1 and can indicate the LLOS (Line LOS) status of all 16 channels in a serial format. When the clock output on CLKE1 is enabled, LLOS indicates the LLOS status of the 16 channels in a serial format and repeats every seventeen cycles. The start filler is positioned by LLOS0. Refer to the description of LLOS0 below for details. LLOS is updated on the rising edge of CLKE1 and is always active high. When the clock output of CLKE1 is disabled, LLOS will be held in High-Z state. (Refer to Section 3.5.3.1 Line LOS (LLOS) for details.)

Name	I / O	Pin No.	Description
LLOS0	Output	AA13	**LLOS0: Receive Line Loss Of Signal for Start Position** LLOS0 can indicate the start position on the LLOS pin. When the clock output on CLKE1 is enabled, LLOS0 pulses high for one CLKE1 clock cycle to indicate the start position on the LLOS pin. When CLKE1 outputs 8 KHz clock, LLOS0 pulses high for one 8 KHz clock cycle (125 μs) every seventeen 8 KHz clock cycles; when CLKE1 outputs 2.048 MHz clock, LLOS0 pulses high for one 2.048 MHz clock cycle (488 ns) every seventeen 2.048 MHz clock cycles. LLOS0 is updated on the rising edge of CLKE1. When the clock output on CLKE1 is disabled, LLOS0 will be held in High-Z state. (Refer to Section 3.5.3.1 Line LOS (LLOS) for details.)
TDn / TDPn (n=0~15)	Input	AB5, V4, W6, AA4, AA6, AA16, V19, V17, D18, B17, B15, B13, B10, B8, B16, C5	**TDn: Transmit Data for Channel 0 ~ 15** When the transmit system interface is configured to Single Rail NRZ Format mode, this multiplex pin is used as TDn. TDn accepts Single Rail NRZ data. The data is sampled into the device on the active edge of TCLKn. The active level on TDn is selected by the TD_INV bit (b3, TCF1,...). **TDPn: Positive Transmit Data for Channel 0 ~ 15** When the transmit system interface is configured to Dual Rail NRZ Format mode or Dual Rail RZ Format mode, this multiplex pin is used as TDPn. In Transmit Dual Rail NRZ Format mode, the pre-encoded NRZ data is input on TDPn and TDNn and sampled on the active edge of TCLKn. In Transmit Dual Rail RZ Format mode, the pre-encoded RZ data is input on TDPn and TDNn. The line code is as follows (when the TD_INV bit (b3, TCF1,...) is '0'): _(see table below)_ The active level on TDPn and TDNn is selected by the TD_INV bit (b3, TCF1,...).
TDNn (n=0~15)	Input / Output	AB6, Y3, W5, AB1, AB3, AB19, AB21, AA19, C18, A17, A15, A13, A10, A8, A6, D5	**TDNn: Negative Transmit Data for Channel 0 ~ 15** When the transmit system interface is configured to Dual Rail NRZ Format mode, this multiplex pin is used as TDNn. (Refer to the description of TDPn for details).
TCLKn / TDNn (n=0~15)	Input	W10, W3, V6, V7, V8, W17, V16, AA20, E18, D16, D14, D12, D11, D9, D7, B5	**TCLKn: Transmit Clock for Channel 0 ~ 15** When the transmit system interface is configured to Single Rail NRZ Format mode or Dual Rail NRZ Format mode, this multiplex pin is used as TCLKn. TCLKn inputs a 2.048 MHz (in E1 mode) clock. The data input on TDn (in Transmit Single Rail NRZ Format mode) or TDPn/TDNn (in Transmit Dual Rail NRZ Format mode) is sampled on the active edge of TCLKn. **TDNn: Negative Transmit Data for Channel 0 ~ 15** When the transmit system interface is configured to Dual Rail RZ Format mode, this multiplex pin is used as TDNn. (Refer to the description of TDPn for details).

The line code table referenced in the TDPn description:

TDPn	TDNn	Output Pulse on TTIPn	Output Pulse on TRINGn *
0	0	Space	Space
0	1	Negative Pulse	Positive Pulse
1	0	Positive Pulse	Negative Pulse
1	1	Space	Space

Note:
* For Transmit Single Ended line interface, TRINGn should be open.

Name	I / O	Pin No.	Description
			**Clock**
MCLK	Input	AB18	**MCLK: Master Clock Input** MCLK provides a stable reference timing for the IDT82P20516. MCLK should be a clock with +/-50 ppm (in E1 mode) accuracy. The clock frequency of MCLK is informed to the device by MCKSEL[3:0]. If MCLK misses (duty cycle is less than 30% for 10 μs) and then recovers, the device will be reset automatically.
MCKSEL[0] MCKSEL[1] MCKSEL[2] MCKSEL[3]	Input	AB17 W16 AA15 V15	**MCKSEL[3:0]: Master Clock Selection** These four pins inform the device of the clock frequency input on MCLK:

MCKSEL[3:0][*]	Frequency (MHz)
0000	1.544
0001	1.544 X 2
0010	1.544 X 3
0011	1.544 X 4
0100	1.544 X 5
0101	1.544 X 6
0110	1.544 X 7
0111	1.544 X 8
1000	2.048
1001	2.048 X 2
1010	2.048 X 3
1011	2.048 X 4
1100	2.048 X 5
1101	2.048 X 6
1110	2.048 X 7
1111	2.048 X 8

Note:
0: GNDD
1: VDDIO

Name	I / O	Pin No.	Description
CLKE1	Output	AB16	**CLKE1: 8 KHz / E1 Clock Output** The output on CLKE1 can be enabled or disabled, as determined by the CLKE1_EN bit (b3, CLKG). When the output is enabled, CLKE1 outputs an 8 KHz or 2.048 MHz clock, as selected by the CLKE1 bit (b2, CLKG). The output is locked to MCLK. When the output is disabled, CLKE1 is in High-Z state.
CLKA	Input	AA14	**CLKA: External E1 Clock Input A** External E1 (2.048 MHz) clock is input on this pin. When not used, this pin should be connected to GNDD.
CLKB	Input	V14	**CLKB: External E1 Clock Input B** External E1 (2.048 MHz) clock is input on this pin. When not used, this pin should be connected to GNDD.

Name	I / O	Pin No.	Description
Common Control			
VCOM[0] VCOM[1]	Output	M20 M19	**VCOM: Voltage Common Mode [1:0]** These pins are used only when the receive line interface is in Receive Differential mode and connected without a transformer (transformer-less). To enable these pins, the VCOMEN pin must be connected high. Refer to Figure-6 for the connection. When these pins are not used, they should be left open.
VCOMEN	Input (Pull-Down)	L19	**VCOMEN: Voltage Common Mode Enable** This pin should be connected high only when the receive line interface is in Receive Differential mode and connected without a transformer (transformer-less). When not used, this pin should be left open.
REF	-	L20	**REF: Reference Resistor** An external resistor (10 KΩ, ±1%) is used to connect this pin to ground to provide a standard reference current for internal circuit. This resistor is required to ensure correct device operation.
RIM	Input (Pull-Down)	AB11	**RIM: Receive Impedance Matching** In Receive Differential mode, when RIM is low, all 16 receivers become High-Z and only external impedance matching is supported. In this case, the per-channel impedance matching configuration bits - the R_TERM[2:0] bits (b2~0, RCF0,...) and the R120IN bit (b4, RCF0,...) - are ignored. In Receive Differential mode, when RIM is high, impedance matching is configured on a per-channel basis by the R_TERM[2:0] bits (b2~0, RCF0,...) and the R120IN bit (b4, RCF0,...). This pin can be used to control the receive impedance state for Hitless Protection applications. Refer to Section 4.4 Hitless Protection Switching (HPS) Summary for details. In Receive Single Ended mode, this pin should be left open.
OE	Input	V11	**OE: Output Enable** OE enables or disables all Line Drivers globally. A high level on this pin enables all Line Drivers while a low level on this pin places all Line Drivers in High-Z state and independent from related register settings. Note that the functionality of the internal circuit is not affected by OE. If this pin is not used, it should be tied to VDDIO. This pin can be used to control the transmit impedance state for Hitless protection applications. Refer to Section 4.4 Hitless Protection Switching (HPS) Summary for details.
TEHWE	Input (Pull-Up)	V12	**TEHWE: Hardware E1 Mode Selection Enable** When this pin is open, the E1 operation mode is selected by TEHW globally. When this pin is low, the E1 operation mode is selected by the E1 bit (b0, CHCF,...) on a per-channel basis.
TEHW	Input (Pull-Up)	AB10	**TEHW: Hardware E1 Mode Selection** When TEHWE is open, this pin selects the E1 operation mode globally: Low - E1 mode; When TEHWE is low, the input on this pin is ignored.
GPIO[0] GPIO[1]	Output / Input	V10 AA10	**GPIO: General Purpose I/O [1:0]** These two pins can be defined as input pins or output pins by the DIR[1:0] bits (b1~0, GPIO) respectively. When the pins are input, their polarities are indicated by the LEVEL[1:0] bits (b3~2, GPIO) respectively. When the pins are output, their polarities are controlled by the LEVEL[1:0] bits (b3~2, GPIO) respectively.
$\overline{\text{RST}}$	Input	AA11	**$\overline{\text{RST}}$: Reset (Active Low)** A low pulse on this pin resets the device. This hardware reset process completes in 2 µs maximum. Refer to Section 4.1 Reset for an overview on reset options.

Name	I / O	Pin No.	Description
		MCU Interface	
$\overline{INT}$	Output	AB13	**$\overline{INT}$: Interrupt Request** This pin indicates interrupt requests for all unmasked interrupt sources. The output characteristics (open drain or push-pull internally) and the active level are determined by the INT_PIN[1:0] bits (b3~2, GCF).
$\overline{CS}$	Input	V13	**$\overline{CS}$: Chip Select (Active Low)** This pin must be asserted low to enable the microprocessor interface. A transition from high to low must occur on this pin for each Read/Write operation and $\overline{CS}$ should remain low until the operation is over.
SCLK	Input	AB12	**SCLK: Shift Clock** In Serial microprocessor interface, this multiplex pin is used as SCLK. SCLK inputs the shift clock for the Serial microprocessor interface. Data on SDI is sampled by the device on the rising edge of SCLK. Data on SDO is updated on the falling edge of SCLK.
SDI	Input	W13	**SDI: Serial Data Input** In Serial microprocessor interface, this multiplex pin is used as SDI. Address and data on this pin are serially clocked into the device on the rising edge of SCLK.
SDO	Output	AA12	**SDO: Serial Data Output** In Serial microprocessor interface, this multiplex pin is used as SDO. Data on this pin is serially clocked out of the device on the falling edge of SCLK.
		JTAG (per IEEE 1149.1)	
$\overline{TRST}$	Input Pull-Down	AB8	**$\overline{TRST}$: JTAG Test Reset (Active Low)** A low signal on this pin resets the JTAG test port. To ensure deterministic operation of the test logic, TMS should be held high when the signal on $\overline{TRST}$ changes from low to high. This pin may be left unconnected when JTAG is not used. This pin has an internal pull-down resistor.
TMS	Input Pull-up	W11	**TMS: JTAG Test Mode Select** The signal on this pin controls the JTAG test performance and is sampled on the rising edge of TCK. To ensure deterministic operation of the test logic, TMS should be held high when the signal on $\overline{TRST}$ changes from low to high. This pin may be left unconnected when JTAG is not used. This pin has an internal pull-up resistor.
TCK	Input	W12	**TCK: JTAG Test Clock** The clock for the JTAG test is input on this pin. TDI and TMS are sampled on the rising edge of TCK and TDO is updated on the falling edge of TCK. When TCK is idle at low state, all stored-state devices contained in the test logic shall retain their state indefinitely. This pin should be connected to GNDD when JTAG is not used.
TDI	Input Pull-up	AA9	**TDI: JTAG Test Data Input** The test data is input on this pin. It is clocked into the device on the rising edge of TCK. This pin has an internal pull-up resistor. This pin may be left unconnected when JTAG is not used.
TDO	Output	AB9	**TDO: JTAG Test Data Output** The test data is output on this pin. It is clocked out of the device on the falling edge of TCK. TDO is a High-Z output signal except during the process of data scanning.
		Power & Ground	
VDDIO		D8, D13, D15, D17, E10, F12, P13, R10, R11, R16, T7	**VDDIO: 3.3 V I/O Power Supply**
VDDA		N21, M12, N12, M18	**VDDA: 3.3 V Analog Core Power Supply**

Name	I / O	Pin No.	Description
VDDD		F5, F8, F10, F13, F14, F15, F16, F17, F18, G5, G6, G11, R12, R14, R15, T8, T9, T16, U8, U9	**VDDD: 1.8 V Digital Core Power Supply**
VDDRn (N=0~15)		H6, J16, K8, K9, K13, K15, L5, L6, L17, M7, M9, M16, N7, N16, P8, P17	**VDDRn: 3.3 V Power Supply for Receiver**
VDDT		J5, J6, J17, J18, K5, K6, K17, K18, L7, L9, L13, L16, M5, M6, M10, M17, N5, N6, N13, N15, N17, N18, P5, P6, R5, R6, T18, T19	**VDDT: 3.3 V Power Supply for Transmitter Driver**
GNDA		E2, E3, E4, E19, E20, F3, F4, F19, F20, M13, M21, T3, T4, T20, U3, U4, U19, U20, V3, V20, V21	**GNDA: GND for Analog Core / Receiver**
GNDD		C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, D10, E8, E13, E15, F6, F7, F11, G7, G8, G9, G10, G12, G13, G14, G15, G16, G17, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, H17, P9, P10, P12, P15, R9, R13, R17, T10, T11, T12, T13, T14, T17, U10, U11, U12, U13, U14, U15, U16, U17, Y20	**GNDD: Digital GND**
GNDT		J7, J8, J9, J10, J11, J12, J13, J14, J15, K7, K10, K11, K12, K14, K16, L8, L10, L11, L12, L14, L15, M8, M11, M14, M15, N8, N9, N10, N11, P7, P16	**GNDT: Analog GND for Transmitter Driver**
TEST			
NC	-	A1, A2, A3, A4, A19, A20, A21, A22, B1, B2, B3, B4, B19, B20, B21, B22, C2, C3, C4, C19, C20, C21, C22, D2, D3, D4, D19, D20, D21, D22, E5, E21, F2, F9, F21, G2, G18, G21, H2, H5, H18, H21, J2, J21, K2, K21, L2, L18, L21, M2, N2, N14, P2, P11, P14, P18, P21, R2, R7, R8, R18, R21, T2, T5, T6, T21, U2, U5, U6, U7, U18, U21, V2, W2, W21, W22, Y4, Y5, Y6, Y7, Y8, Y9, Y10, Y11, Y12, Y13, Y14, Y15, Y16, Y17, Y18, Y19, Y21, Y22, AA1, AA22, AB15, W14, W15	**NC: No Connected** These pins should be left open.
Others			
IC		W20	**IC: Internal Connected** This pin is for IDT use only and should be connected to GNDD.

3   FUNCTIONAL DESCRIPTION

3.1   E1 MODE SELECTION

The IDT82P20516 can be configured to E1 mode globally or on a per-channel basis. The configuration is determined by the TEHWE pin, the TEHW pin and the E1 bit (b0, CHCF,...). Refer to Table-1 for details of the operation mode selection.

Table-1   Operation Mode Selection

	Global Programming		Per-Channel Programming	
TEHWE Pin	Open		Low	
TEHW Pin	Open	Low	(The configuration of this pin is ignored)	
E1 Bit	(The configuration of this bit is ignored).		0	1
Operation Mode		E1		E1

3.2   RECEIVE PATH

3.2.1   R$_X$ TERMINATION

The receive line interface supports Receive Differential mode. In Receive Differential mode, both RTIPn and RRINGn are used to receive signal from the line side.

In Receive Differential mode, the line interface can be connected with E1 120 Ω twisted pair cable or E1 75 Ω coaxial cable.

The receive impedance matching is realized by using internal impedance matching or external impedance matching for each channel in different applications.

3.2.1.1   Receive Differential Mode

In Receive Differential mode, three kinds of impedance matching are supported: Fully Internal Impedance Matching, Partially Internal Impedance Matching and External Impedance Matching. Figure-3 shows an overview of how these Impedance Matching modes are switched.

Fully Internal Impedance Matching circuit uses an internal programmable resistor (IM) only and does not use an external resistor. This configuration saves external components and supports 1:1 Hitless Protection Switching (HPS) applications without relays. Refer to Section 4.4 Hitless Protection Switching (HPS) Summary.

Partially Internal Impedance Matching circuit consists of an internal programmable resistor (IM) and a value-fixed 120 Ω external resistor (Rr). Compared with Fully Internal Impedance Matching, this configuration provides considerable savings in power dissipation of the device. For example, In E1 120 Ω PRBS mode, the power savings would be 0.44 W. For power savings in other modes, please refer to Chapter 8 Physical And Electrical Specifications.

External Impedance Matching circuit uses an external resistor (Rr) only.
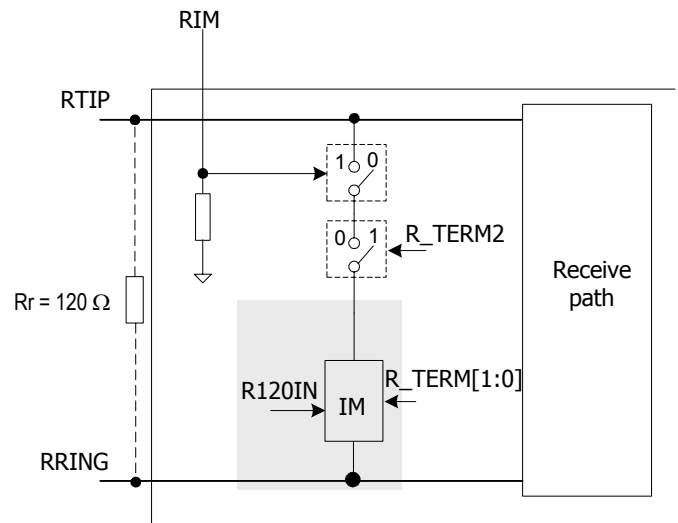
Figure-3   Switch between Impedance Matching Modes

To support some particular applications, such as hot-swap or Hitless Protection Switch (HPS) hot-switchover, RTIPn/RRINGn must be forced to enter high impedance state (i.e., External Impedance Matching). For hot-swap, RTIPn/RRINGn must be always held in high impedance state during /after power up; for HPS hot-switchover, RTIPn/RRINGn must enter high impedance state immediately after switchover. Though each channel can be individually configured to External Impedance Matching through register access, it is too slow for hitless switch. Therefore, a hardware pin - RIM - is provided to globally control the high impedance for all 16 receivers.

When RIM is low, only External Impedance Matching is supported for all 16 receivers and the per-channel impedance matching configuration bits - the R_TERM[2:0] bits (b2~0, RCF0,...) and the R120IN bit (b4, RCF0,...) - are ignored.

When RIM is high, impedance matching is configured on a per-channel basis. Three kinds of impedance matching are all supported and selected by the R_TERM[2:0] bits (b2~0, RCF0,...) and the R120IN bit (b4, RCF0,...). The R_TERM[2] bit (b2, RCF0,...) should be set to match internal or external impedance. If the R_TERM[2] bit (b2, RCF0,...) is '0', internal impedance matching is enabled. The R120IN bit (b4, RCF0,...) should be set to select Partially Internal Impedance Matching or Fully Internal Impedance Matching. The internal programmable resistor (IM) is determined by the R_TERM[1:0] bits (b1~0, RCF0,...). If the R_TERM[2] bit (b2, RCF0,...) is '1', external impedance matching is enabled. The configuration of the R120IN bit (b4, RCF0,...) and the R_TERM[1:0] bits (b1~0, RCF0,...) is ignored.

A twisted pair cable can be connected with a 1:1 transformer or without a transformer (transformer-less), while a coaxial cable must be connected with a 1:1 transformer. Table 2 lists the recommended impedance matching value in different applications. Figure-4 to Figure-6 show the connection for one channel.

The transformer-less connection will offer a termination option with reduced cost and board space. However, the waveform amplitude is not standard compliant, and surge protection and common mode depression should be enhanced depending on equipment environment.

Table-2　Impedance Matching Value in Receive Differential Mode

Cable Condition	Partially Internal Impedance Matching (R120IN = 0) [1]		Fully Internal Impedance Matching (R120IN = 1) [1, 2]		External Impedance Matching	
	R_TERM[2:0]	Rr	R_TERM[2:0]	Rr	R_TERM[2:0] [3]	Rr
E1 120 Ω twisted pair (with transformer)	010	120 Ω	010	(open)	1XX	120 Ω
E1 75 Ω coaxial (with transformer)	011		011			75 Ω
E1 120 Ω twisted pair (transformer-less)	010		(not supported)			120 Ω

Note:
1. Partially Internal Impedance Matching and Fully Internal Impedance Matching are not supported when RIM is low.
2. Fully Internal Impedance Matching is not supported in transformer-less applications.
3. When RIM is low, the setting of the R_TERM[2:0] bits is ignored.
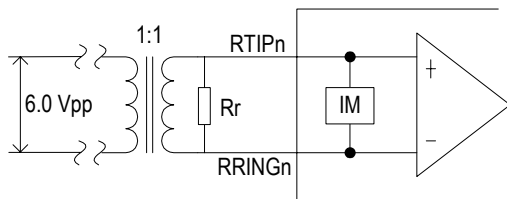
Figure-4　Receive Differential Line Interface with Twisted Pair Cable (with transformer)

Figure-5　Receive Differential Line Interface with Coaxial Cable (with transformer)

Note: 1. Two Rr/2 resistors should be connected to VCOM[1:0] that are coupled to ground via a 10 μF capacitor, which provide 60 Ω common mode input resistance.
2. In this mode, lightning protection should be enhanced.
3. The maximum input dynamic range of RTIP/TRING pin is -0.3 V ~3.6 V (in line monitor mode it is -0.3 V ~ 2 V)

Figure-6　Receive Differential Line Interface with Twisted Pair Cable (transformer-less, non standard compliant)
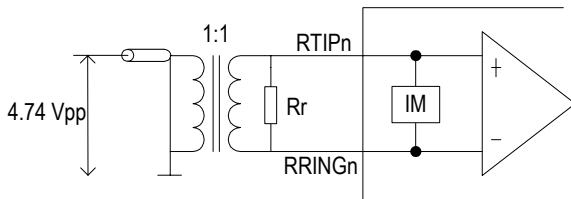
3.2.2　EQUALIZER

The equalizer compensates high frequency attenuation to enhance receive sensitivity.

3.2.2.1 Line Monitor

In both E1 short haul applications, the Protected Non-Intrusive Monitoring can be performed between two devices. The monitored channel of one device is in normal operation, and the monitoring channel of the other device taps the monitored one through a high impedance bridging circuit (refer to Figure-7 and Figure-8).

After the high resistance bridging circuit, the signal arriving at RTIPn/RRINGn of the monitoring channel is dramatically attenuated. To compensate this bridge resistive attenuation, Monitor Gain can be used to boost the signal by 20 dB, 26 dB or 32 dB, as selected by the MG[1:0] bits (b1~0, RCF2,...). For normal operation, the Monitor Gain should be set to 0 dB, i.e., the Monitor Gain of the monitored channel should be 0 dB.

The monitoring channel can be configured to any of the External, Partially Internal or Fully Internal Impedance Matching mode. Here the external r or internal IM is used for voltage division, not for impedance matching. That is, the r (IM) and the two R make up of a resistance bridge. The resistive attenuation of this bridge is $20lg(r/(2R+r))$ dB.

Note that line monitor is only available in differential line interface.

3.2.2.2 Receive Sensitivity

The receive sensitivity is the minimum range of receive signal level for which the receiver recovers data error-free with -18 dB interference signal added.

For Receive Differential line interface, the receive sensitivity is -15 dB.

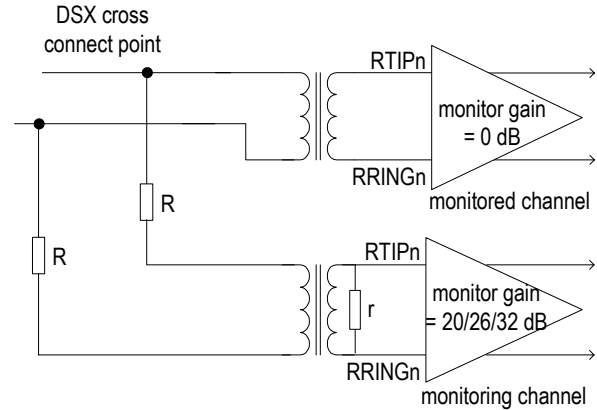For Receive Single Ended line interface, the receive sensitivity is -12 dB.
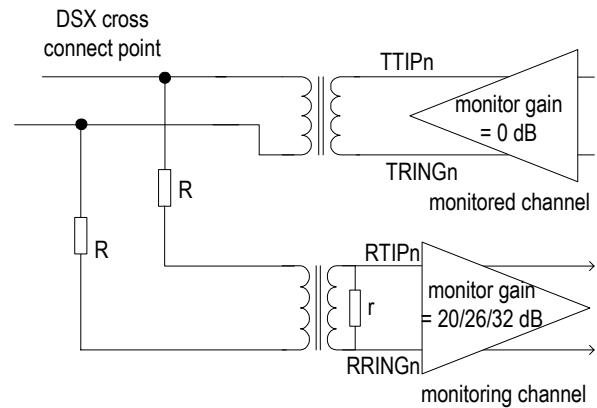

Figure-7   Receive Path Monitoring

Figure-8   Transmit Path Monitoring

3.2.3   SLICER

The Slicer is used to generate a standard amplitude mark or a space according to the amplitude of the input signals. The input signal is sliced at 50% of the peak value.

3.2.4   R$_X$ CLOCK & DATA RECOVERY

The Rx Clock & Data Recovery is used to recover the clock signal from the received data. It is accomplished by an integrated Digital Phase Locked Loop (DPLL). The recovered clock tracks the jitter in the data output from the Slicer and keeps the phase relationship between data and clock during the absence of the incoming pulse.

3.2.5   DECODER

The Decoder is used only when the receive system interface is in Single Rail NRZ Format mode. When the receive system interface is in other modes, the Decoder is bypassed automatically. (Refer to Section 3.2.6 Receive System Interface for the description of the receive system interface).

In E1 mode, the received signal is decoded by AMI or HDB3 line code rule. The line code rule is selected by the R_CODE bit (b2, RCF1,...).

3.2.6   RECEIVE SYSTEM INTERFACE

The received data can be output to the system side in four modes: Single Rail NRZ Format mode, Dual Rail NRZ Format mode, Dual Rail RZ Format mode and Dual Rail Sliced mode, as selected by the R_MD[1:0] bits (b1~0, RCF1).

If data is output on RDn in NRZ format and the recovered clock is output on RCLKn, the receive system interface is in Single Rail NRZ Format mode. In this mode, the data is decoded and updated on the active edge of RCLKn. RCLKn outputs a 2.048 MHz (in E1 mode) clock.

If data is output on RDPn and RDNn in NRZ format and the recovered clock is output on RCLKn, the receive system interface is in Dual Rail NRZ Format mode. In this mode, the data is un-decoded and updated on the active edge of RCLKn. RCLKn outputs a 2.048 MHz (in E1 mode) clock.

If data is output on RDPn and RDNn in RZ format and the recovered clock is output on RCLKn, the receive system interface is in Dual Rail RZ Format mode. In this mode, the data is un-decoded and updated on the active edge of RCLKn. RCLKn outputs a 2.048 MHz (in E1 mode) clock.

If data is output on RDPn and RDNn in RZ format directly after passing through the Slicer, the receive system interface is in Dual Rail Sliced mode. In this mode, the data is raw sliced and un-decoded.

Table-3 summarizes the multiplex pin used in different receive system interface.

Table-3   Multiplex Pin Used in Receive System Interface

Receive System Interface	Multiplex Pin Used On Receive System Interface		
	RDn / RDPn	**RDNn**	**RCLKn**
Single Rail NRZ Format	RDn [1]		RCLKn [2]
Dual Rail NRZ Format	RDPn [1]	RDNn [1]	RCLKn [2]
Dual Rail RZ Format	RDPn [1]	RDNn [1]	RCLKn [2]
Dual Rail Sliced	RDPn [1]	RDNn [1]	
Note:			
1. The active level on RDn, RDPn and RDNn is selected by the RD_INV bit (b3, RCF1,...). **2.** The active edge of RCLKn is selected by the RCK_ES bit (b4, RCF1,...).			

3.2.7   RECEIVER POWER DOWN

Set the R_OFF bit (b5, RCF0,...) to '1' will power down the corresponding receiver.

In this way, the corresponding receive circuit is turned off and the RTIPn/RRINGn pins are forced to High-Z state. The pins on receive system interface (including RDn/RDPn, RDNn, RCLKn) will be in High-Z state if the RHZ bit (b6, RCF0,...) is '1' or in low level if the RHZ bit (b6, RCF0,...) is '0'.

After clearing the R_OFF bit (b5, RCF0,...), it will take 1 ms for the receiver to achieve steady state, i.e., to return to the previous configuration and performance.

3.3   TRANSMIT PATH

3.3.1   TRANSMIT SYSTEM INTERFACE

The data from the system side is input to the device in three modes: Single Rail NRZ Format mode, Dual Rail NRZ Format mode and Dual Rail RZ Format mode, as selected by the T_MD[1:0] bits (b1~0, TCF1,...).

If data is input on TDn in NRZ format and a 2.048 MHz (in E1 mode) clock is input on TCLKn, the transmit system interface is in Single Rail NRZ Format mode. In this mode, the data is encoded and sampled on the active edge of TCLKn.

If data is input on TDPn and TDNn in NRZ format and a 2.048 MHz (in E1 mode) clock is input on TCLKn, the transmit system interface is in Dual Rail NRZ Format mode. In this mode, the data is pre-encoded and sampled on the active edge of TCLKn.

If data is input on TDPn and TDNn in RZ format and no transmit clock is input, the transmit system interface is in Dual Rail RZ Format mode. In this mode, the data is pre-encoded.

Table-4 summarizes the multiplex pin used in different transmit system interface.

Table-4　Multiplex Pin Used in Transmit System Interface

Transmit System Interface	Multiplex Pin Used On Transmit System Interface		
	TDn / TDPn	TDNn	TCLKn / TDNn
Single Rail NRZ Format	TDn [1]		TCLKn [2]
Dual Rail NRZ Format	TDPn [1]	TDNn [1]	TCLKn [2]
Dual Rail RZ Format	TDPn [1]		TDNn [1]

Note:
1. The active level on TDn, TDPn and TDNn is selected by the TD_INV bit (b3, TCF1,...).
2. The active edge of TCLKn is selected by the TCK_ES bit (b4, TCF1,...). If TCLKn is missing, i.e., no transition for more than 64 E1 clock cycles, the TCKLOS_S bit (b3, STAT0,...) will be set. A transition from '0' to '1' on the TCKLOS_S bit (b3, STAT0,...) or any transition (from '0' to '1' or from '1' to '0') on the TCKLOS_S bit (b3, STAT0,...) will set the TCKLOS_IS bit (b3, INTS0,...) to '1', as selected by the TCKLOS_IES bit (b3, INTES,...). When the TCKLOS_IS bit (b3, INTS0,...) is '1', an interrupt will be reported by $\overline{\text{INT}}$ if not masked by the TCKLOS_IM bit (b3, INTM0,...).

3.3.2　T$_X$ CLOCK RECOVERY

The Tx Clock Recovery is used only when the transmit system interface is in Dual Rail RZ Format mode. When the transmit system interface is in other modes, the Tx Clock Recovery is bypassed automatically.

The Tx Clock Recovery is used to recover the clock signal from the data input on TDPn and TDNn.

3.3.3　ENCODER

The Encoder is used only when the transmit system interface is in Single Rail NRZ Format mode. When the transmit system interface is in other modes, the Encoder is bypassed automatically.

In E1 mode, the data to be transmitted is encoded by AMI or HDB3 line code rule. The line code rule is selected by the T_CODE bit (b2, TCF1,...).

3.3.4　WAVEFORM SHAPER

The IDT82P20516 provides two ways to manipulate the pulse shape before data is transmitted:
- Preset Waveform Template;
- User-Programmable Arbitrary Waveform.

3.3.4.1　Preset Waveform Template

In E1 applications, the waveform template meets G.703, as shown in Figure-9. It is measured in the near end line side, as shown in Figure-10.

In E1 applications, the PULS[3:0] should be set to '0000' if differential signals (output from TTIP and TRING) are coupled to a 75 Ω coaxial cable using Internal Impedance matching mode; the PULS[3:0] should be set to '0001' for other E1 interfaces. Refer to Table-5 for details.
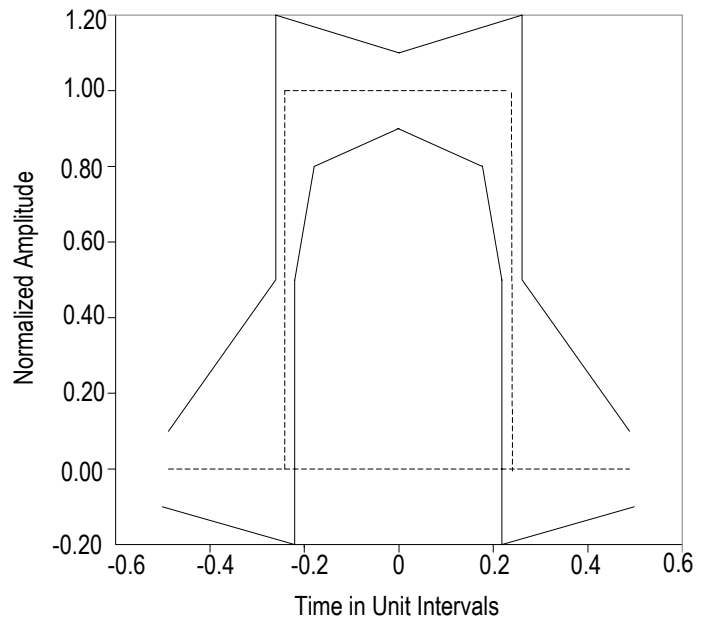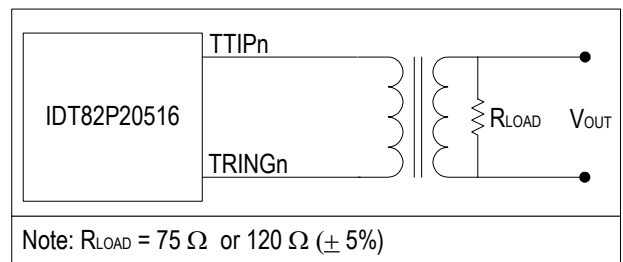

Figure-9　E1 Waveform Template

Note: R$_{LOAD}$ = 75 Ω or 120 Ω ($\pm$ 5%)

Figure-10　E1 Waveform Template Measurement Circuit

Table-5 PULS[3:0] Setting in E1 Mode

Interface Conditions	PULS[3:0]
E1 75 Ω differential interface, Internal Impedance matching mode	0000
Other E1 interface	0001

After one of the preset waveform templates is selected, the preset waveform amplitude can be adjusted to get the desired waveform.

In E1 mode, the SCAL[5:0] bits (b5~0, SCAL,...) should be set to '100001' to get the standard amplitude. The adjusting is made by increasing or decreasing by '1' from the standard value to scale up or down at a percentage ratio of 3%.

In summary, do the following step by step, the desired waveform will be got based on the preset waveform template:
- Select one preset waveform template by setting the PULS[3:0] bits (b3~0, PULS,...);
- Write '100001 to the SCAL[5:0] bits (b5~0, SCAL,...) if E1 mode is selected.
- Write the scaling value to the SCAL[5:0] bits (b5~0, SCAL,...) to scale the amplitude of the selected preset waveform template (- this step is optional).

3.3.4.2 User-Programmable Arbitrary Waveform

When the PULS[3:0] bits (b3~0, PULS,...) are set to '1XXX', user-programmable arbitrary waveform will be used in the corresponding channel.

Each waveform shape can extend up to $1\frac{1}{4}$ UIs (Unit Interval), and is divided into 20 sub-phases that are addressed by the SAMP[4:0] bits (b4~0, AWG0,...). The waveform amplitude of each phase is represented by a binary byte, within the range from +63 to -63, stored in the WDAT[6:0] bits (b6~0, AWG1,...) in signed magnitude form. The maximum number +63 (D) represents the maximum positive amplitude of the transmit pulse while the most negative number -63 (D) represents the maximum negative amplitude of the transmit pulse. Therefore, up to 20 bytes are used.

There are eight standard templates which are stored in a local ROM. One of them can be selected as reference and made some changes to get the desired waveform.

To do this, the first step is to choose a set of waveform value from the standard templates. The selected waveform value should be the most similar to the desired waveform shape. Table-6 to Table-7 list the sample data of each template.

Then modify the sample data to get the desired transmit waveform shape. By increasing or decreasing by '1' from the standard value in the SCAL[5:0] bits (b5~0, SCAL,...), the waveform amplitude will be scaled up or down.

In summary, do the following for the write operation:
- Modify the sample data in the AWG1 register;
- Write the AWG0 register to implement the write operation, including:
  - Write the sample address to the SAMP[4:0] bits (b4~0, AWG0,...);
  - Write '0' to the RW bit (b5, AWG0,...);
  - Write '1' to the DONE bit (b6, AWG0,...).

Do the following for the read operation:
- Write the AWG0 register, including:
  - Write sample address to the SAMP[4:0] bits (b4~0, AWG0,...);
  - Write '1' to the RW bit (b5, AWG0,...);
  - Write '1' to the DONE bit (b6, AWG0,...);
- Read the AWG1 register to get the sample data.

When the write operation is completed, write the scaling value to the SCAL[5:0] bits (b5~0, SCAL,...) to scale the amplitude of the selected standard waveform (- this step is optional).

When more than one UI is used to compose the waveform template and the waveform amplitude is not set properly, the overlap of the two consecutive waveforms will make the waveform amplitude overflow (i.e., exceed the maximum limitation). This overflow is captured by the DAC_IS bit (b7, INTS0,...) and will be reported by the $\overline{INT}$ pin if enabled by the DAC_IM bit (b7, INTM0,...).