Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Single T1/E1/J1 Long Haul / Short Haul Transceiver

IDT82P2281

Version 11
August 20, 2009

6024 Silver Creek Valley Road, San Jose, CA 95138
Telephone: (800) 345-7015 • TWX: 910-338-2070 • FAX: (408) 284-2775
Printed in U.S.A.

Table of Contents

List of Tables

List of Figures

Single T1/E1/J1 Long Haul / Short Haul Transceiver

IDT82P2281

FEATURES

LINE INTERFACE

- The device can be configured as T1, E1 or J1
- Supports T1/E1/J1 long haul/short haul line interface
- HPS for 1+1 protection without external relays
- Receive sensitivity exceeds -36 dB @ 772 Hz and -43 dB @ 1024 Hz
- Selectable internal line termination impedance: 100 Ω (for T1), 75 Ω / 120 Ω (for E1) and 110 Ω (for J1)
- Supports AMI/B8ZS (for T1/J1) and AMI/HDB3 (for E1) line encoding/decoding
- Provides T1/E1/J1 short haul pulse templates, long haul LBO (per ANSI T1.403 and FCC68: 0 dB, -7.5 dB, -15 dB, -22 dB) and user-programmable arbitrary pulse template
- Supports T1.102 line monitor
- Transmit line short-circuit detection and protection
- Separate Transmit and Receive Jitter Attenuators (2 per link)
- Indicates the interval between the write pointer and the read pointer of the FIFO in JA
- Loss of signal indication with programmable thresholds according to ITUT-T G.775, ETS 300 233 (E1) and ANSI T1.403 (T1/J1)
- Supports Analog Loopback, Digital Loopback and Remote Loopback
- The receiver and transmitter can be individually powered down

FRAMER

- The device can be configured as T1, E1 or J1
- Frame alignment/generation for T1 (per ITU-T G.704, TA-TSY-000278, TR-TSY-000008), E1 (per ITU-T G.704), J1 (per JT G.704) and un-framed mode
- Supports T1/J1 Super Frame and Extended Super Frame, T1 Digital Multiplexer and Switch Line Carrier - 96, E1 CRC Multi-frame and Signaling Multi-frame
- Signaling extraction/insertion for CAS and RBS signaling
- Provides programmable system interface supporting Mitel™ ST-bus, AT&T™ CHI and MVIP bus, 8.192 Mb/s multiplexed bus and 1.544 Mb/s or 2.048 Mb/s non-multiplexed bus
- Three HDLC controllers with separate 128-byte transmit and receive FIFOs per controller
- Programmable bit insertion and bit inversion on per channel/ timeslot basis
- Provides Bit Oriented Message (BOM) generation and detection
- Provides Automatic Performance Report Message (APRM) generation
- Detects and generates alarms (AIS, RAI)
- Provides performance monitor to count Bipolar Violation error, Excess Zero error, CRC error, framing bit error, far end CRC error, out of frame and change of framing alignment position
- Supports System Loopback, Payload Loopback, Digital Loopback and Inband Loopback
- Detects and generates selectable PRBS and QRSS
- Transmission and Extraction of Synchronization Supply Message (SSM) in BITS application

CONTROL INTERFACE

- Supports Serial Peripheral Interface (SPI) microprocessor and parallel Intel/Motorola non-multiplexed microprocessor interface
- Global hardware and software reset
- One general purpose I/O pin
- Device power down

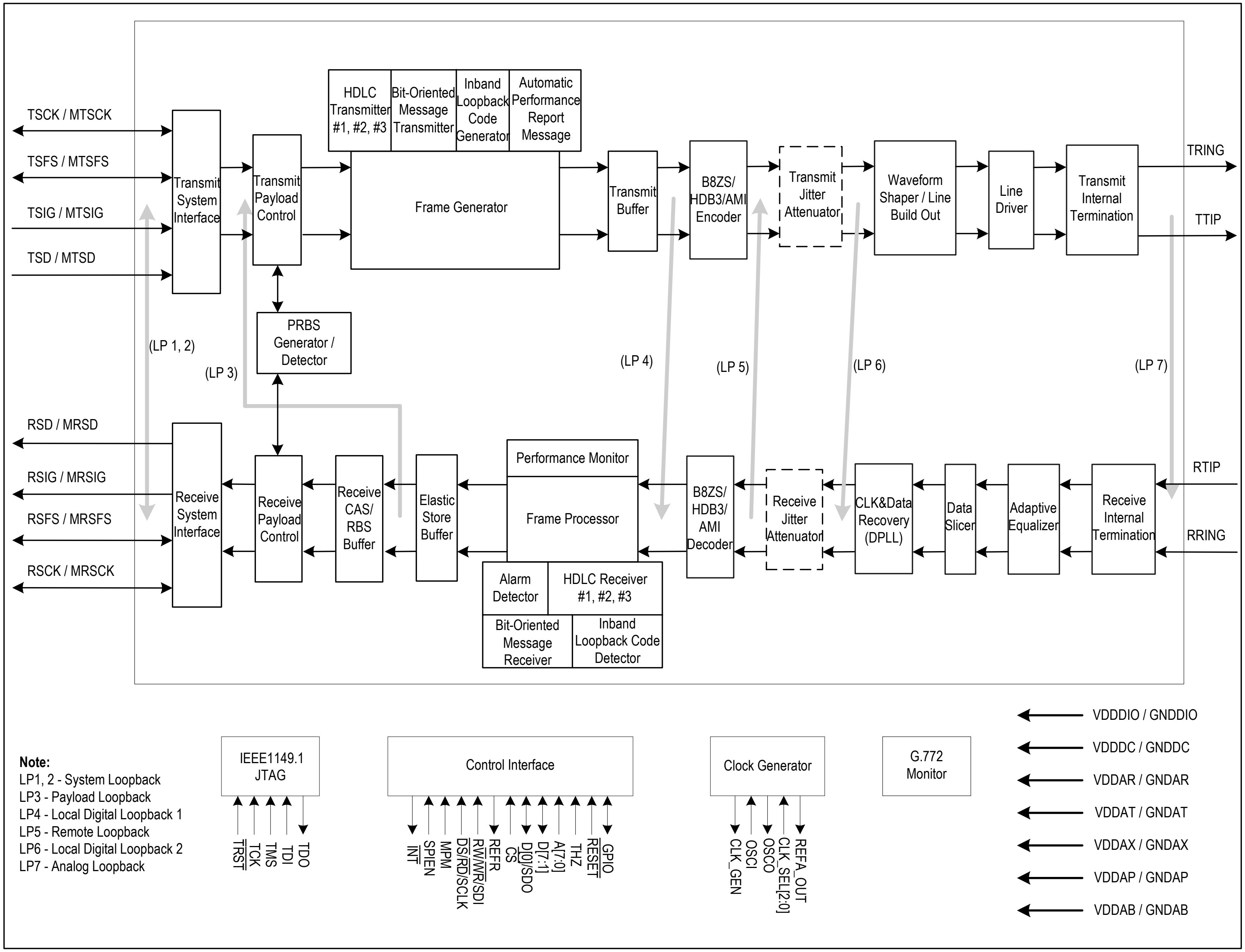
GENERAL

- Flexible reference clock (N x 1.544 MHz or N x 2.048 MHz) (0<N<5)
- JTAG boundary scan
- 3.3 V I/O with 5 V tolerant inputs
- Low power consumption (Typical 190 mW)
- 3.3 V and 1.8 V power supply
- 80-pin TQFP package

APPLICATIONS

- C.O, PABX, ISDN PRI
- Wireless Base Stations
- T1/E1/J1 ATM Gateways, Multiplexer
- T1/E1/J1 Access Networks
- LAN/WAN Router
- Digital Cross Connect
- SONET/SDH Add/Drop Equipment
- Clock recovery at 1.544 MHz / 2.048 MHz for BITS application with SSM support

BLOCK DIAGRAM



1 PIN ASSIGNMENT

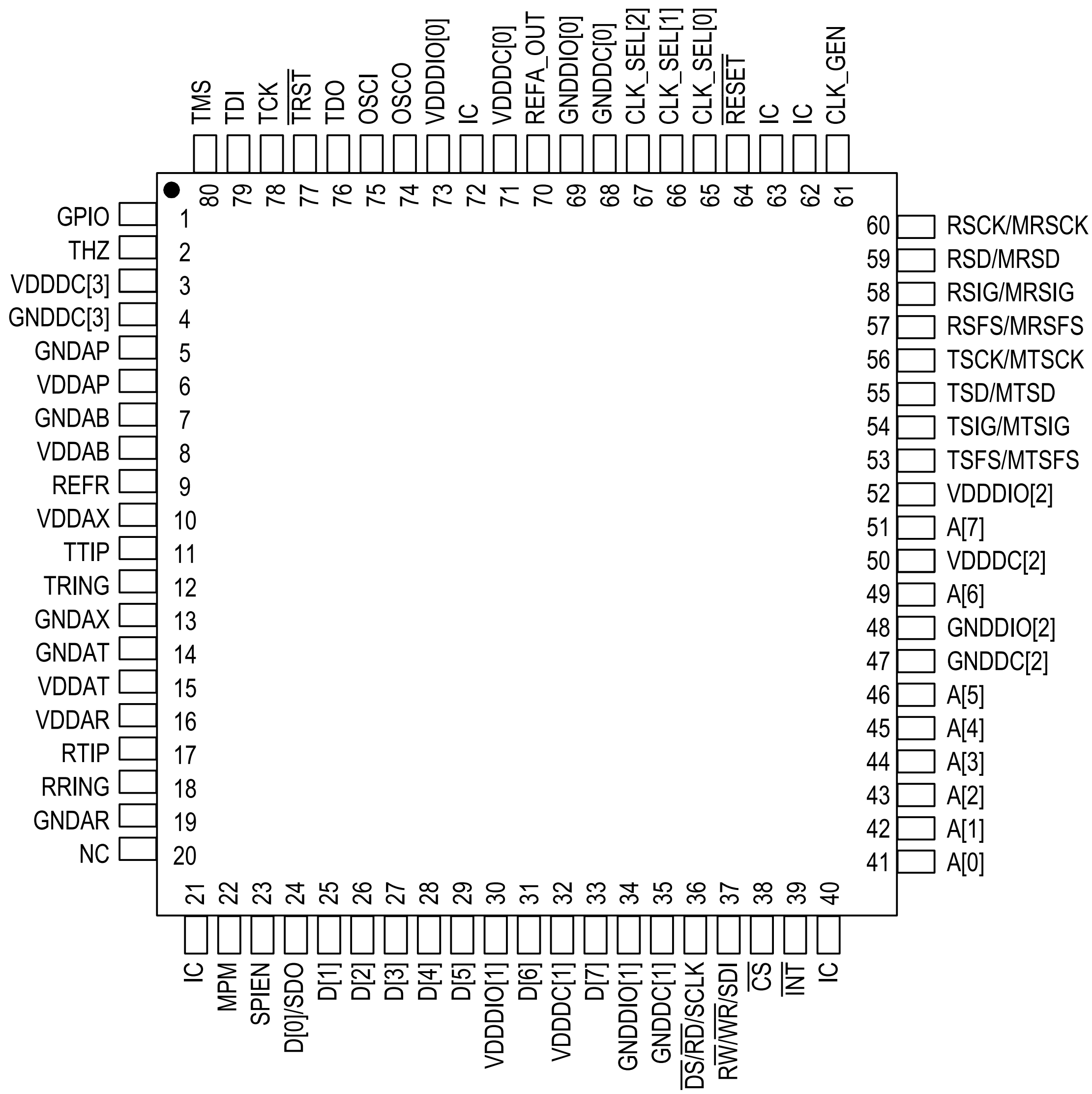


Figure 1. 80-Pin TQFP (Top View)

2 PIN DESCRIPTION

Name	Type	Pin No.	Description
Line and System Interface			
RTIP RRING	Input	17 18	**RTIP / RRING: Receive Bipolar Tip/Ring** These pins are the differential line receiver inputs.
TTIP TRING	Output	11 12	**TTIP / TRING: Transmit Bipolar Tip/Ring** These pins are the differential line driver outputs and can be set to high impedance state. A logic high on the THZ pin sets both two pins to high impedance state. When the T_HZ bit (b4, T1/J1-023H / b4, E1-023H) is set to '1', these two pins will also be set to high impedance state. Besides, TTIP/TRING will also be set to high impedance state by other ways (refer to Chapter 3.25 Line Driver for details).
RSD / MRSD	Output	59	**RSD: Receive Side System Data** The processed data stream is output on this pin. In Receive Non-Multiplexed mode, the RSD pin is updated on the active edge of RSCK. **MRSD: Multiplexed Receive Side System Data** In Receive Multiplexed mode, the MRSD pin is used to output the processed data stream. Using a byte-interleaved multiplexing scheme, the MRSD pin outputs the data from the link. The data on the MRSD pin is updated on the active edge of MRSCK.
RSIG / MRSIG	Output	58	**RSIG: Receive Side System Signaling** The extracted signaling bits are output on this pin. They are located in the lower nibble (b5 ~ b8) and are channel/timeslot-aligned with the data output on the RSD pin. In Receive Non-Multiplexed mode, the RSIG pin is updated on the active edge of RSCK. **MRSIG: Multiplexed Receive Side System Signaling** In Receive Multiplexed mode, the MRSIG pin is used to output the extracted signaling bits. The signaling bits are located in the lower nibble (b5 ~ b8) and are channel/timeslot-aligned with the data output on the MRSD pin. Using the byte-interleaved multiplexing scheme, the MRSIG pin outputs the signaling bits from the link. The signaling bits on the MRSIG pin is updated on the active edge of the MRSCK.
RSFS / MRSFS	Output / Input	57	**RSFS: Receive Side System Frame Pulse** In T1/J1 Receive Clock Master mode, RSFS outputs the pulse to indicate each F-bit, every second F-bit in SF frame, the first F-bit of every SF/ESF/T1 DM/SLC-96 multi-frame or the first F-bit of every second SF multi-frame. In T1/J1 Receive Clock Slave mode, RSFS inputs the pulse at a rate of integer multiple of 125 µs to indicate the start of a frame. In E1 Receive Clock Master mode, RSFS outputs the pulse to indicate the Basic frame, CRC Multi-frame, Signaling Multi-frame, or both the CRC Multi-frame and Signaling Multi-frame, or the TS1 and TS16 overhead. In E1 Receive Clock Slave mode, RSFS inputs the pulse at a rate of integer multiple of 125 µs to indicate the start of a frame. RSFS is updated/sampled on the active edge of RSCK. The active polarity of the RSFS is selected by the FSINV bit (b4, T1/J1-048H / b4, E1-048H). **MRSFS: Multiplexed Receive Side System Frame Pulse** In Receive Multiplexed mode, MRSFS inputs the pulse at a rate of integer multiple of 125 µs to indicate the start of a frame on the multiplexed data bus. MRSFS is sampled on the active edge of MRSCK. The active polarity of MRSFS is selected by the FSINV bit (b4, T1/J1-048H / b4, E1-048H). RSFS/MRSCK is a Schmitt-triggered input/output with pull-up resistor.

Name	Type	Pin No.	Description
RSCK / MRSCK	Output / Input	60	**RSCK: Receive Side System Clock** In Receive Clock Master mode, the RSCK pin outputs a (gapped) 1.544 MHz (for T1/J1 mode) / 2.048 MHz (for E1 mode) clock used to update the signal on the RSD, RSIG and RSFS pins. In Receive Clock Slave mode, the RSCK pin inputs a 1.544 MHz (for T1/J1 mode only), 2.048 MHz or 4.096 MHz clock used to update the signals on the RSD and RSIG pins and sample the signals on the RSFS pin. **MRSCK: Multiplexed Receive Side System Clock** In Receive Multiplexed mode, MRSCK inputs a 8.192 MHz or 16.384 MHz clock used to update the signals on the MRSD and MRSIG pins and sample the signal on the MRSFS pin. RSCK/MRSCK is a Schmitt-triggered input/output with pull-up resistor.
TSD / MTSD	Input	55	**TSD: Transmit Side System Data** The data stream from the system side is input on this pin. In Transmit Non-Multiplexed mode, the TSD pin is sampled on the active edge of TSCK. **MTSD: Multiplexed Transmit Side System Data** In Transmit Multiplexed mode, the MTSD pin is used to input the data stream. Using a byte-interleaved multiplexing scheme, the MTSD pin inputs the data for the link. The data on the MTSD pin is sampled on the active edge of MTSCK. TSD/MTSD is a Schmitt-triggered input.
TSIG / MTSIG	Input	54	**TSIG: Transmit Side System Signaling** The signaling bits are input on this pin. They are located in the lower nibble (b5 ~ b8) and are channel/timeslot-aligned with the data input on the TSD pin. In Transmit Non-Multiplexed mode, TSIG is sampled on the active edge of TSCK. **MTSIG: Multiplexed Transmit Side System Signaling** In Transmit Multiplexed mode, the MTSIG pin is used to input the signaling bits. The signaling bits are located in the lower nibble (b5 ~ b8) and are channel/timeslot-aligned with the data input on the MTSD pin. Using the byte-interleaved multiplexing scheme, the MTSIG pin inputs the signaling bits for the link. The signaling bits on the MTSIG pin is sampled on the active edge of MTSCK. TSIG/MTSIG is a Schmitt-triggered input.
TSFS / MTSFS	Output / Input	53	**TSFS: Transmit Side System Frame Pulse** In T1/J1 Transmit Clock Master mode, TSFS outputs the pulse to indicate each F-bit or the first F-bit of every SF/ESF/T1 DM/SLC-96 multi-frame. In T1/J1 Transmit Clock Slave mode, TSFS inputs the pulse to indicate each F-bit or the first F-bit of every SF/ESF/T1 DM/SLC-96 multi-frame. In E1 Transmit Clock Master mode, TSFS outputs the pulse to indicate the Basic frame, CRC Multi-frame and/or Signaling Multi-frame. In E1 Transmit Clock Slave mode, TSFS inputs the pulse to indicate the Basic frame, CRC Multi-frame and/or Signaling Multi-frame. TSFS is updated/sampled on the active edge of TSCK. The active polarity of TSFS is selected by the FSINV bit (b1, T1/J1-042H / b1, E1-042H). **MTSFS: Multiplexed Transmit Side System Frame Pulse** In T1/J1 Transmit Multiplexed mode, MTSFS inputs the pulse to indicate each F-bit or the first F-bit of every SF/ESF/T1 DM/SLC-96 multi-frame of the link on the multiplexed data bus. In E1 Transmit Multiplexed mode, MTSFS inputs the pulse to indicate each Basic frame, CRC Multi-frame and/or Signaling Multi-frame of the link on the multiplexed data bus. MTSFS is sampled on the active edge of MTSCK. The active polarity of MTSFS is selected by the FSINV bit (b1, T1/J1-042H / b1, E1-042H). TSFS/MTSFS is a Schmitt-triggered input/output with pull-up resistor.

Name	Type	Pin No.	Description
TSCK / MTSCK	Output / Input	56	**TSCK: Transmit Side System Clock** In Transmit Clock Master mode, TSCK outputs a (gapped) 1.544 MHz (for T1/J1 mode) / 2.048 MHz (for E1 mode) clock used to sample the signal on the TSD and TSIG pins and update the signal on the TSFS pin. In Transmit Clock Slave mode, TSCK inputs a 1.544 MHz (for T1/J1 mode only), 2.048 MHz or 4.096 MHz clock used to sample the signal on the TSD, TSIG and TSFS pins. **MTSCK: Multiplexed Transmit Side System Clock** In Transmit Multiplexed mode, MTSCK inputs a 8.192 MHz or 16.384 MHz clock used to sample the signal on the MTSD, MTSIG and MTSFS pins. TSCK/MTSCK is a Schmitt-triggered input/output with pull-up resistor.
Clock Generator			
OSCI	Input	75	**OSCI: Crystal Oscillator Input** This pin is connected to an external clock source. The clock frequency of OSCI is defined by CLK_SEL[2:0]. The clock accuracy should be ±32 ppm and duty cycle should be from 40% to 60%. Hardware or software reset can only be applied when the clock on this pin is available.
OSCO	Output	74	**OSCO: Crystal Oscillator Output** This pin outputs the inverted, buffered clock input from OSCI.
CLK_SEL[0] CLK_SEL[1] CLK_SEL[2]	Input	65 66 67	**CLK_SEL[2:0]: Clock Selection** These three pins select the input clock signal: When the CLK_SEL[2] pin is low, the input clock signal is N X 1.544 MHz; When the CLK_SEL[2] pin is high, the input clock signal is N X 2.048 MHz. When the CLK_SEL[1:0] pins are '00', the N is 1; When the CLK_SEL[1:0] pins are '01', the N is 2; When the CLK_SEL[1:0] pins are '10', the N is 3; When the CLK_SEL[1:0] pins are '11', the N is 4. CLK_SEL[2:0] are Schmitt-trigger inputs.
CLK_GEN	Output	61	**CLK_GEN: Clock Generator** This pin outputs the 1.544/2.048 MHz clock signal generated by the Clock Generator.
REFA_OUT	Output	70	**REFA_OUT: Reference Clock Output A** The frequency is 2.048 MHz(E1) or 1.544 MHz(T1/J1). When no LOS is detected, this pin outputs a recovered clock from the Clock and Data Recovery function block. When LOS is detected, this pin outputs MCLK or high level, as selected by the REFH_LOS bit (b0, T1/J1-03EH/ b0, E1-03EH). Note: MCLK is a clock derived from OSCI using an internal PLL, the frequency is 2.048 MHz(E1) or 1.544 MHz(T1/J1).
Control Interface			
$\overline{\text{RESET}}$	Input	64	**$\overline{\text{RESET}}$: Reset (Active Low)** A low pulse for more than 100 ns on this pin resets the device. All the registers are accessible 2 ms after the reset. Reset can only be applied when the clock on the OSCI pin is available. The $\overline{\text{RESET}}$ pin is a Schmitt-trigger input with a weak pull-up resistor.
GPIO	Output / Input	1	**General Purpose I/O** This pin can be defined as input pin or output pin by the DIR0 bit (b0, T1/J1-006H / b0, E1-006H). When the pin is input, its polarity is indicated by the LEVEL0 bit (b2, T1/J1-006H / b2, E1-006H). When the pin is output, its polarity is controlled by the LEVEL0 bit (b2, T1/J1-006H / b2, E1-006H). GPIO is a Schmitt-trigger input/output with a pull-up resistor
THZ	Input	2	**THZ: Transmit High-Z** A high level on this pin puts the TTIP/TRING pins into high impedance state. THZ is a Schmitt-trigger input.

Name	Type	Pin No.	Description
$\overline{\text{INT}}$	Output	39	**$\overline{\text{INT}}$: Interrupt (Active Low)** This is the open drain, active low interrupt output. This pin will stay low until all the active unmasked interrupt indication bits are cleared.
REFR	Output	9	**REFR:** This pin should be connected to ground via an external 10K resistor.
$\overline{\text{CS}}$	Input	38	**$\overline{\text{CS}}$: Chip Select (Active Low)** This pin must be asserted low to enable the microprocessor interface. The signal must be asserted high at least once after power up to clear the internal test modes. A transition from high to low must occur on this pin for each Read/Write operation and can not return to high until the operation is completed. $\overline{\text{CS}}$ is a Schmitt-trigger input.
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7]	Input	41 42 43 44 45 46 49 51	**A[7:0]: Address Bus** In parallel mode, the signals on these pins select the register for the microprocessor to access. In SPI mode, these pins should be connected to the ground. A[7:0] are Schmitt-trigger inputs with pull-down resistor.
D[0] / SDO D[1] D[2] D[3] D[4] D[5] D[6] D[7]	Output / Input	24 25 26 27 28 29 31 33	**D[7:0]: Bi-directional Data Bus** In parallel mode, the signals on these pins are the data for Read / Write operation. In SPI mode, the D[7:1] pins should be connected to the ground through a 10 K resistor. D[7:0] are Schmitt-trigger inputs/outputs. **SDO: Serial Data Output** In SPI mode, the data is serially output on this pin.
MPM	Input	22	**MPM: Micro Controller Mode** In parallel mode, set this pin low for Motorola mode or high for Intel mode. In SPI mode, set this pin to a fixed level (high or low). This pin is useless in SPI mode. MPM is a Schmitt-trigger input.
R$\overline{\text{W}}$ / $\overline{\text{WR}}$ / SDI	Input	37	**R$\overline{\text{W}}$: Read / Write Select** In parallel Motorola mode, this pin is active high for read operation and active low for write operation. **$\overline{\text{WR}}$: Write Strobe (Active Low)** In parallel Intel mode, this pin is active low for write operation. **SDI: Serial Data Input** In SPI mode, the address/control and/or data are serially input on this pin. R$\overline{\text{W}}$ / $\overline{\text{WR}}$ / SDI is a Schmitt-trigger input.
$\overline{\text{DS}}$ / $\overline{\text{RD}}$ / SCLK	Input	36	**$\overline{\text{DS}}$: Data Strobe (Active Low)** In parallel Motorola mode, this pin is active low. **$\overline{\text{RD}}$: Read Strobe (Active Low)** In parallel Intel mode, this pin is active low for read operation. **SCLK: Serial Clock** In SPI mode, this pin inputs the timing for the SDO and SDI pins. The signal on the SDO pin is updated on the falling edge of SCLK, while the signal on the SDI pin is sampled on the rising edge of SCLK. $\overline{\text{DS}}$ / $\overline{\text{RD}}$ / SCLK is a Schmitt-trigger input.

Name	Type	Pin No.	Description
SPIEN	Input	23	**SPIEN: Serial Microprocessor Interface Enable** When this pin is low, the microprocessor interface is in parallel mode. When this pin is high, the microprocessor interface is in SPI mode. SPIEN is a Schmitt-trigger input.
			JTAG (per IEEE 1149.1)
$\overline{\text{TRST}}$	Input	77	**$\overline{\text{TRST}}$: Test Reset (Active Low)** A low signal on this pin resets the JTAG test port. This pin is a Schmitt-triggered input with an internal pull-up resistor. It must be connected to the $\overline{\text{RESET}}$ pin or ground when JTAG is not used.
TMS	Input	80	**TMS: Test Mode Select** The signal on this pin controls the JTAG test performance and is sampled on the rising edge of TCK. This pin is a Schmitt-triggered input with an internal pull-up resistor.
TCK	Input	78	**TCK: Test Clock** The clock for the JTAG test is input on this pin. TDI and TMS are sampled on the rising edge of TCK and TDO is clocked out of the device on the falling edge of TCK. This pin is a Schmitt-triggered input with an internal pull-up resistor.
TDI	Input	79	**TDI: Test Input** The test data is sampled at this pin on the rising edge of TCK. This pin has an internal pull-up resistor. This pin is a Schmitt-triggered input with an internal pull-up resistor.
TDO	High-Z	76	**TDO: Test Output** The test data are output on this pin. It is updated on the falling edge of TCK. This pin is High-Z except during the process of data scanning.
			Power & Ground
VDDDIO[0] VDDDIO[1] VDDDIO[2]	Power	73 30 52	**VDDDIO[2:0]: 3.3 V I/O Power Supply**
GNDDIO[0] GNDDIO[1] GNDDIO[2]	Ground	69 34 48	**GNDDIO[2:0]: Digital Pad Ground**
VDDDC[0] VDDDC[1] VDDDC[2] VDDDC[3]	Power	71 32 50 3	**VDDDC[3:0]: 1.8 V Digital Core Power Supply**
GNDDC[0] GNDDC[1] GNDDC[2] GNDDC[3]	Ground	68 35 47 4	**GNDDC[3:0]: Digital Core Ground**
VDDAR	Power	16	**VDDAR: 3.3 V Power Supply for Receiver**
GNDAR	Ground	19	**GNDAR: Analog Ground for Receiver**
VDDAT	Power	15	**VDDAT: 3.3 V Power Supply for Transmitter**
GNDAT	Ground	14	**GNDAT: Analog Ground for Transmitter**
VDDAX	Power	10	**VDDAX: 3.3 V Power Supply for Transmit Driver**
GNDAX	Ground	13	**GNDAX: Analog Ground for Transmitter Driver**
VDDAP	Power	6	**VDDAP: 3.3 V Power Analog PLL**
GNDAP	Ground	5	**GNDAP: Analog Ground PLL**
VDDAB	Power	8	**VDDAB: 3.3 V Power Analog Bias**
GNDAB	Ground	7	**GNDAB: Analog Ground Bias**

Name	Type	Pin No.	Description
TEST			
IC	-	21 40 62 63	**IC: Internal Connected** These pins are for IDT use only and should be connected to ground.
IC	Output	72	**IC: Internal Connected** This pin is for IDT use only and should not be connected.
NC	-	20	**NC: Not Connected**

3 FUNCTIONAL DESCRIPTION

The IDT82P2281 is a highly featured single device solution for T1/E1/J1 trunks. The configuration is performed through an SPI or parallel microprocessor interface.

LINE INTERFACE - RECEIVE PATH

In the receive path, the signals from the line side are coupled into the RTIP and RRING pins and pass through an Impedance Terminator. An Adaptive Equalizer is provided to increase the sensitivity for small signals. Clock and data are recovered from the digital pulses output from the slicer. After passing through the Receive Jitter Attenuator (can be enabled or disabled), the recovered data is decoded using B8ZS (for T1/J1) / HDB3 (for E1) or AMI line code rules and clocked into the Frame Processor. Loss of signal, line code violations and excessive zero are detected.

FRAMER - RECEIVE PATH

In T1/J1 Mode, the recovered data and clock can be configured in Super Frame (SF), Extended Super Frame (ESF), T1 Digital Multiplexer (DM) or Switch Line Carrier - 96 (SLC-96) formats. (The T1 DM and SLC-96 formats only exist in T1 mode). The framing can also be bypassed (unframed mode). The Framer detects and indicates the out of SF/ESF/DM/SLC-96 synchronization event, the Yellow, Red and AIS alarms. The Framer also detects the presence of inband loopback codes and bit-oriented messages. Frame Alignment Signal errors, CRC-6 errors, out of SF/ESF/T1 DM/SLC-96 events and Frame Alignment position changes are counted. Up to three HDLC links (in ESF and T1 DM format) or two HDLC links (in SF and SLC-96 format) are provided to extract the HDLC message on the DL bit (in ESF format) / D bit in CH24 (in T1 DM format) or any arbitrary position. In the T1/J1 receive path, signaling debounce, signaling freeze, idle code substitution, digital milliwatt code insertion, idle code insertion, data inversion and pattern generation or detection are supported on a per-channel basis. An Elastic Store Buffer that supports controlled slip and adaptation to backplane timing may be enabled. In the Receive System Interface, various operating modes can be selected to output signals to the system.

In E1 Mode, the recovered data and clock can be configured to frame to Basic Frame, CRC Multi-Frame and Signaling Multi-Frame. The framing can be bypassed (unframed mode). The Framer detects and indicates the following event: out of Basic Frame Sync, out of CRC Multi-Frame, out of Signaling Multi-Frame, Remote Alarm Indication signal and Remote Signaling Multi-Frame Alarm Indication signal. The Framer also monitors Red and AIS alarms. Basic Frame Alignment Signal errors, Far End Block Errors (FEBE) and CRC errors are counted. Up to three HDLC links are provided to extract the HDLC message on TS16, the Sa National bits or any arbitrary timeslot. In the E1 receive path, signaling debounce, signaling freezing, idle code substitution, digital milliwatt code insertion, trunk conditioning, data inversion and pattern generation or detection are also supported on a per-timeslot basis. An Elastic Store Buffer that supports slip buffering and adaptation to backplane timing may be enabled. In the Receive System Interface, various operating modes can be selected to output signals to the system.

SYSTEM INTERFACE

On the system side, if the device is in T1/J1 mode, the data stream of 1.544 Mbit/s can be converted to/from the data stream of 2.048 Mbit/s by software configuration. In addition, the link can be multiplexed to or de-multiplexed from a 8.192 Mbit/s bus. If the device is in E1 mode, the link can be multiplexed to or de-multiplexed from a 8.192 Mbit/s bus.

FRAMER - TRANSMIT PATH

In the transmit path, the Transmit System Interface inputs the signals with various operating modes. In T1/J1 mode, the signals can be processed by a Transmit Payload Control to execute the signaling insertion, idle code substitution, data insertion, data inversion and test pattern generation or detection on a per-channel basis. The transmit path of each transceiver can be configured to generate SF, ESF, T1 DM or SLC-96. The framer can also be disabled (unframed mode). The Framer can transmit Yellow alarm and AIS alarm. Inband loopback codes and bit oriented message can be transmitted. Up to three HDLC links (in ESF and T1 DM format) or two HDLC links (in SF and SLC-96 format) are provided to insert the HDLC message on the DL bit (in ESF format) / D bit in CH24 (in T1 DM format) or any arbitrary position. After passing through a Transmit Buffer, the processed data and clock are input to the Encoder.

In E1 mode, the signals can be processed by a Transmit Payload Control to execute the signaling insertion, idle code substitution, data insertion, data inversion and test pattern generation or detection on a per-timeslot basis. The transmit path of each transceiver can be configured to generate Basic Frame, CRC Multi-Frame and Signaling Multi-Frame. The framer can be disabled (unframed mode). The Framer can transmit Remote Alarm Indication signal, the Remote Signaling Multi-Frame Alarm Indication signal, AIS alarm and FEBE. Three HDLC links are provided to insert the HDLC message on TS16, the Sa National bits or any arbitrary timeslot. The processed data and clock are input to the Encoder.

LINE INTERFACE - TRANSMIT PATH

The data is encoded using AMI or B8ZS (for T1/J1) and HDB3 (for E1) line code rules. The Transmit Jitter Attenuator, if enabled, is provided with a FIFO in the transmit data path. A de-jittered clock is generated by an integrated digital phase-locked loop and is used to read data from the FIFO. The shapes of the pulses are user programmable to ensure that the T1/E1/J1 pulse template is met after the signal passing through different cable lengths and types. Bipolar violation can be inserted for diagnostic purposes if AMI line code rule is enabled. The signal is transmitted on the TTIP and TRING pins through an Impedance Terminator.

TEST AND DIAGNOSES

To facilitate the testing and diagnostic functions, Analog Loopback, Remote Digital Loopback, Remote Loopback, Local Digital Loopback, Payload Loopback and System Loopback are also integrated in the IDT82P2281. A programmable pseudo random bit sequence can be generated in receive/transmit direction and detected in the opposite direction for testing purpose.

The JTAG is also supported by the IDT82P2281.

3.1 T1 / E1 / J1 MODE SELECTION

The IDT82P2281 can be configured as a duplex T1 transceiver, or a duplex E1 transceiver, or a duplex J1 transceiver. When it is in T1 mode, Super Frame (SF), Extended Super Frame (ESF), T1 Digital Multiplexer (T1 DM) and Switch Line Carrier - 96 (SLC-96) framing formats can be selected. When it is in J1 mode, Super Frame (SF) and Extended Super Frame (ESF) formats can be selected. All the selections are made by the TEMODE bit, the T1/J1 bit and the FM[1:0] bits as shown in Table 1.

Table 1: Operating Mode Selection

TEMODE	T1/J1	FM[1:0]	Operating Mode
1	0	0 0	T1 mode SF format
		0 1	T1 mode ESF format
		1 0	T1 mode T1 DM format
		1 1	T1 mode SLC-96 format
	1	0 0	J1 mode SF format
		0 1	J1 mode ESF format
0	X	X	E1 mode

Table 2: Related Bit / Register In Chapter 3.1

Bit	Register	Address (Hex)
TEMODE	T1/J1 Or E1 Mode	020
T1/J1		
FM[1:0]		

3.2 RECEIVER IMPEDANCE MATCHING

The receiver impedance matching can be realized by using internal impedance matching circuit or external impedance matching circuit.

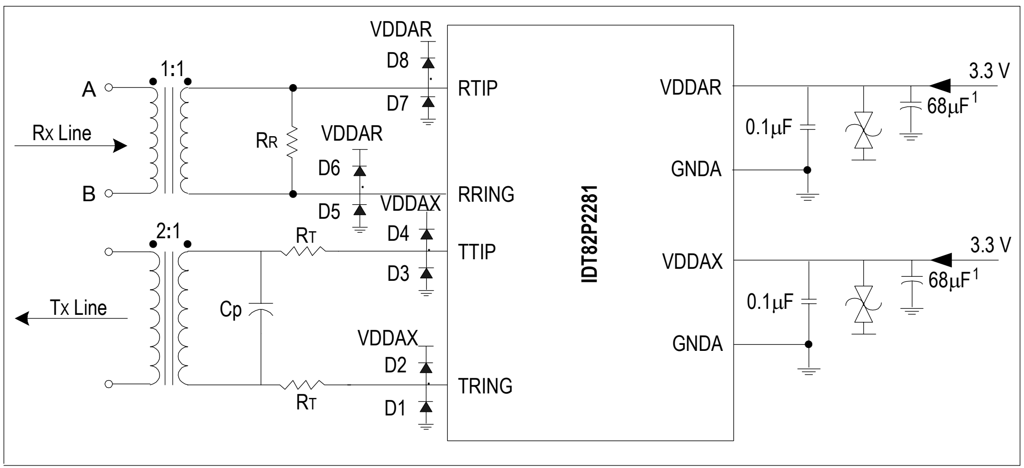
When the R_TERM[2] bit is '0', the internal impedance matching circuit is enabled. 100 Ω, 110 Ω, 75 Ω or 120 Ω internal impedance matching circuit can be selected by the R_TERM[1:0] bits.

When the R_TERM[2] bit is '1', the internal impedance matching circuit is disabled, and different external resistors should be used to realize different impedance matching.

Figure 2 shows the appropriate components to connect with the cable. Table 3 lists the recommended matching resistor values for the receiver.

Table 3: Impedance Matching Value For The Receiver

Cable Configuration	Internal Termination		External Termination	
	R_TERM[2:0]	R_R	R_TERM[2:0]	R_R
75 Ω (E1)	0 0 0	120 Ω	1 X X	75 Ω
120 Ω (E1)	0 0 1			120 Ω
100 Ω (T1)	0 1 0			100 Ω
110 Ω (J1)	0 1 1			110 Ω



Note: 1. Common decoupling capacitor
2. Cp 0-560 (pF)
3. D1 - D8, Motorola - MBR0540T1; International Rectifier - 11DQ04 or 10BQ060

Figure 2. Receive / Transmit Line Circuit

3.2.1 LINE MONITOR

In both T1/J1 and E1 short haul applications, the Protected Non-Intrusive Monitoring per T1.102 can be performed between two devices. The monitored link of one device is in normal operation, and the monitoring link of the other device taps the monitored one through a high impedance bridging circuit. Refer to Figure 3&Figure 4 (Twisted Pair) and Figure 5&Figure 6 (COAX).

After the high resistance bridging circuit, the signal arriving at RTIP/RRING of the monitoring link is dramatically attenuated. To compensate this bridge resistive attenuation, Monitor Gain can be used to boost the signal by 22 dB, as selected by the MG[1:0] bits (b1~0, T1/J1-02AH). For normal operation, the Monitor Gain should be set to 0 dB, i.e., the Monitor Gain of the monitored link should be 0 dB.

The monitoring link can be configured to any of the External or Partially Internal Impedance Matching mode. Here the external r or internal IM is used for voltage division, not for impedance matching. That is, the r (IM) and the R make up of a resistance bridge. The resistive attenuation of this bridge is 20lg(r/(2R+r)) dB for Twisted Pair or 20lg(r/(R+r)) dB for COAX. The value of resistive attenuation should be consistent with the setting of Monitor Gain (22 dB).

In case of LOS, REFH_LOS bit (b0, T1/J1-03EH) determines the outputs on the REFA_OUT pin. When set to 0, the output is MCLK; when set to 1, the output is high level.

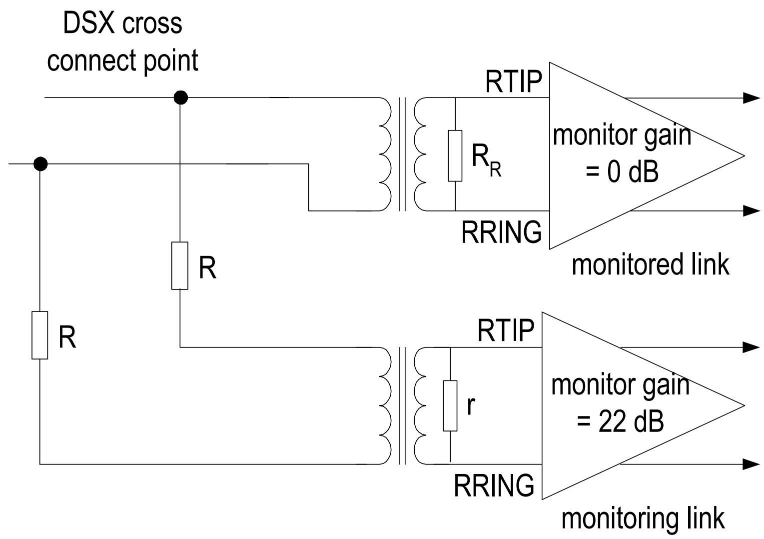


Figure 3. Receive Path Monitoring (Twisted Pair)

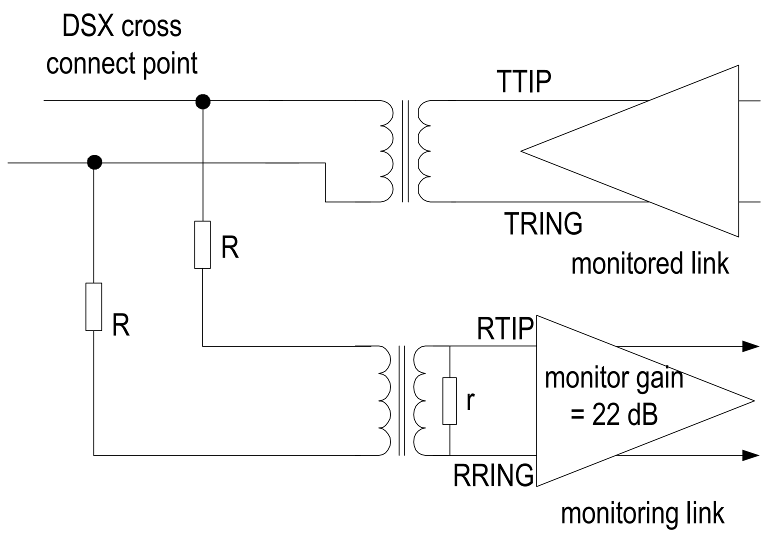


Figure 4. Transmit Path Monitoring (Twisted Pair)