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Octal T1/E1/J1 Long Haul / Short Haul Transceiver

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Version 8
JANUARY 10, 2011

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FEATURES

LINE INTERFACE

- Each link can be configured as T1, E1 or J1
- Supports T1/E1/J1 long haul/short haul line interface
- HPS for 1+1 protection without external relays
- Receive sensitivity exceeds -36 dB @ 772 Hz and -43 dB @ 1024 Hz
- Selectable internal line termination impedance: 100 Ω (for T1), 75 Ω / 120 Ω (for E1) and 110 Ω (for J1)
- Supports AMI/B8ZS (for T1/J1) and AMI/HDB3 (for E1) line encoding/decoding
- Provides T1/E1/J1 short haul pulse templates, long haul LBO (per ANSI T1.403 and FCC68: 0 dB, -7.5 dB, -15 dB, -22 dB) and user-programmable arbitrary pulse template
- Supports G.772 non-intrusive monitoring
- Supports T1.102 line monitor
- Transmit line short-circuit detection and protection
- Separate Transmit and Receive Jitter Attenuators (2 per link)
- Indicates the interval between the write pointer and the read pointer of the FIFO in JA
- Loss of signal indication with programmable thresholds according to ITUT-T G.775, ETS 300 233 (E1) and ANSI T1.403 (T1/J1)
- Supports Analog Loopback, Digital Loopback and Remote Loopback
- Each receiver and transmitter can be individually powered down

FRAMER

- Each link can be configured as T1, E1 or J1
- Frame alignment/generation for T1 (per ITU-T G.704, TA-TSY-000278, TR-TSY-000008), E1 (per ITU-T G.704), J1 (per JT G.704) and un-framed mode
- Supports T1/J1 Super Frame and Extended Super Frame, T1 Digital Multiplexer and Switch Line Carrier - 96, E1 CRC Multi-frame and Signaling Multi-frame
- Signaling extraction/insertion for CAS and RBS signaling
- Provides programmable system interface supporting Mitel™ ST-bus, AT&T™ CHI and MVIP bus, 8.192 Mb/s multiplexed bus and 1.544 Mb/s or 2.048 Mb/s non-multiplexed bus
- Three HDLC controllers per link with separate 128-byte transmit and receive FIFOs per controller
- Programmable bit insertion and bit inversion on per channel/timeslot basis
- Provides Bit Oriented Message (BOM) generation and detection
- Provides Automatic Performance Report Message (APRM) generation
- Detects and generates alarms (AIS, RAI)
- Provides performance monitor to count Bipolar Violation error, Excess Zero error, CRC error, framing bit error, far end CRC error, out of frame and change of framing alignment position
- Supports System Loopback, Payload Loopback, Digital Loopback and Inband Loopback
- Detects and generates selectable PRBS and QRSS

CONTROL INTERFACE

- Supports Serial Peripheral Interface (SPI) microprocessor and parallel Intel/Motorola non-multiplexed microprocessor interface
- Global hardware and software reset
- Two general purpose I/O pins
- Per link power down

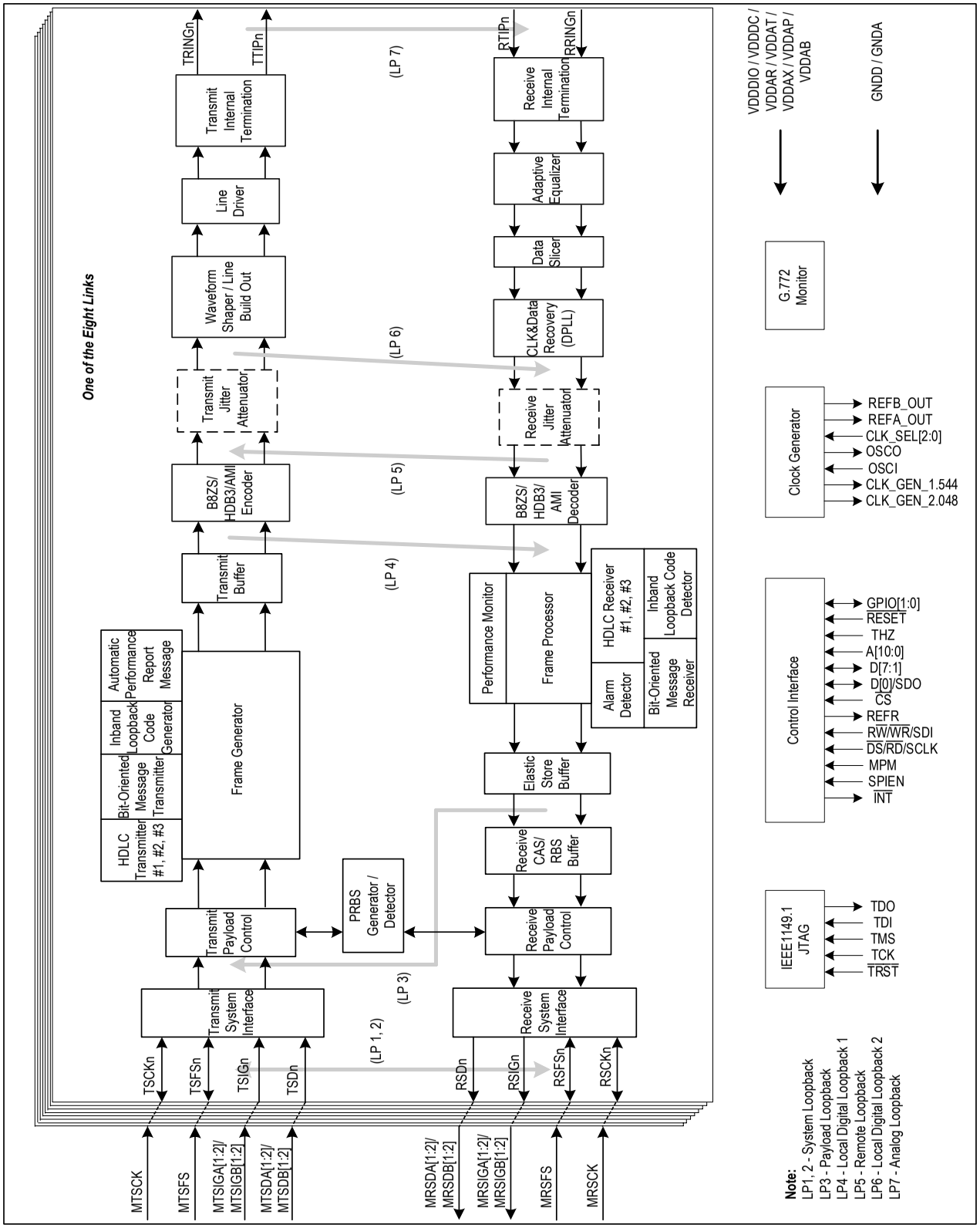
GENERAL

- Flexible reference clock (N x 1.544 MHz or N x 2.048 MHz) (0<N<5)
- JTAG boundary scan
- 3.3 V I/O with 5 V tolerant inputs
- Low power consumption (Typical 900 mW)
- 3.3 V and 1.8 V power supply
- 256-pin CABGA package

APPLICATIONS

- C.O, PABX, ISDN PRI
- Wireless Base Stations
- T1/E1/J1 ATM Gateways, Multiplexer
- T1/E1/J1 Access Networks
- LAN/WAN Router
- Digital Cross Connect
- SONET/SDH Add/Drop Equipment

BLOCK DIAGRAM



1 PIN ASSIGNMENT

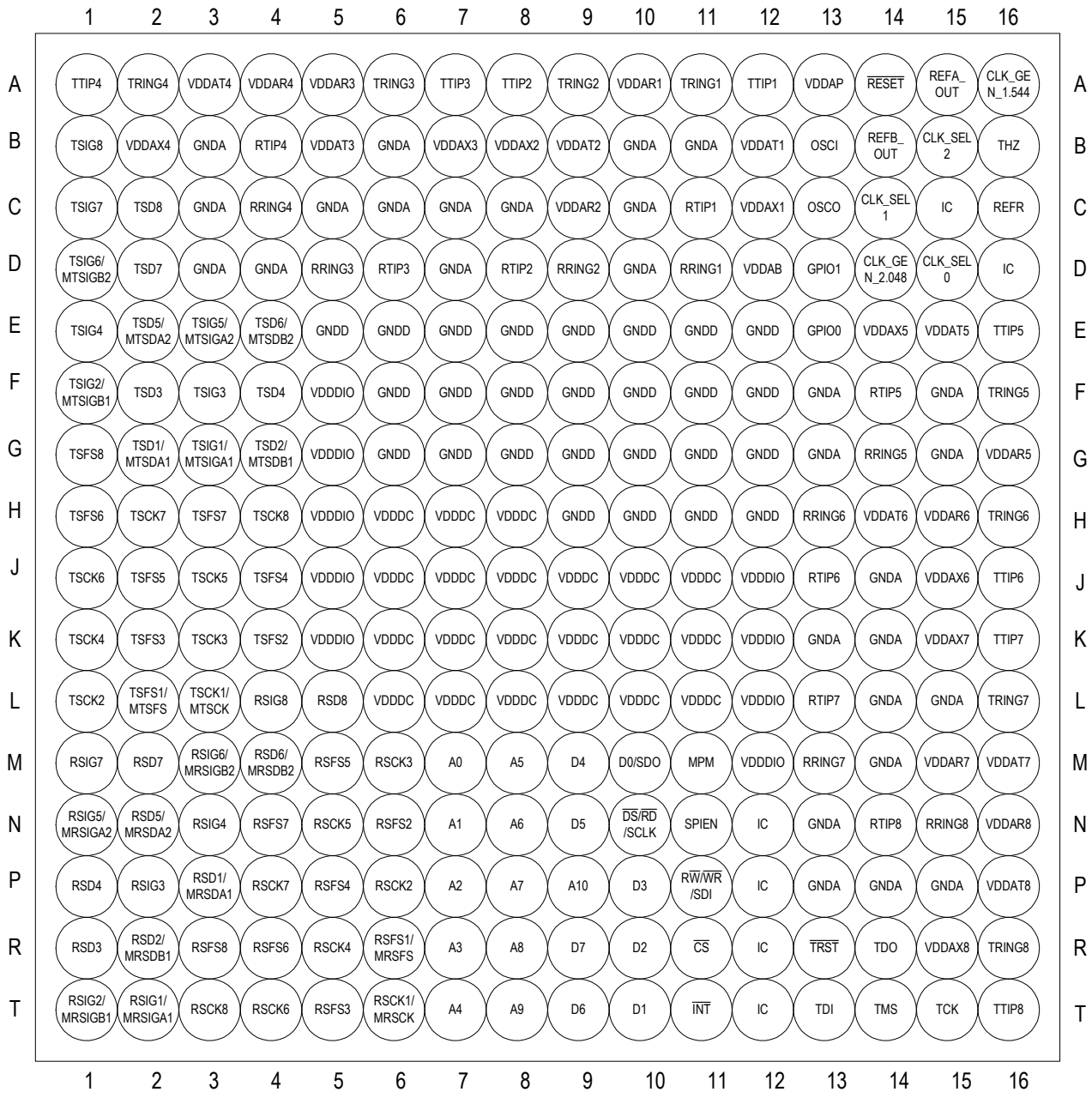


Figure 1. 256-Pin CABGA and PBGA (Top View)

2 PIN DESCRIPTION

Name	Type	Pin No.	Description
			Line and System Interface
RTIP[1] RTIP[2] RTIP[3] RTIP[4] RTIP[5] RTIP[6] RTIP[7] RTIP[8] RRING[1] RRING[2] RRING[3] RRING[4] RRING[5] RRING[6] RRING[7] RRING[8]	Input	C11 D8 D6 B4 F14 J13 L13 N14 D11 D9 D5 C4 G14 H13 M13 N15	**RTIP[1:8] / RRING[1:8]: Receive Bipolar Tip/Ring for Link 1 ~ 8** These pins are the differential line receiver inputs.
TTIP[1] TTIP[2] TTIP[3] TTIP[4] TTIP[5] TTIP[6] TTIP[7] TTIP[8] TRING[1] TRING[2] TRING[3] TRING[4] TRING[5] TRING[6] TRING[7] TRING[8]	Output	A12 A8 A7 A1 E16 J16 K16 T16 A11 A9 A6 A2 F16 H16 L16 R16	**TTIP[1:8] / TRING[1:8]: Transmit Bipolar Tip/Ring for Link 1 ~ 8** These pins are the differential line driver outputs and can be set to high impedance state globally or individually. A logic high on the THZ pin sets all these pins to high impedance state. When the T_HZ bit (b4, T1/J1-023H,... / b4, E1-023H,...) * is set to '1', the TTIPn/TRINGn pins in the corresponding link are set to high impedance state. Besides, TTIPn/TRINGn will also be set to high impedance state by other ways (refer to Chapter 3.25 Line Driver for details).
RSD[1] / MRSDA[1] RSD[2] / MRSDB[1] RSD[3] RSD[4] RSD[5] / MRSDA[2] RSD[6] / MRSDB[2] RSD[7] RSD[8]	High-Z Output	P3 R2 R1 P1 N2 M4 M2 L5	**RSD[1:8]: Receive Side System Data for Link 1 ~ 8** The processed data stream is output on these pins. In Receive Clock Master mode, the RSDn pins are updated on the active edge of the corresponding RSCKn. In Receive Clock Slave mode, determined by the RSLVCK bit (b4, T1/J1-010H / b4, E1-010H), the RSDn pins are updated on the active edge of the corresponding RSCKn or all eight RSDn pins are updated on the active edge of RSCK[1]. **MRSDA[1:2] / MRSDB[1:2]: Multiplexed Receive Side System Data A / B for Link 1 ~ 8** In Receive Multiplexed mode, the MRSDA[1:2] pins or the MRSDB[1:2] pins are used to output the processed data stream. Using a byte-interleaved multiplexing scheme, the MRSDA[1]/MRSDB[1] pins output the data from Link 1 to Link 4, while the MRSDA[2]/MRSDB[2] pins output the data from Link 5 to Link 8. The data on the MRSDA[1:2]/MRSDB[1:2] pins are updated on the active edge of the MRSCK. The data on MRSDA[1:2] is the same as the data on MRSDB[1:2]. MRSDB[1:2] are for back-up purpose.

Note:

***** The contents in the brackets indicate the position of the preceding bit and the address of the register. After the address, if the punctuation ',...' is followed, this bit is in a per-link control register and the listed address belongs to Link 1. Users can find the omitted addresses in Chapter 5. If there is no punctuation following the address, this bit is in a global control register.

Name	Type	Pin No.	Description
RSIG[1] / MRSIGA[1] RSIG[2] / MRSIGB[1] RSIG[3] RSIG[4] RSIG[5] / MRSIGA[2] RSIG[6] / MRSIGB[2] RSIG[7] RSIG[8]	High-Z Output	T2 T1 P2 N3 N1 M3 M1 L4	**RSIG[1:8]: Receive Side System Signaling for Link 1 ~ 8** The extracted signaling bits are output on these pins. They are located in the lower nibble (b5 ~ b8) and are channel/timeslot-aligned with the data output on the corresponding RSDn pin. In Receive Clock Master mode, the RSIGn pins are updated on the active edge of the corresponding RSCKn. In Receive Clock Slave mode, determined by the RSLVCK bit (b4, T1/J1-010H / b4, E1-010H), the RSIGn pins are updated on the active edge of the corresponding RSCKn or all eight RSIGn are updated on the active edge of RSCK[1]. **MRSIGA[1:2] / MRSIGB[1:2]: Multiplexed Receive Side System Signaling A / B for Link 1 ~ 8** In Receive Multiplexed mode, the MRSIGA[1:2] pins or the MRSIGB[1:2] pins are used to output the extracted signaling bits. The signaling bits are located in the lower nibble (b5 ~ b8) and are channel/timeslot-aligned with the data output on the corresponding MRSDA[1:2]/MRSDB[1:2] pins. Using the byte-interleaved multiplexing scheme, the MRSIGA[1]/MRSIGB[1] pins output the signaling bits from Link 1 to Link 4, while the MRSDA[2]/MRSDB[2] pins output the signaling bits from Link 5 to Link 8. The signaling bits on the MRSIGA[1:2]/MRSIGB[1:2] pins are updated on the active edge of the MRSCK. The signaling bits on MRSIGA[1:2] is the same as the signaling bits on MRSIGB[1:2]. MRSIGB[1:2] are for back-up purpose.
RSFS[1] / MRSFS RSFS[2] RSFS[3] RSFS[4] RSFS[5] RSFS[6] RSFS[7] RSFS[8]	Output / Input	R6 N6 T5 P5 M5 R4 N4 R3	**RSFS[1:8]: Receive Side System Frame Pulse for Link 1 ~ 8** In T1/J1 Receive Clock Master mode, RSFSn outputs the pulse to indicate each F-bit, every second F-bit in SF frame, the first F-bit of every SF/ESF/T1 DM/SLC-96 multi-frame or the first F-bit of every second SF multi-frame. In T1/J1 Receive Clock Slave mode, RSFSn inputs the pulse at a rate of integer multiple of 125 µs to indicate the start of a frame. In E1 Receive Clock Master mode, RSFSn outputs the pulse to indicate the Basic frame, CRC Multi-frame, Signaling Multi-frame, or both the CRC Multi-frame and Signaling Multi-frame, or the TS1 and TS16 overhead. In E1 Receive Clock Slave mode, RSFSn inputs the pulse at a rate of integer multiple of 125 µs to indicate the start of a frame. RSFSn is updated/sampled on the active edge of the corresponding RSCKn. The active polarity of RSFSn is determined by the FSINV bit (b4, T1/J1-048H,... / b4, E1-048H,...). **MRSFS: Multiplexed Receive Side System Frame Pulse for Link 1 ~ 8** In Receive Multiplexed mode, MRSFS inputs the pulse at a rate of integer multiple of 125 µs to indicate the start of a frame on the multiplexed data bus. MRSFS is sampled on the active edge of MRSCK. The active polarity of MRSFS is determined by the FSINV bit (b4, T1/J1-048H,... / b4, E1-048H,...). RSFS[1:8]/MRSCK are Schmitt-triggered inputs/outputs with pull-up resistors.
RSCK[1] / MRSCK RSCK[2] RSCK[3] RSCK[4] RSCK[5] RSCK[6] RSCK[7] RSCK[8]	Output / Input	T6 P6 M6 R5 N5 T4 P4 T3	**RSCK[1:8]: Receive Side System Clock for Link 1 ~ 8** In Receive Clock Master mode, the RSCKn pins output a (gapped) 1.544 MHz (for T1/J1 mode) / 2.048 MHz (for E1 mode) clock used to update the signal on the corresponding RSDn, RSIGn and RSFSn pins. In Receive Clock Slave mode, the RSCKn pins input a 1.544 MHz (for T1/J1 mode only), 2.048 MHz or 4.096 MHz clock used to update the signals on the corresponding RSDn and RSIGn pins and sample the signals on the corresponding RSFSn pins. Selected by the RSLVCK bit (b4, T1/J1-010H / b4, E1-010H), the RSCK[1] pin can be used for all eight links. **MRSCK: Multiplexed Receive Side System Clock for Link 1 ~ 8** In Receive Multiplexed mode, MRSCK inputs a 8.192 MHz or 16.384 MHz clock used to update the signals on the corresponding MRSDA/MRSDB and MRSIGA/MRSIGB pins and sample the signal on the corresponding MRSFS pin. RSCK[1:8]/MRSCK are Schmitt-triggered inputs/outputs with pull-up resistors.

Name	Type	Pin No.	Description
TSD[1] / MTSDA[1] TSD[2] / MTSDB[1] TSD[3] TSD[4] TSD[5] / MTSDA[2] TSD[6] / MTSDB[2] TSD[7] TSD[8]	Input	G2 G4 F2 F4 E2 E4 D2 C2	**TSD[1:8]: Transmit Side System Data for Link 1 ~ 8** The data stream from the system side is input on these pins. In Transmit Clock Master mode, the TSDn pins are sampled on the active edge of the corresponding TSCKn. In Transmit Clock Slave mode, selected by the TSLVCK bit (b1, T1/J1-010H / b1, E1-010H), the TSDn pins are sampled on the active edge of the corresponding TSCKn or all eight TSDn pins are sampled on the active edge of TSCK[1]. **MTSDA[1:2] / MTSDB[1:2]: Multiplexed Transmit Side System Data A / B for Link 1 ~ 8** In Transmit Multiplexed mode, selected by the MTSDA bit (b2, T1/J1-010H / b2, E1-010H), the MTSDA[1:2] pins or the MTSDB[1:2] pins are used to input the data stream. Using a byte-interleaved multiplexing scheme, the MTSDA[1]/MTSDB[1] pins input the data for Link 1 to Link 4, while the MTSDA[2]/MTSDB[2] pins input the data for Link 5 to Link 8. The data on the MTSDA[1:2]/MTSDB[1:2] pins are sampled on the active edge of MTSCK. TSD[1:8]/MTSDA[1:2]/MTSDB[1:2] are Schmitt-triggered inputs.
TSIG[1] / MTSIGA[1] TSIG[2] / MTSIGB[1] TSIG[3] TSIG[4] TSIG[5] / MTSIGA[2] TSIG[6] / MTSIGB[2] TSIG[7] TSIG[8]	Input	G3 F1 F3 E1 E3 D1 C1 B1	**TSIG[1:8]: Transmit Side System Signaling for Link 1 ~ 8** The signaling bits are input on these pins. They are located in the lower nibble (b5 ~ b8) and are channel/timeslot-aligned with the data input on the corresponding TSDn pin. In Transmit Clock Master mode, TSIGn is sampled on the active edge of the corresponding TSCKn. In Transmit Clock Slave mode, selected by the TSLVCK bit (b1, T1/J1-010H / b1, E1-010H), TSIGn is sampled on the active edge of the corresponding TSCKn or all eight TSIGn are updated on the active edge of TSCK[1]. **MTSIGA[1:2] / MTSIGB[1:2]: Multiplexed Transmit Side System Signaling A / B for Link 1 ~ 8** In Transmit Multiplexed mode, selected by the MTSDA bit (b2, T1/J1-010H / b2, E1-010H), the MTSIGA[1:2] pins or the MTSIGB[1:2] pins are used to input the signaling bits. The signaling bits are located in the lower nibble (b5 ~ b8) and are channel/timeslot-aligned with the data input on the corresponding MTSDA[1:2]/MTSDB[1:2] pins. Using the byte-interleaved multiplexing scheme, the MTSIGA[1]/MTSIGB[1] pins input the signaling bits for Link 1 to Link 4, while the MTSIGA[2]/MTSIGB[2] pins input the signaling bits for Link 5 to Link 8. The signaling bits on the MTSIGA[1:2]/MTSIGB[1:2] pins are sampled on the active edge of MTSCK. TSIG[1:8]/MTSIGA[1:2]/MTSIGB[1:2] are Schmitt-triggered inputs.
TSFS[1] / MTSFS TSFS[2] TSFS[3] TSFS[4] TSFS[5] TSFS[6] TSFS[7] TSFS[8]	Output / Input	L2 K4 K2 J4 J2 H1 H3 G1	**TSFS[1:8]: Transmit Side System Frame Pulse for Link 1 ~ 8** In T1/J1 Transmit Clock Master mode, TSFSn outputs the pulse to indicate each F-bit or the first F-bit of every SF/ESF/T1 DM/SLC-96 multi-frame. In T1/J1 Transmit Clock Slave mode, TSFSn inputs the pulse to indicate each F-bit or the first F-bit of every SF/ESF/T1 DM/SLC-96 multi-frame. In E1 Transmit Clock Master mode, TSFSn outputs the pulse to indicate the Basic frame, CRC Multi-frame and/or Signaling Multi-frame. In E1 Transmit Clock Slave mode, TSFSn inputs the pulse to indicate the Basic frame, CRC Multi-frame and/or Signaling Multi-frame. TSFSn is updated/sampled on the active edge of the corresponding TSCKn. The active polarity of TSFSn is selected by the FSINV bit (b1, T1/J1-042H,... / b1, E1-042H,...). **MTSFS: Multiplexed Transmit Side System Frame Pulse for Link 1 ~ 8** In T1/J1 Transmit Multiplexed mode, MTSFS inputs the pulse to indicate each F-bit or the first F-bit of every SF/ESF/T1 DM/SLC-96 multi-frame of one link on the multiplexed data bus. In E1 Transmit Multiplexed mode, MTSFS inputs the pulse to indicate each Basic frame, CRC Multi-frame and/or Signaling Multi-frame of one link on the multiplexed data bus. MTSFS is sampled on the active edge of MTSCK. The active polarity of MTSFS is selected by the FSINV bit (b1, T1/J1-042H,... / b1, E1-042H,...). TSFS[1:8]/MTSFS are Schmitt-triggered inputs/outputs with pull-up resistors.

Name	Type	Pin No.	Description
TSCK[1] / MTSCK TSCK[2] TSCK[3] TSCK[4] TSCK[5] TSCK[6] TSCK[7] TSCK[8]	Output / Input	L3 L1 K3 K1 J3 J1 H2 H4	**TSCK[1:8]: Transmit Side System Clock for Link 1 ~ 8** In Transmit Clock Master mode, TSCKn outputs a (gapped) 1.544 MHz (for T1/J1 mode) / 2.048 MHz (for E1 mode) clock used to sample the signal on the corresponding TSDn and TSIGn pins and update the signal on the corresponding TSFSn pin. In Transmit Clock Slave mode, TSCKn inputs a 1.544 MHz (for T1/J1 mode only), 2.048 MHz or 4.096 MHz clock used to sample the signal on the corresponding TSDn, TSIGn and TSFSn pins. Selected by the TSLVCK bit (b1, T1/J1-010H / b1, E1-010H), the TSCK[1] can be used for all eight links. **MTSCK: Multiplexed Transmit Side System Clock for Link 1 ~ 8** In Transmit Multiplexed mode, MTSCK inputs a 8.192 MHz or 16.384 MHz clock used to sample the signal on the corresponding MTSDA/MTSDB, MTSIGA/MTSIGB and MTSFS pins. TSCK[1:8]/MTSCK are Schmitt-triggered inputs/outputs with pull-up resistors.
Clock Generator			
OSCI	Input	B13	**OSCI: Crystal Oscillator Input** This pin is connected to an external clock source. In T1 mode E1 Rate of Transmit System interface, this clock must keep the source same with system transmit clock (TSCKn/MTSCK). The clock frequency of OSCI is defined by CLK_SEL[2:0]. The clock accuracy should be ±32 ppm and duty cycle should be from 40% to 60%.
OSCO	Output	C13	**OSCO: Crystal Oscillator Output** This pin outputs the inverted, buffered clock input from OSCI.
CLK_SEL[0] CLK_SEL[1] CLK_SEL[2]	Input	D15 C14 B15	**CLK_SEL[2:0]: Clock Selection** These three pins select the input clock signal: When the CLK_SEL[2] pin is low, the input clock signal is N X 1.544 MHz; When the CLK_SEL[2] pin is high, the input clock signal is N X 2.048 MHz. When the CLK_SEL[1:0] pins are '00', the N is 1; When the CLK_SEL[1:0] pins are '01', the N is 2; When the CLK_SEL[1:0] pins are '10', the N is 3; When the CLK_SEL[1:0] pins are '11', the N is 4. CLK_SEL[2:0] are Schmitt-trigger inputs.
CLK_GEN_1.544	Output	A16	**CLK_GEN_1.544: Clock Generator 1.544 MHz Output** This pin outputs the 1.544 MHz clock signal generated by the Clock Generator.
CLK_GEN_2.048	Output	D14	**CLK_GEN_2.048: Clock Generator 2.048 MHz Output** This pin outputs the 2.048 MHz clock signal generated by the Clock Generator.
REFA_OUT	Output	A15	**REFA_OUT: Reference Clock Output A** The frequency is 2.048 MHz (E1) or 1.544 MHz (T1/J1) When no LOS is detected, this pin outputs a recovered clock from the Clock and Data Recovery function block of one of the eight links. The link is selected by the RO1[2:0] bits (b2~0, T1/J1-007H / b2~0, E1-007H). When LOS is detected, this pin outputs MCLK or high level, as selected by the REFH_LOS bit (b0, T1/J1-03EH,... / b0, E1-03EH,...). * Note: MCLK is a clock derived from OSCI using an internal PLL, and the frequency is 2.048 MHz (E1) or 1.544 MHz (T1/J1).
REFB_OUT	Output	B14	**REFB_OUT: Reference Clock Output B** The frequency is 2.048 MHz (E1) or 1.544 MHz (T1/J1) When no LOS is detected, this pin outputs a recovered clock from the Clock and Data Recovery function block of one of the eight links. The link is selected by the RO2[2:0] bits (b5~3, T1/J1-007H / b5~3, E1-007H). When LOS is detected, this pin outputs MCLK or high level, as selected by the REFH_LOS bit (b0, T1/J1-03EH,... / b0, E1-03EH,...). *

Note:
* This feature is available in ZB revision only.

Name	Type	Pin No.	Description
			Control Interface
$\overline{\text{RESET}}$	Input	A14	**$\overline{\text{RESET}}$: Reset (Active Low)** A low pulse for more than 100 ns on this pin resets the device. All the registers are accessible 2 ms after the reset. The $\overline{\text{RESET}}$ pin is a Schmitt-trigger input with a weak pull-up resistor. The OSCI clock must exist when the device is reset.
GPIO[0] GPIO[1]	Output / Input	E13 D13	**General Purpose I/O [1:0]** These two pins can be defined as input pins or output pins by the DIR[1:0] bits (b1~0, T1/J1-006H / b1~0, E1-006H) respectively. When the pins are input, their polarities are indicated by the LEVEL[1:0] bits (b3~2, T1/J1-006H / b3~2, E1-006H) respectively. When the pins are output, their polarities are controlled by the LEVEL[1:0] bits (b3~2, T1/J1-006H / b3~2, E1-006H) respectively. GPIO[1:0] are Schmitt-trigger input/output with a pull-up resistor.
THZ	Input	B16	**THZ: Transmit High-Z** A high level on this pin puts all the TTIPn/TRINGn pins into high impedance state. THZ is a Schmitt-trigger input.
$\overline{\text{INT}}$	Output	T11	**$\overline{\text{INT}}$: Interrupt (Active Low)** This is the open drain, active low interrupt output. This pin will stay low until all the active unmasked interrupt indication bits are cleared.
REFR	Output	C16	**REFR:** This pin should be connected to ground via an external 10K resistor.
$\overline{\text{CS}}$	Input	R11	**$\overline{\text{CS}}$: Chip Select (Active Low)** This pin must be asserted low to enable the microprocessor interface. The signal must be asserted high at least once after power up to clear the internal test modes. A transition from high to low must occur on this pin for each Read/Write operation and can not return to high until the operation is completed. $\overline{\text{CS}}$ is a Schmitt-trigger input.
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7] A[8] A[9] A[10]	Input	M7 N7 P7 R7 T7 M8 N8 P8 R8 T8 P9	**A[10:0]: Address Bus** In parallel mode, the signals on these pins select the register for the microprocessor to access. In SPI mode, these pins should be connected to ground. A[10:0] are Schmitt-trigger inputs.
D[0] / SDO D[1] D[2] D[3] D[4] D[5] D[6] D[7]	Output / Input	M10 T10 R10 P10 M9 N9 T9 R9	**D[7:0]: Bi-directional Data Bus** In parallel mode, the signals on these pins are the data for Read / Write operation. In SPI mode, the D[7:1] pins should be connected to the ground through a 10 K resistor. D[7:0] are Schmitt-trigger inputs/outputs. **SDO: Serial Data Output** In SPI mode, the data is serially output on this pin.
MPM	Input	M11	**MPM: Micro Controller Mode** In parallel mode, set this pin low for Motorola mode or high for Intel mode. In SPI mode, set this pin to a fixed level (high or low). This pin is useless in SPI mode. MPM is a Schmitt-trigger input.

Name	Type	Pin No.	Description
R/$\overline{W}$ / $\overline{WR}$ / SDI	Input	P11	**R/$\overline{W}$: Read / Write Select** In parallel Motorola mode, this pin is active high for read operation and active low for write operation. **$\overline{WR}$: Write Strobe (Active Low)** In parallel Intel mode, this pin is active low for write operation. **SDI: Serial Data Input** In SPI mode, the address/control and/or data are serially input on this pin. R/$\overline{W}$ / $\overline{WR}$ / SDI is a Schmitt-trigger input.
$\overline{DS}$ / $\overline{RD}$ / SCLK	Input	N10	**$\overline{DS}$: Data Strobe (Active Low)** In parallel Motorola mode, this pin is active low. **$\overline{RD}$: Read Strobe (Active Low)** In parallel Intel mode, this pin is active low for read operation. **SCLK: Serial Clock** In SPI mode, this pin inputs the timing for the SDO and SDI pins. The signal on the SDO pin is updated on the falling edge of SCLK, while the signal on the SDI pin is sampled on the rising edge of SCLK. $\overline{DS}$ / $\overline{RD}$ / SCLK is a Schmitt-trigger input.
SPIEN	Input	N11	**SPIEN: Serial Microprocessor Interface Enable** When this pin is low, the microprocessor interface is in parallel mode. When this pin is high, the microprocessor interface is in SPI mode. SPIEN is a Schmitt-trigger input.
JTAG (per IEEE 1149.1)			
$\overline{TRST}$	Input	R13	**$\overline{TRST}$: Test Reset (Active Low)** A low signal on this pin resets the JTAG test port. This pin is a Schmitt-triggered input with an internal pull-up resistor. It must be connected to the $\overline{RESET}$ pin or ground when JTAG is not used.
TMS	Input	T14	**TMS: Test Mode Select** The signal on this pin controls the JTAG test performance and is sampled on the rising edge of TCK. This pin is a Schmitt-triggered input with an internal pull-up resistor.
TCK	Input	T15	**TCK: Test Clock** The clock for the JTAG test is input on this pin. TDI and TMS are sampled on the rising edge of TCK and TDO is clocked out of the device on the falling edge of TCK. This pin is a Schmitt-triggered input with an internal pull-up resistor.
TDI	Input	T13	**TDI: Test Input** The test data is sampled at this pin on the rising edge of TCK. This pin is a Schmitt-triggered input with an internal pull-up resistor.
TDO	High-Z	R14	**TDO: Test Output** The test data are output on this pin. It is updated on the falling edge of TCK. This pin is High-Z except during the process of data scanning.
Power & Ground			
VDDDIO	Power	F5, G5, H5, J5, J12, K5, K12, L12, M12	**VDDDIO: 3.3 V I/O Power Supply**

Name	Type	Pin No.	Description
VDDDC	Power	H6, H7, H8, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, L6, L7, L8, L9, L10, L11	**VDDDC: 1.8 V Digital Core Power Supply**
VDDAR[1] VDDAR[2] VDDAR[3] VDDAR[4] VDDAR[5] VDDAR[6] VDDAR[7] VDDAR[8]	Power	A10 C9 A5 A4 G16 H15 M15 N16	**VDDAR[8:1]: 3.3 V Power Supply for Receiver**
VDDAT[1] VDDAT[2] VDDAT[3] VDDAT[4] VDDAT[5] VDDAT[6] VDDAT[7] VDDAT[8]	Power	B12 B9 B5 A3 E15 H14 M16 P16	**VDDAT[8:1]: 3.3 V Power Supply for Transmitter**
VDDAX[1] VDDAX[2] VDDAX[3] VDDAX[4] VDDAX[5] VDDAX[6] VDDAX[7] VDDAX[8]	Power	C12 B8 B7 B2 E14 J15 K15 R15	**VDDAX[8:1]: 3.3 V Power Supply for Transmit Driver**
VDDAP	Power	A13	**VDDAP: 3.3 V Power Analog PLL**
VDDAB	Power	D12	**VDDAB: 3.3 V Power Analog Bias**
GNDD	Ground	E5, E6, E7, E8, E9, E10, E11, E12, F6, F7, F8, F9, F10, F11, F12, G6, G7, G8, G9, G10, G11, G12, H9, H10, H11, H12	**GNDD: Digital Ground**

Name	Type	Pin No.	Description
GNDA	Ground	B3, B6, B10, B11, C3, C5, C6, C7, C8, C10, D3, D4, D7, D10, F13, F15, G13, G15, J14, K13, K14, L14, L15, M14, N13, P13, P14, P15	**GNDA: Analog Ground**
TEST			
IC	-	N12 P12 R12 T12 C15 D16	**IC: Internally Connected** These pins are for IDT use only and should be connected to ground.

3 FUNCTIONAL DESCRIPTION

The IDT82P2288 is a highly featured single device solution for T1/E1/J1 trunks. Each link of the IDT82P2288 can be independently configured. The configuration is performed through an SPI or parallel microprocessor interface.

LINE INTERFACE - RECEIVE PATH

In the receive path, the signals from the line side are coupled into the RTIPn and RRINGn pins and pass through an Impedance Terminator. An Adaptive Equalizer is provided to increase the sensitivity for small signals. Clock and data are recovered from the digital pulses output from the slicer. After passing through the Receive Jitter Attenuator (can be enabled or disabled), the recovered data is decoded using B8ZS (for T1/J1) / HDB3 (for E1) or AMI line code rules and clocked into the Frame Processor. Loss of signal, line code violations and excessive zero are detected.

FRAMER - RECEIVE PATH

In T1/J1 Mode, the recovered data and clock of each link can be configured in Super Frame (SF), Extended Super Frame (ESF), T1 Digital Multiplexer (DM) or Switch Line Carrier - 96 (SLC-96) formats. (The T1 DM and SLC-96 formats only exist in T1 mode). The framing can also be bypassed (unframed mode). The Framer detects and indicates the out of SF/ESF/DM/SLC-96 synchronization event, the Yellow, Red and AIS alarms. The Framer also detects the presence of inband loopback codes and bit-oriented messages. Frame Alignment Signal errors, CRC-6 errors, out of SF/ESF/T1 DM/SLC-96 events and Frame Alignment position changes are counted. Up to three HDLC links (in ESF and T1 DM format) or two HDLC links (in SF and SLC-96 format) are provided to extract the HDLC message on the DL bit (in ESF format) / D bit in CH24 (in T1 DM format) or any arbitrary position. In the T1/J1 receive path, signaling debounce, signaling freeze, idle code substitution, digital milliwatt code insertion, idle code insertion, data inversion and pattern generation or detection are supported on a per-channel basis. An Elastic Store Buffer that supports controlled slip and adaptation to backplane timing may be enabled. In the Receive System Interface, various operating modes can be selected to output signals to the system.

In E1 Mode, the recovered data and clock of each link can be configured to frame to Basic Frame, CRC Multi-Frame and Signaling Multi-Frame. The framing can be bypassed (unframed mode). The Framer detects and indicates the following event: out of Basic Frame Sync, out of CRC Multi-Frame, out of Signaling Multi-Frame, Remote Alarm Indication signal and Remote Signaling Multi-Frame Alarm Indication signal. The Framer also monitors Red and AIS alarms. Basic Frame Alignment Signal errors, Far End Block Errors (FEBE) and CRC errors are counted. Up to three HDLC links are provided to extract the HDLC message on TS16, the Sa National bits or any arbitrary timeslot. In the E1 receive path, signaling debounce, signaling freezing, idle code substitution, digital milliwatt code insertion, trunk conditioning, data inversion and pattern generation or detection are also supported on a per-timeslot basis. An Elastic Store Buffer that supports slip buffering and adaptation to backplane timing may be enabled. In the Receive System Interface, various operating modes can be selected to output signals to the system.

SYSTEM INTERFACE

On the system side, if the device is in T1/J1 mode, the data stream of 1.544 Mbit/s can be converted to/from the data stream of 2.048 Mbit/s by software configuration. In addition, the eight links can be grouped into two sets with four links in each set. Each set can be multiplexed to or de-multiplexed from one of the two 8.192 Mbit/s buses. If the device is in E1 mode, four of the eight links can be multiplexed to or de-multiplexed from one of the two 8.192 Mbit/s buses.

FRAMER - TRANSMIT PATH

In the transmit path, the Transmit System Interface inputs the signals with various operating modes. In T1/J1 mode, the signals can be processed by a Transmit Payload Control to execute the signaling insertion, idle code substitution, data insertion, data inversion and test pattern generation or detection on a per-channel basis. The transmit path of each transceiver can be configured to generate SF, ESF, T1 DM or SLC-96. The framer can also be disabled (unframed mode). The Framer can transmit Yellow alarm and AIS alarm. Inband loopback codes and bit oriented message can be transmitted. Up to three HDLC links (in ESF and T1 DM format) or two HDLC links (in SF and SLC-96 format) are provided to insert the HDLC message on the DL bit (in ESF format) / D bit in CH24 (in T1 DM format) or any arbitrary position. After passing through a Transmit Buffer, the processed data and clock are input to the Encoder.

In E1 mode, the signals can be processed by a Transmit Payload Control to execute the signaling insertion, idle code substitution, data insertion, data inversion and test pattern generation or detection on a per-timeslot basis. The transmit path of each transceiver can be configured to generate Basic Frame, CRC Multi-Frame and Signaling Multi-Frame. The framer can be disabled (unframed mode). The Framer can transmit Remote Alarm Indication signal, the Remote Signaling Multi-Frame Alarm Indication signal, AIS alarm and FEBE. Three HDLC links are provided to insert the HDLC message on TS16, the Sa National bits or any arbitrary timeslot. The processed data and clock are input to the Encoder.

LINE INTERFACE - TRANSMIT PATH

The data is encoded using AMI or B8ZS (for T1/J1) and HDB3 (for E1) line code rules. The Transmit Jitter Attenuator, if enabled, is provided with a FIFO in the transmit data path. A de-jittered clock is generated by an integrated digital phase-locked loop and is used to read data from the FIFO. The shapes of the pulses are user programmable to ensure that the T1/E1/J1 pulse template is met after the signal passing through different cable lengths and types. Bipolar violation can be inserted for diagnostic purposes if AMI line code rule is enabled. The signal is transmitted on the TTIPn and TRINGn pins through an Impedance Terminator.

TEST AND DIAGNOSES

To facilitate the testing and diagnostic functions, Analog Loopback, Remote Digital Loopback, Remote Loopback, Local Digital Loopback, Payload Loopback and System Loopback are also integrated in the IDT82P2288. A programmable pseudo random bit sequence can be generated in receive/transmit direction and detected in the opposite direction for testing purpose.

The G.772 Non-intrusive monitoring and JTAG are also supported by the IDT82P2288.

3.1 T1 / E1 / J1 MODE SELECTION

Each link in the IDT82P2288 can be configured as a duplex T1 transceiver, or a duplex E1 transceiver, or a duplex J1 transceiver. When it is in T1 mode, Super Frame (SF), Extended Super Frame (ESF), T1 Digital Multiplexer (T1 DM) and Switch Line Carrier - 96 (SLC-96) framing formats can be selected. When it is in J1 mode, Super Frame (SF) and Extended Super Frame (ESF) formats can be selected. All the selections are made by the TEMODE bit, the T1/J1 bit and the FM[1:0] bits as shown in Table 1.

Table 1: Operating Mode Selection

TEMODE	T1/J1	FM[1:0]	Operating Mode
1	0	0 0	T1 mode SF format
		0 1	T1 mode ESF format
		1 0	T1 mode T1 DM format
		1 1	T1 mode SLC-96 format
	1	0 0	J1 mode SF format
		0 1	J1 mode ESF format
0	X	X	E1 mode

Table 2: Related Bit / Register In Chapter 3.1

Bit	Register	Address (Hex)
TEMODE	T1/J1 Or E1 Mode	020, 120, 220, 320, 420, 520, 620, 720
T1/J1		
FM[1:0]		

3.2 RECEIVER IMPEDANCE MATCHING

The receiver impedance matching can be realized by using internal impedance matching circuit or external impedance matching circuit.

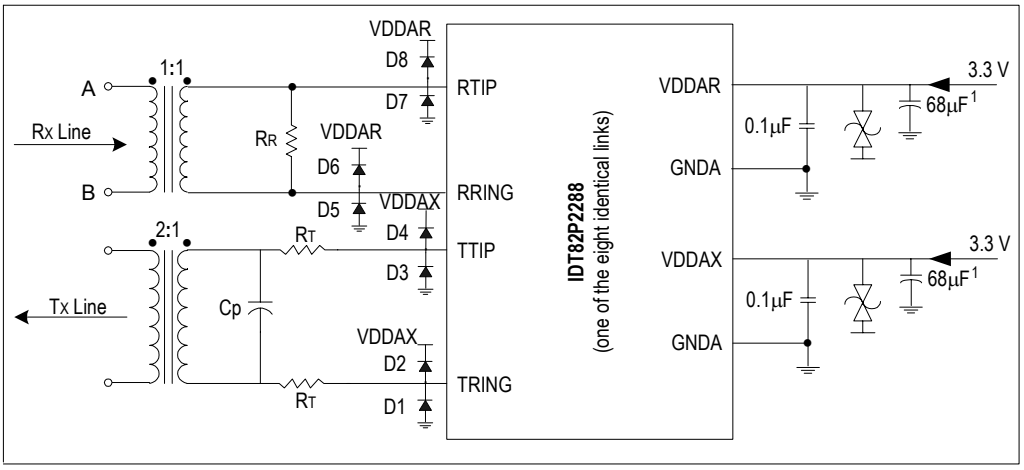
When the R_TERM[2] bit is '0', the internal impedance matching circuit is enabled. 100 Ω, 110 Ω, 75 Ω or 120 Ω internal impedance matching circuit can be selected by the R_TERM[1:0] bits.

Table 3: Impedance Matching Value For The Receiver

Cable Configuration	Internal Termination		External Termination	
	R_TERM[2:0]	R_R	R_TERM[2:0]	R_R
75 Ω (E1)	0 0 0	120 Ω	1 X X	75 Ω
120 Ω (E1)	0 0 1			120 Ω
100 Ω (T1)	0 1 0			100 Ω
110 Ω (J1)	0 1 1			110 Ω

When the R_TERM[2] bit is '1', the internal impedance matching circuit is disabled, and different external resistors should be used to realize different impedance matching.

Figure 2 shows the appropriate components to connect with the cable for one link. Table 3 lists the recommended matching resistor values for the receiver.



Note: 1. Common decoupling capacitor
2. Cp 0-560 (pF)
3. D1 - D8, Motorola - MBR0540T1; International Rectifier - 11DQ04 or 10BQ060

Figure 2. Receive / Transmit Line Circuit

3.2.1 LINE MONITOR

In both T1/J1 and E1 short haul applications, the Protected Non-Intrusive Monitoring per T1.102 can be performed between two devices. The monitored link of one device is in normal operation, and the monitoring link of the other device taps the monitored one through a high impedance bridging circuit. Refer to Figure 3&Figure 4 (Twisted Pair) and Figure 5&Figure 6 (COAX).

After the high resistance bridging circuit, the signal arriving at RTIPn/RRINGn of the monitoring link is dramatically attenuated. To compensate this bridge resistive attenuation, Monitor Gain can be used to boost the signal by 22 dB, as selected by the MG[1:0] bits (b1~0, T1/J1-02AH,...). For normal operation, the Monitor Gain should be set to 0 dB, i.e., the Monitor Gain of the monitored link should be 0 dB.

The monitoring link can be configured to any of the External or Partially Internal Impedance Matching mode. Here the external r or internal IM is used for voltage division, not for impedance matching. That is, the r (IM) and the R make up of a resistance bridge. The resistive attenuation of this bridge is 20lg(r/(2R+r)) dB for Twisted Pair or 20lg(r/(R+r)) dB for COAX. The value of resistive attenuation should be consistent with the setting of Monitor Gain (22 dB).

In case of LOS, REFH_LOS bit (b0, T1/J1-03EH) determines the outputs on the REFA_OUT and REFB_OUT pins. When set to 0, the output is MCLK; when set to 1, the output is high level.

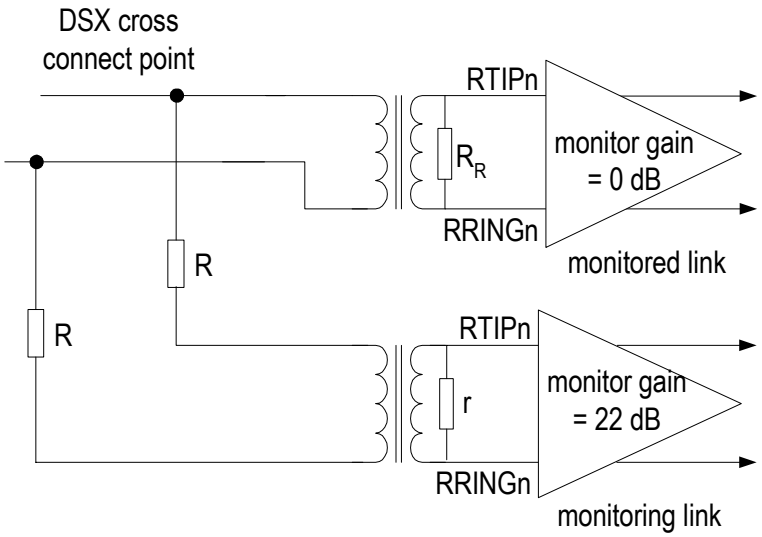


Figure 3. Receive Path Monitoring (Twisted Pair)

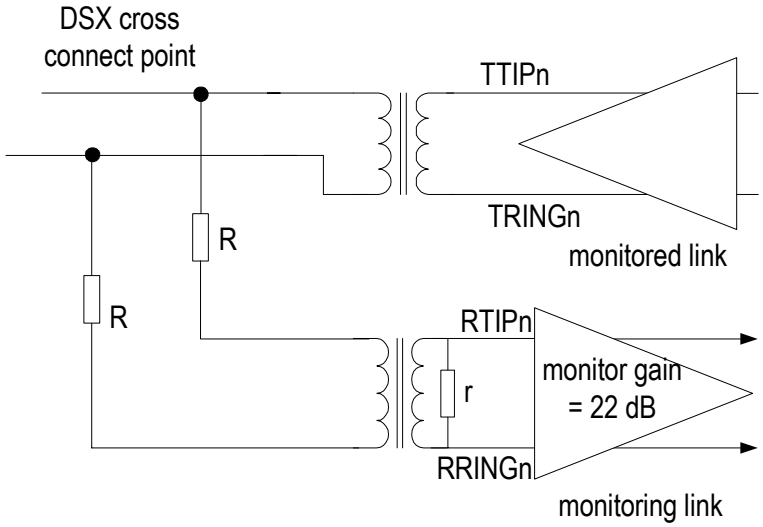


Figure 4. Transmit Path Monitoring (Twisted Pair)