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28(+1) Channel High-Density T1/E1/J1 Line Interface Unit

IDT82P2828

Version 3
February 6, 2009

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FEATURES

- **Integrates 28+1 channels T1/E1/J1 short haul line interface units for 100 Ω T1, 120 Ω E1, 110 Ω J1 twisted pair cable and 75 Ω E1 coaxial cable applications**
- **Per-channel configurable Line Interface options**
  - Supports various line interface options
    - *Differential and Single Ended line interfaces*
    - *true Single Ended termination on primary and secondary side of transformer for E1 75 Ω coaxial cable applications*
    - *transformer-less for Differential interfaces*
  - Fully integrated and software selectable receive and transmit termination
    - *Option 1: Fully Internal Impedance Matching with integrated receive termination resistor*
    - *Option 2: Partially Internal Impedance Matching with common external resistor for improved device power dissipation*
    - *Option 3: External impedance Matching termination*
  - Supports global configuration and per-channel configuration to T1, E1 or J1 mode
- **Per-channel programmable features**
  - Provides T1/E1/J1 short haul waveform templates and user-programmable arbitrary waveform templates
  - Provides two JAs (Jitter Attenuator) for each channel of receiver and transmitter
  - Supports AMI/B8ZS (for T1/J1) and AMI/HDB3 (for E1) encoding and decoding
- **Per-channel System Interface options**
  - Supports Single Rail, Dual Rail with clock or without clock and sliced system interface
  - Integrated Clock Recovery for the transmit interface to recover transmit clock from system transmit data
- **Per-channel system and diagnostic functions**
  - Provides transmit driver over-current detection and protection with optional automatic high impedance of transmit interface
  - Detects and generates PRBS (Pseudo Random Bit Sequence), ARB (Arbitrary Pattern) and IB (Inband Loopback) in either receive or transmit direction
  - Provides defect and alarm detection in both receive and transmit directions.
    - *Defects include BPV (Bipolar Violation) /CV (Code Violation) and EXZ (Excessive Zeroes)*
    - *Alarms include LLOS (Line LOS), SLOS (System LOS), TLOS (Transmit LOS) and AIS (Alarm Indication Signal)*
  - Programmable LLOS detection /clear levels. Compliant with ITU and ANSI specifications
  - Various pattern, defect and alarm reporting options
    - *Serial hardware LLOS reporting (LLOS, LLOS0) for all 29 channels*
    - *Configurable per-channel hardware reporting with RMF/TMF (Receive /Transmit Multiplex Function)*
    - *Register access to individual registers or 16-bit error counters*
  - Supports Analog Loopback, Digital Loopback and Remote Loopback
  - Supports T1.102 line monitor
- **Channel 0 monitoring options**
  - Channel 0 can be configured as monitoring channel or regular channel to increase capacity
  - Supports all internal G.772 Monitoring for Non-Intrusive Monitoring of any of the 28 channels of receiver or transmitter
  - Jitter Measurement per ITU O.171
- **Hitless Protection Switching (HPS) without external Relays**
  - Supports 1+1 and 1:1 hitless protection switching
  - Asynchronous hardware control (OE, RIM) for fast global high impedance of receiver and transmitter (hot switching between working and backup board)
  - High impedance transmitter and receiver while powered down
  - Per-channel register control for high impedance, independent for receiver and transmitter
- **Clock Inputs and Outputs**
  - Flexible master clock (N x 1.544 MHz or N x 2.048 MHz) ($1 \leq N \leq 8$, N is an integer number)
  - Two selectable reference clock outputs
    - *from the recovered clock of any of the 29 channels*
    - *from external clock input*
    - *from device master clock*
  - Integrated clock synthesizer can multiply or divide the reference clock to a wide range of frequencies: 8 KHz, 64 KHz, 2.048 MHz, 4.096 MHz, 8.192 MHz, 19.44 MHz and 32.768 MHz
  - Cascading is provided to select a single reference clock from multiple devices without the need for any external logic
- **Microprocessor Interface**
  - Supports Serial microprocessor interface and Parallel Intel / Motorola Non-Multiplexed /Multiplexed microprocessor interface
- **Other Key Features**
  - IEEE1149.1 JTAG boundary scan
  - Two general purpose I/O pins
  - 3.3 V I/O with 5 V tolerant inputs
  - 3.3 V and 1.8 V power supply
  - Package: 640-pin TEPBGA (31 mm X 31 mm)
- **Applicable Standards**
  - AT&T Pub 62411 Accunet T1.5 Service
  - ANSI T1.102, T1.403 and T1.231
  - Bellcore TR-TSY-000009, GR-253-CORE and GR-499-CORE
  - ETSI CTR12/13
  - ETS 300166 and ETS 300 233
  - G.703, G.735, G.736, G.742, G.772, G.775, G.783 and G.823
  - O.161
  - ITU I.431 and ITU O.171

APPLICATIONS

- **SDH/SONET multiplexers**
- **Central office or PBX (Private Branch Exchange)**
- **Digital access cross connects**
- **Remote wireless modules**
- **Microwave transmission systems**

DESCRIPTION

The IDT82P2828 is a 28+1 channels high-density T1/E1/J1 short haul Line Interface Unit. Each channel of the IDT82P2828 can be independently configured. The configuration is performed through a Serial or Parallel Intel/Motorola Non-Multiplexed /Multiplexed microprocessor interface.

In the receive path, through a Single Ended or Differential line interface, the received signal is processed by an adaptive Equalizer and then sent to a Slicer. Clock and data are recovered from the digital pulses output from the Slicer. After passing through an enabled or disabled Receive Jitter Attenuator, the recovered data is decoded using B8ZS/AMI/HDB3 line code rule in Single Rail NRZ Format mode and output to the system, or output to the system without decoding in Dual Rail NRZ Format mode and Dual Rail RZ Format mode.

In the transmit path, the data to be transmitted is input on TDn in Single Rail NRZ Format mode or TDPn/TDNn in Dual Rail NRZ Format mode and Dual Rail RZ Format mode, and is sampled by a transmit reference clock. The clock can be supplied externally from TCLKn or recovered from the input transmit data by an internal Clock Recovery. A selectable JA in Tx path is used to de-jitter gapped clocks. To meet T1/E1/J1 waveform standards, five preset T1 templates and two E1 templates, as well as an arbitrary waveform generator are provided. The data through the Waveform Shaper, the Line Driver and the Tx Transmitter is output on TTIPn and TRINGn.

Alarms (including LOS, AIS) and defects (including BPV, EXZ) are detected in both receive line side and transmit system side. AIS alarm, PRBS, ARB and IB patterns can be generated /detected in receive / transmit direction for testing purpose. Analog Loopback, Digital Loopback and Remote Loopback are all integrated for diagnostics.

Channel 0 is a special channel. Besides normal operation as the other 28 channels, channel 0 also supports G.772 Monitoring and Jitter Measurement per ITU O.171.

A line monitor function per T1.102 is available to provide a Non-Intrusive Monitoring of channels of other devices.

JTAG per IEEE 1149.1 is also supported by the IDT82P2828.

BLOCK DIAGRAM

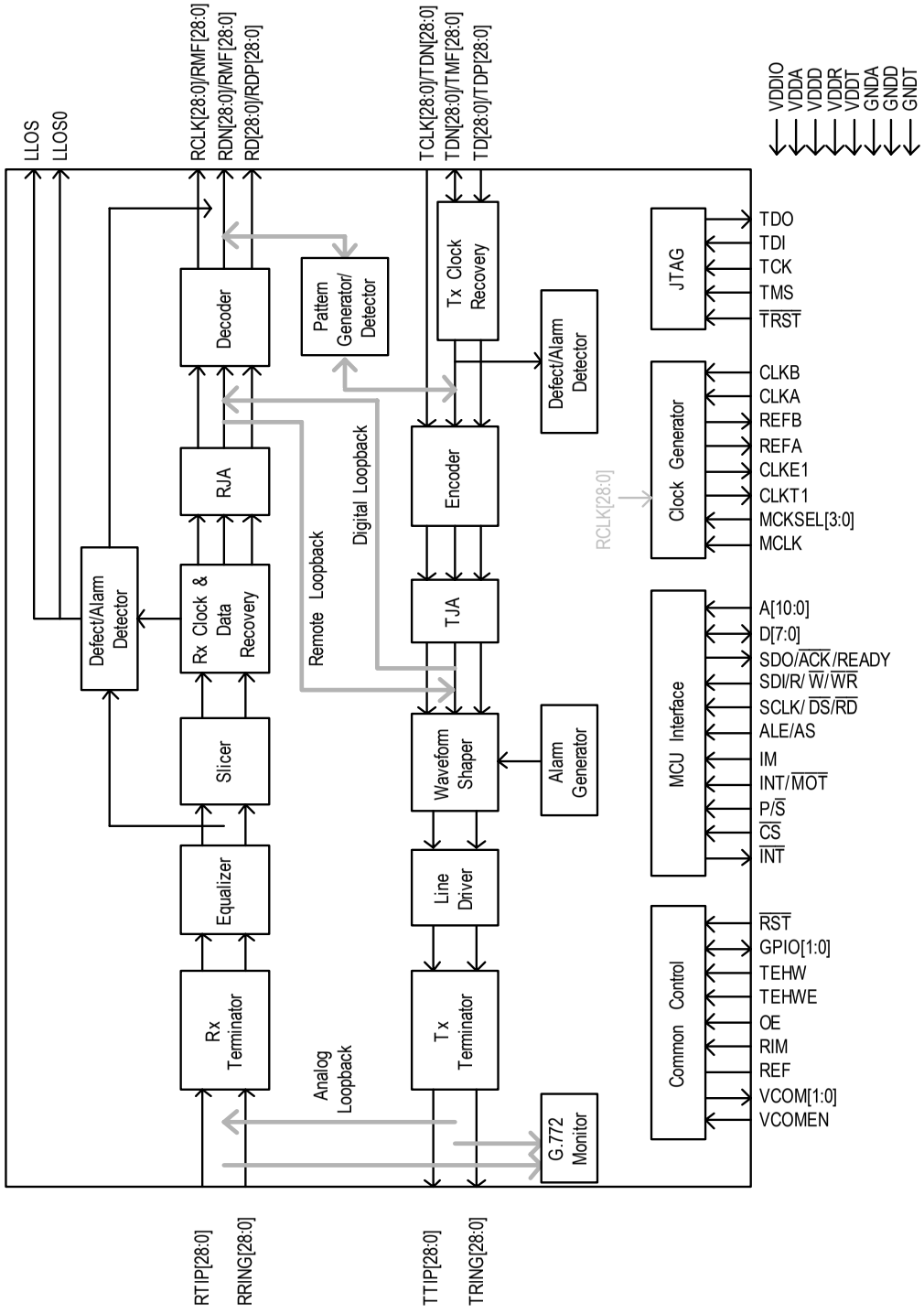

Figure-1 Functional Block Diagram

1 PIN ASSIGNMENT

Figure-2 shows the outline of the pin assignment. For a clearer description, four segments are divided in this figure and the details of each are shown from Figure-3 to Figure-6.

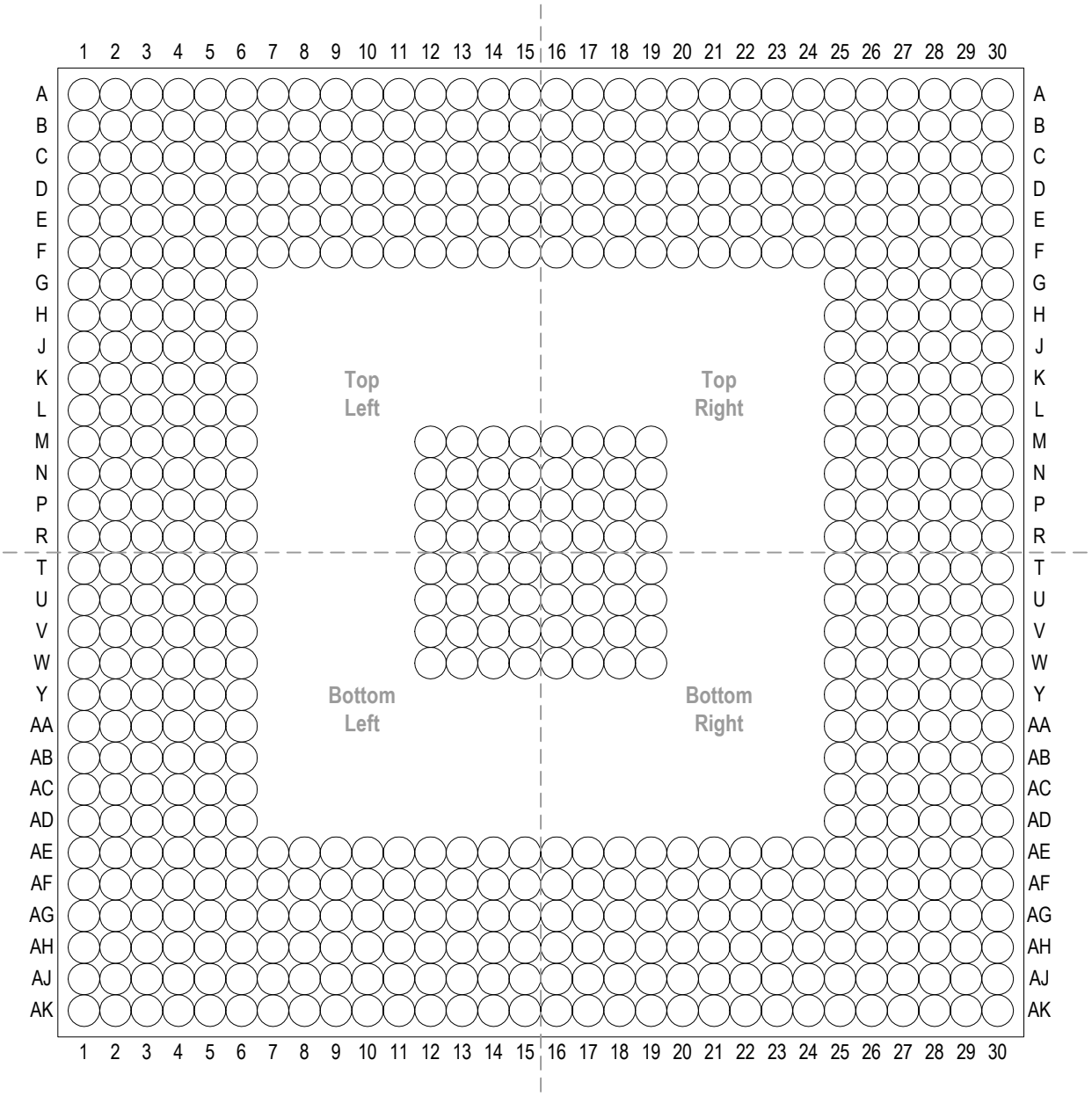

Figure-2 640-Pin PBGA (Top View) - Outline

Figure-3 640-Pin PBGA (Top View) - Top Left

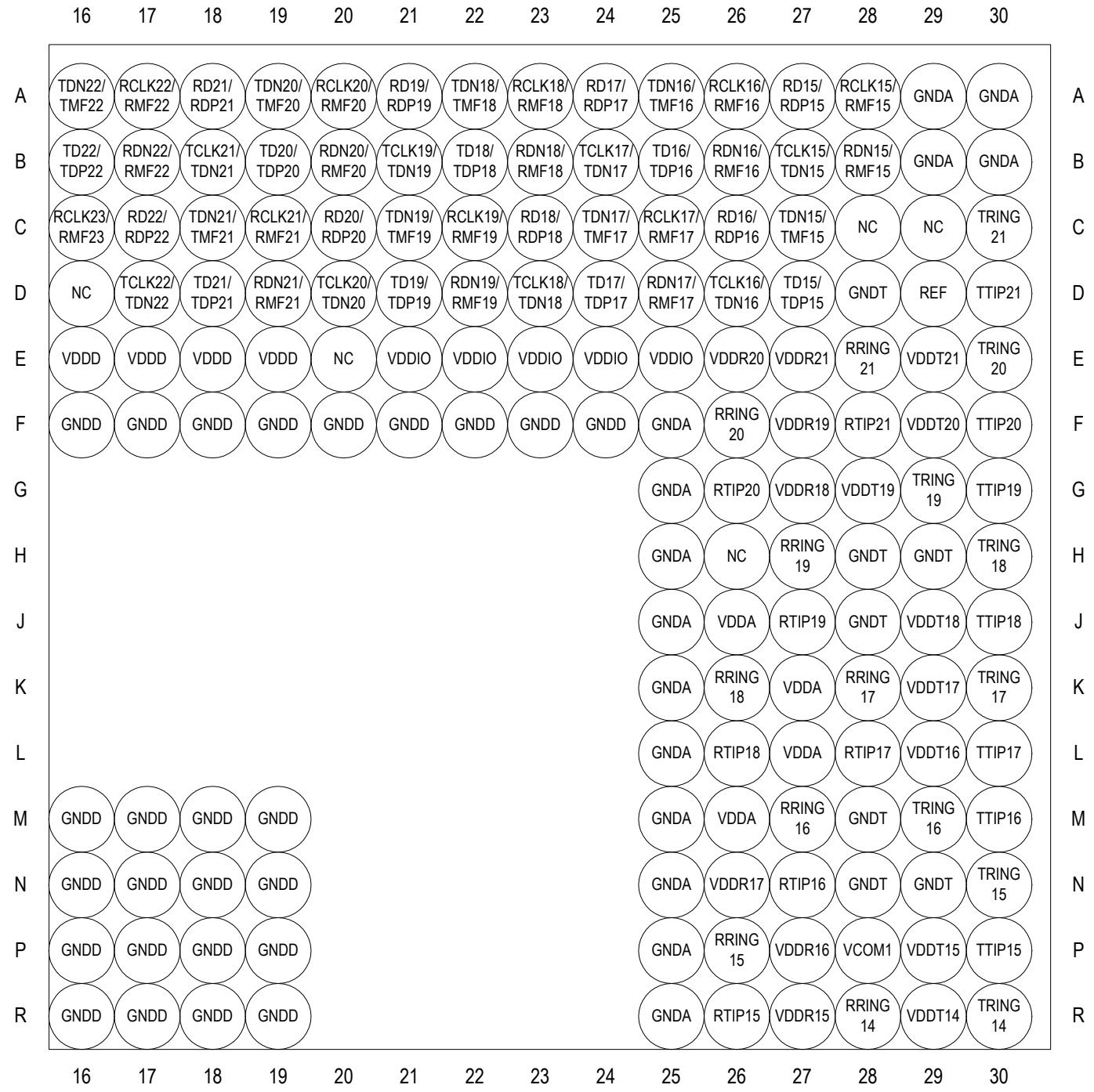

Figure-4 640-Pin PBGA (Top View) - Top Right

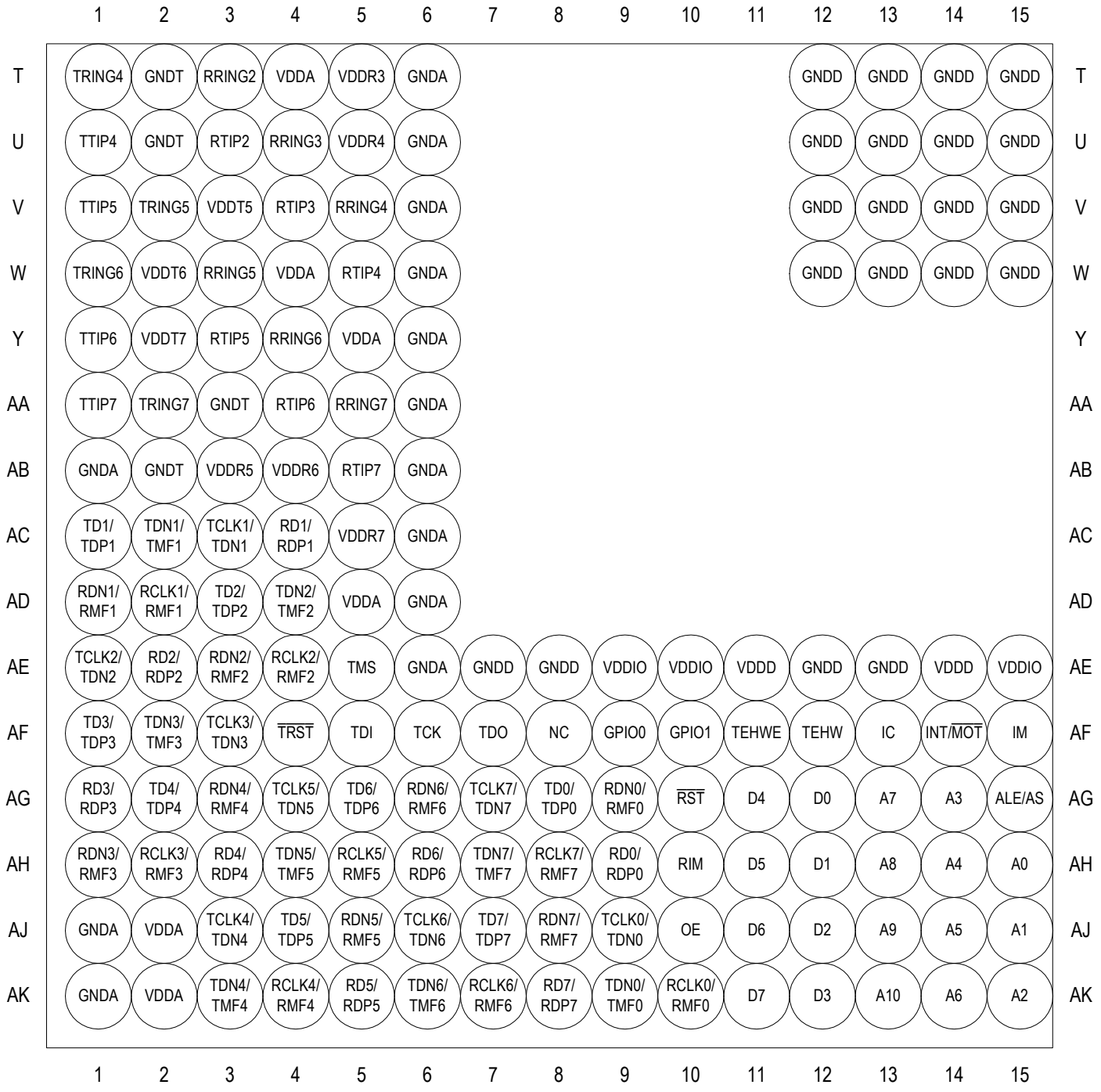

Figure-5 640-Pin PBGA (Top View) - Bottom Left

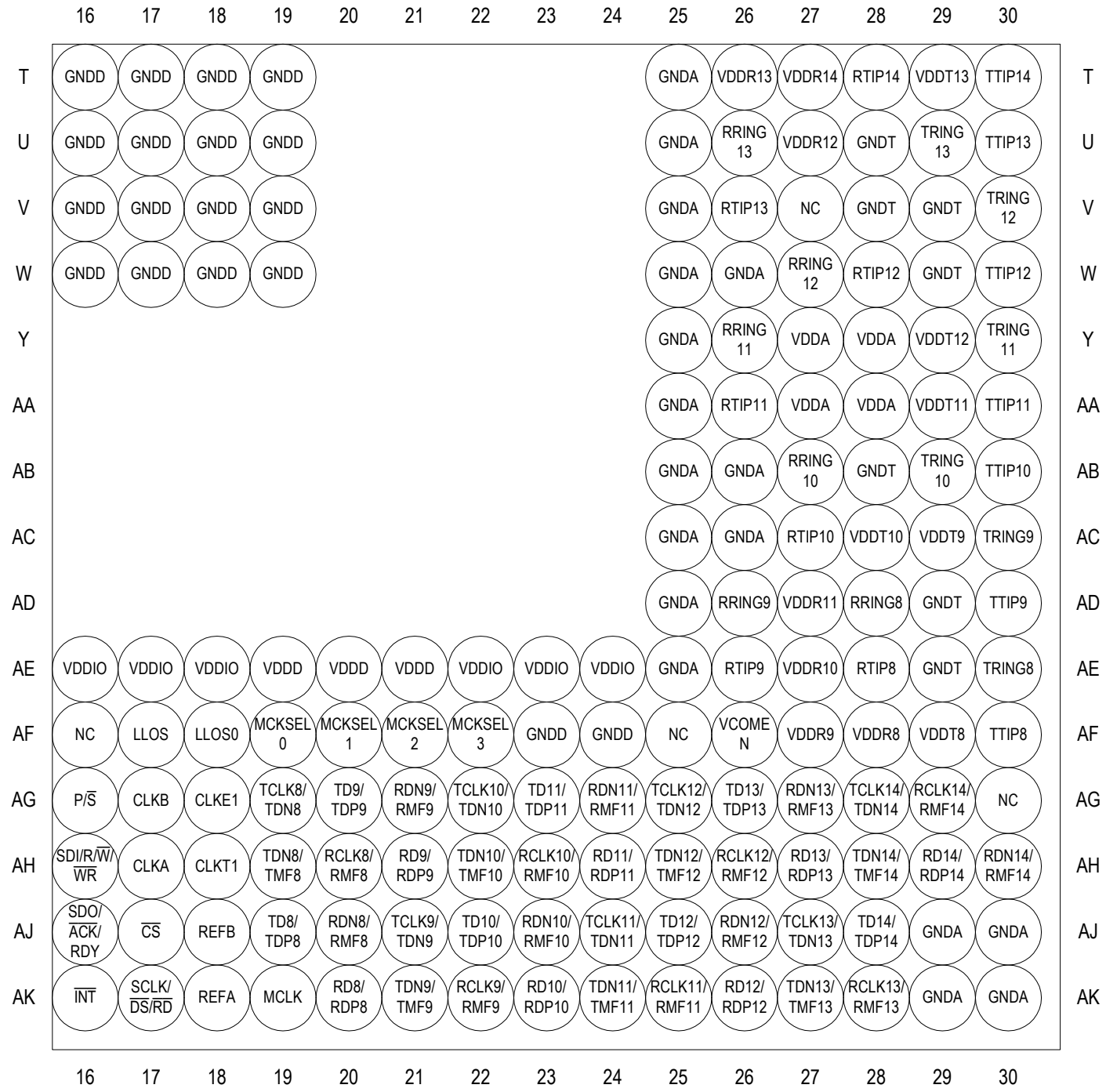

Figure-6 640-Pin PBGA (Top View) - Bottom Right

2 PIN DESCRIPTION

Name	I / O	Pin No. [1]	Description
Line Interface			
RTIPn RRINGn (n=0~28)	Input	P3, R5, U3, V4, W5, Y3, AA4, AB5, AE28, AE26, AC27, AA26, W28, V26, T28, R26, N27, L28, L26, J27, G26, F28, D6, D4, D3, G4, H5, K4, M5 N3, P5, T3, U4, V5, W3, Y4, AA5, AD28, AD26, AB27, Y26, W27, U26, R28, P26, M27, K28, K26, H27, F26, E28, E6, D5, E3, F4, G5, J4, L5	**RTIPn / RRINGn: Receive Bipolar Tip/Ring for Channel 0 ~ 28** The receive line interface supports both Receive Differential mode and Receive Single Ended mode. In Receive Differential mode, the received signal is coupled into RTIPn and RRINGn via a 1:1 transformer or without a transformer (transformer-less). In Receive Single Ended mode, RRINGn should be left open. The received signal is input on RTIPn via a 2:1 (step down) transformer or without a transformer (transformer-less). These pins will become High-Z globally or channel specific in the following conditions: • Global High-Z: - Connecting the RIM pin to low; - Loss of MCLK - During and after power-on reset, hardware reset or global software reset; • Per-channel High-Z - Receiver power down by writing '1' to the R_OFF bit (b5, RCF0,...)
TTIPn TRINGn (n=0~28)	Output	L1, M1, P1, R1, U1, V1, Y1, AA1, AF30, AD30, AB30, AA30, W30, U30, T30, P30, M30, L30, J30, G30, F30, D30, A5, A4, A3, C1, F1, H1, J1 K1, M2, N1, R2, T1, V2, W1, AA2, AE30, AC30, AB29, Y30, V30, U29, R30, N30, M29, K30, H30, G29, E30, C30, A6, B4, B3, D1, E1, G1, J2	**TTIPn / TRINGn: Transmit Bipolar Tip /Ring for Channel 0 ~ 28** The transmit line interface supports both Transmit Differential mode and Transmit Single Ended mode. In Transmit Differential mode, TTIPn outputs a positive differential pulse while TRINGn outputs a negative differential pulse. The pulses are coupled to the line side via a 1:2 (step up) transformer or without a transformer (transformer-less). In Transmit Single Ended mode, TRINGn should be left open (it is shorted to ground internally). The signal presented at TTIPn is output to the line side via a 1:2 (step up) transformer. These pins will become High-Z globally or channel specific in the following conditions: • Global High-Z: - Connecting the OE pin to low; - Loss of MCLK; - During and after power-on reset, hardware reset or global software reset; • Per-channel High-Z - Writing '0' to the OE bit (b6, TCF0,...) [2]; - Loss of TCLKn in Transmit Single Rail NRZ Format mode or Transmit Dual Rail NRZ Format mode, except that the channel is in Remote Loopback or transmit internal pattern with XCLK [3]; - Transmitter power down by writing '1' to the T_OFF bit (b5, TCF0,...); - Per-channel software reset; - The THZ_OC bit (b4, TCF0,...) is set to '1' and the transmit driver over-current is detected. Refer to Section 3.3.8 Output High-Z on TTIP and TRING for details.

Note:

1. The pin number of the pins with the footnote 'n' is listed in order of channel (CH0 ~ CH28).

2. The content in the brackets indicates the position and the register name of the preceding bit. After the register name, if the punctuation '...' is followed, this bit is in a per-channel register. If there is no punctuation following the address, this bit is in a global register or in a channel 0 only register. The addresses and details are included in Chapter 5 Programming Information.

3. XCLK is derived from MCLK. It is 1.544 MHz in T1/J1 mode or 2.048 MHz in E1 mode.

Name	I / O	Pin No.	Description
		System Interface	
RDn / RDPn (n=0~28)	Output	AH9, AC4, AE2, AG1, AH3, AK5, AH6, AK8, AK20, AH21, AK23, AH24, AK26, AH27, AH29, A27, C26, A24, C23, A21, C20, A18, C17, B15, D14, B12, D11, B9, D8	**RDn: Receive Data for Channel 0 ~ 28** When the receive system interface is configured to Single Rail NRZ Format mode, this multiplex pin is used as RDn. The decoded NRZ data is updated on the active edge of RCLKn. The active level on RDn is selected by the RD_INV bit (b3, RCF1,...). When the receiver is powered down, RDn will be in High-Z state or low, as selected by the RHZ bit (b6, RCF0,...). **RDPn: Positive Receive Data for Channel 0 ~ 28** When the receive system interface is configured to Dual Rail NRZ Format mode, Dual Rail RZ Format mode or Dual Rail Sliced mode, this multiplex pin is used as RDPn. In Receive Dual Rail NRZ Format mode, the un-decoded NRZ data is output on RDPn and RDNn and updated on the active edge of RCLKn. In Receive Dual Rail RZ Format mode, the un-decoded RZ data is output on RDPn and RDNn and updated on the active edge of RCLKn. In Receive Dual Rail Sliced mode, the raw RZ sliced data is output on RDPn and RDNn. For Receive Differential line interface, an active level on RDPn indicates the receipt of a positive pulse on RTIPn and a negative pulse on RRINGn; while an active level on RDNn indicates the receipt of a negative pulse on RTIPn and a positive pulse on RRINGn. For Receive Single Ended line interface, an active level on RDPn indicates the receipt of a positive pulse on RTIPn; while an active level on RDNn indicates the receipt of a negative pulse on RTIPn. The active level on RDPn and RDNn is selected by the RD_INV bit (b3, RCF1,...). When the receiver is powered down, RDPn and RDNn will be in High-Z state or low, as selected by the RHZ bit (b6, RCF0,...).
RDNn / RMFn (n=0~28)	Output	AG9, AD1, AE3, AH1, AG3, AJ5, AG6, AJ8, AJ20, AG21, AJ23, AG24, AJ26, AG27, AH30, B28, B26, D25, B23, D22, B20, D19, B17, A15, C14, A12, C11, A9, C8	**RDNn: Negative Receive Data for Channel 0 ~ 28** When the receive system interface is configured to Dual Rail NRZ Format mode, Dual Rail RZ Format mode or Dual Rail Sliced mode, this multiplex pin is used as RDNn. (Refer to the description of RDPn for details). **RMFn: Receive Multiplex Function for Channel 0 ~ 28** When the receive system interface is configured to Single Rail NRZ Format mode, this multiplex pin is used as RMFn. RMFn is configured by the RMF_DEF[2:0] bits (b7~5, RCF1,...) and can indicate PRBS/ARB, LAIS, LEXZ, LBPV, LEXZ+LBPV, LLOS, output recovered clock (RCLK) or XOR output of positive and negative sliced data. Refer to Section 3.5.7.1 RMFn Indication for details. The output on RMFn is updated on the active edge of RCLKn. The active level of RMFn is always high. When the receiver is powered down, RMFn will be in High-Z state or low, as selected by the RHZ bit (b6, RCF0,...).

Name	I / O	Pin No.	Description
RCLKn / RMFn (n=0~28)	Output	AK10, AD2, AE4, AH2, AK4, AH5, AK7, AH8, AH20, AK22, AH23, AK25, AH26, AK28, AG29, A28, A26, C25, A23, C22, A20, C19, A17, C16, B14, D13, B11, D10, B8	**RCLKn: Receive Clock for Channel 0 ~ 28** When the receive system interface is configured to Single Rail NRZ Format mode, Dual Rail NRZ Format mode or Dual Rail RZ Format mode, this multiplex pin is used as RCLKn. RCLKn outputs a 1.544 MHz (in T1/J1 mode) or 2.048 MHz (in E1 mode) clock which is recovered from the received signal. The data output on RDn and RMFn (in Receive Single Rail NRZ Format mode) or RDPn/RDNn (in Receive Dual Rail NRZ Format mode, Receive Dual Rail RZ Format mode and Receive Dual Rail Sliced) is updated on the active edge of RCLKn. The active edge is selected by the RCK_ES bit (b4, RCF1,...). In LLOS condition, RCLKn output high or XCLK, as selected by the RCKH bit (b7, RCF0,...) (refer to Section 3.5.3.1 Line LOS (LLOS) for details). When the receiver is powered down, RCLKn will be in High-Z state or low, as selected by the RHZ bit (b6, RCF0,...). **RMFn: Receive Multiplex Function for Channel 0 ~ 28** When the receive system interface is configured to Dual Rail Sliced mode, this multiplex pin is used as RMFn. (Refer to the description of RMFn of the RDNn/RMFn multiplex pin for details).
LLOS	Output	AF17	**LLOS: Receive Line Loss Of Signal** LLOS synchronizes with the output of CLKE1 and can indicate the LLOS (Line LOS) status of all 29 channels in a serial format. When the clock output on CLKE1 is enabled, LLOS indicates the LLOS status of the 29 channels in a serial format and repeats every twenty-nine cycles. Channel 0 is positioned by LLOS0. Refer to the description of LLOS0 below for details. LLOS is updated on the rising edge of CLKE1 and is always active high. When the clock output of CLKE1 is disabled, LLOS will be held in High-Z state. (Refer to Section 3.5.3.1 Line LOS (LLOS) for details.)
LLOS0	Output	AF18	**LLOS0: Receive Line Loss Of Signal for Channel 0** LLOS0 can indicate the position of channel 0 on the LLOS pin. When the clock output on CLKE1 is enabled, LLOS0 pulses high for one CLKE1 clock cycle to indicate the position of channel 0 on the LLOS pin. When CLKE1 outputs 8 KHz clock, LLOS0 pulses high for one 8 KHz clock cycle (125 µs) every twenty-nine 8 KHz clock cycles; when CLKE1 outputs 2.048 MHz clock, LLOS0 pulses high for one 2.048 MHz clock cycle (488 ns) every twenty-nine 2.048 MHz clock cycles. LLOS0 is updated on the rising edge of CLKE1. When the clock output on CLKE1 is disabled, LLOS0 will be held in High-Z state. (Refer to Section 3.5.3.1 Line LOS (LLOS) for details.)

<table>
<tr><th>Name</th><th>I / O</th><th>Pin No.</th><th>Description</th></tr>
<tr><td>TDn / TDPn

(n=0~28)</td><td>Input</td><td>AG8, AC1, AD3, AF1, AG2, AJ4, AG5, AJ7, AJ19, AG20, AJ22, AG23, AJ25, AG26, AJ28, D27, B25, D24, B22, D21, B19, D18, B16, A14, C13, A11, C10, A8, C7</td><td>TDn: Transmit Data for Channel 0 ~ 28
When the transmit system interface is configured to Single Rail NRZ Format mode, this multiplex pin is used as TDn.
TDn accepts Single Rail NRZ data. The data is sampled into the device on the active edge of TCLKn.
The active level on TDn is selected by the TD_INV bit (b3, TCF1,...).

TDPn: Positive Transmit Data for Channel 0 ~ 28
When the transmit system interface is configured to Dual Rail NRZ Format mode or Dual Rail RZ Format mode, this multiplex pin is used as TDPn.
In Transmit Dual Rail NRZ Format mode, the pre-encoded NRZ data is input on TDPn and TDNn and sampled on the active edge of TCLKn.
In Transmit Dual Rail RZ Format mode, the pre-encoded RZ data is input on TDPn and TDNn. The line code is as follows (when the TD_INV bit (b3, TCF1,...) is ‘0’):
<table><tr><th>TDPn</th><th>TDNn</th><th>Output Pulse on TTIPn</th><th>Output Pulse on TRINGn *</th></tr><tr><td>0</td><td>0</td><td>Space</td><td>Space</td></tr><tr><td>0</td><td>1</td><td>Negative Pulse</td><td>Positive Pulse</td></tr><tr><td>1</td><td>0</td><td>Positive Pulse</td><td>Negative Pulse</td></tr><tr><td>1</td><td>1</td><td>Space</td><td>Space</td></tr><tr><td colspan="4">Note:
* For Transmit Single Ended line interface, TRINGn should be open.</td></tr></table>
The active level on TDPn and TDNn is selected by the TD_INV bit (b3, TCF1,...).</td></tr>
<tr><td>TDNn / TMFn

(n=0~28)</td><td>Input / Output</td><td>AK9, AC2, AD4, AF2, AK3, AH4, AK6, AH7, AH19, AK21, AH22, AK24, AH25, AK27, AH28, C27, A25, C24, A22, C21, A19, C18, A16, D15, B13, D12, B10, D9, B7</td><td>TDNn: Negative Transmit Data for Channel 0 ~ 28
When the transmit system interface is configured to Dual Rail NRZ Format mode, this multiplex pin is used as TDNn.
(Refer to the description of TDPn for details).

TMFn: Transmit Multiplex Function for Channel 0 ~ 28
When the transmit system interface is configured to Single Rail NRZ Format mode or Dual Rail RZ Format mode, this multiplex pin is used as TMFn.
TMFn is configured by the TMF_DEF[2:0] bits (b7~5, TCF1,...) and can indicate PRBS/ARB, SAIS, TOC, TLOS, SEXZ, SBPV, SEXZ+SBPV, SLOS. Refer to Section 3.5.7.2 TMFn Indication for details.
The output on TMFn is updated on the active edge of TCLKn (if available). The active level of TMFn is always high.</td></tr>
<tr><td>TCLKn / TDNn

(n=0~28)</td><td>Input</td><td>AJ9, AC3, AE1, AF3, AJ3, AG4, AJ6, AG7, AG19, AJ21, AG22, AJ24, AG25, AJ27, AG28, B27, D26, B24, D23, B21, D20, B18, D17, C15, A13, C12, A10, C9, A7</td><td>TCLKn: Transmit Clock for Channel 0 ~ 28
When the transmit system interface is configured to Single Rail NRZ Format mode or Dual Rail NRZ Format mode, this multiplex pin is used as TCLKn.
TCLKn inputs a 1.544 MHz (in T1/J1 mode) or 2.048 MHz (in E1 mode) clock.
The data input on TDn (in Transmit Single Rail NRZ Format mode) or TDPn/TDNn (in Transmit Dual Rail NRZ Format mode) is sampled on the active edge of TCLKn. The data output on TMFn (in Transmit Single Rail NRZ Format mode) is updated on the active edge of TCLKn. The active edge is selected by the TCK_ES bit (b4, TCF1,...).

TDNn: Negative Transmit Data for Channel 0 ~ 28
When the transmit system interface is configured to Dual Rail RZ Format mode, this multiplex pin is used as TDNn.
(Refer to the description of TDPn for details).</td></tr>
</table>

<table>
<tr><th>Name</th><th>I / O</th><th>Pin No.</th><th>Description</th></tr>
<tr><td colspan="4">Clock</td></tr>
<tr><td>MCLK</td><td>Input</td><td>AK19</td><td>MCLK: Master Clock Input
MCLK provides a stable reference timing for the IDT82P2828. MCLK should be a clock with +/-32 ppm (in T1/J1 mode) or +/-50 ppm (in E1 mode) accuracy. The clock frequency of MCLK is informed to the device by MCKSEL[3:0].
If MCLK misses (duty cycle is less than 30% for 10 µs) and then recovers, the device will be reset automatically.</td></tr>
<tr><td>MCKSEL[0]
MCKSEL[1]
MCKSEL[2]
MCKSEL[3]</td><td>Input</td><td>AF19
AF20
AF21
AF22</td><td>MCKSEL[3:0]: Master Clock Selection
These four pins inform the device of the clock frequency input on MCLK:
<table>
<tr><th>MCKSEL[3:0]*</th><th>Frequency (MHz)</th></tr>
<tr><td>0000</td><td>1.544</td></tr>
<tr><td>0001</td><td>1.544 X 2</td></tr>
<tr><td>0010</td><td>1.544 X 3</td></tr>
<tr><td>0011</td><td>1.544 X 4</td></tr>
<tr><td>0100</td><td>1.544 X 5</td></tr>
<tr><td>0101</td><td>1.544 X 6</td></tr>
<tr><td>0110</td><td>1.544 X 7</td></tr>
<tr><td>0111</td><td>1.544 X 8</td></tr>
<tr><td>1000</td><td>2.048</td></tr>
<tr><td>1001</td><td>2.048 X 2</td></tr>
<tr><td>1010</td><td>2.048 X 3</td></tr>
<tr><td>1011</td><td>2.048 X 4</td></tr>
<tr><td>1100</td><td>2.048 X 5</td></tr>
<tr><td>1101</td><td>2.048 X 6</td></tr>
<tr><td>1110</td><td>2.048 X 7</td></tr>
<tr><td>1111</td><td>2.048 X 8</td></tr>
</table>
Note:
0: GNDD
1: VDDIO</td></tr>
<tr><td>CLKT1</td><td>Output</td><td>AH18</td><td>CLKT1: 8 KHz / T1 Clock Output
The output on CLKT1 can be enabled or disabled, as determined by the CLKT1_EN bit (b1, CLKG).
When the output is enabled, CLKT1 outputs an 8 KHz or 1.544 MHz clock, as selected by the CLKT1 bit (b0, CLKG). The output is locked to MCLK.
When the output is disabled, CLKT1 is in High-Z state.</td></tr>
<tr><td>CLKE1</td><td>Output</td><td>AG18</td><td>CLKE1: 8 KHz / E1 Clock Output
The output on CLKE1 can be enabled or disabled, as determined by the CLKE1_EN bit (b3, CLKG).
When the output is enabled, CLKE1 outputs an 8 KHz or 2.048 MHz clock, as selected by the CLKE1 bit (b2, CLKG). The output is locked to MCLK.
When the output is disabled, CLKE1 is in High-Z state.</td></tr>
</table>

Name	I / O	Pin No.	Description
REFA	Output	AK18	**REFA: Reference Clock Output A** REFA can output three kinds of clocks: a recovered clock of one of the 29 channels, an external clock input on CLKA or a free running clock. The clock frequency is programmable. Refer to Section 3.6.2 Clock Outputs on REFA/REFB for details. The output on REFA can also be disabled, as determined by the REFA_EN bit (b6, REFA). When the output is disabled, REFA is in High-Z state.
REFB	Output	AJ18	**REFB: Reference Clock Output B** REFB can output a recovered clock of one of the 29 channels, an external clock input on CLKB or a free running clock. Refer to Section 3.6.2 Clock Outputs on REFA/REFB for details. The output on REFB can also be disabled, as determined by the REFB_EN bit (b6, REFB). When the output is disabled, REFB is in High-Z state.
CLKA	Input	AH17	**CLKA: External T1/E1 Clock Input A** External T1/J1 (1.544 MHz) or E1 (2.048 MHz) clock is input on this pin. The CKA_T1E1 bit (b5, REFA) should be set to match the clock frequency. When not used, this pin should be connected to GNDD.
CLKB	Input	AG17	**CLKB: External T1/E1 Clock Input B** External T1/J1 (1.544 MHz) or E1 (2.048 MHz) clock is input on this pin. The CKB_T1E1 bit (b5, REFB) should be set to match the clock frequency. When not used, this pin should be connected to GNDD.
Common Control			
VCOM[0] VCOM[1]	Output	R4 P28	**VCOM: Voltage Common Mode [1:0]** These pins are used only when the receive line interface is in Receive Differential mode and connected without a transformer (transformer-less). To enable these pins, the VCOMEN pin must be connected high. Refer to Figure-10 for the connection. When these pins are not used, they should be left open.
VCOMEN	Input (Pull-Down)	AF26	**VCOMEN: Voltage Common Mode Enable** This pin should be connected high only when the receive line interface is in Receive Differential mode and connected without a transformer (transformer-less). When not used, this pin should be left open.
REF	-	D29	**REF: Reference Resistor** An external resistor (10 KΩ, ±1%) is used to connect this pin to ground to provide a standard reference current for internal circuit. This resistor is required to ensure correct device operation.
RIM	Input (Pull-Down)	AH10	**RIM: Receive Impedance Matching** In Receive Differential mode, when RIM is low, all 29 receivers become High-Z and only external impedance matching is supported. In this case, the per-channel impedance matching configuration bits - the R_TERM[2:0] bits (b2~0, RCF0,...) and the R120IN bit (b4, RCF0,...) - are ignored. In Receive Differential mode, when RIM is high, impedance matching is configured on a per-channel basis by the R_TERM[2:0] bits (b2~0, RCF0,...) and the R120IN bit (b4, RCF0,...). This pin can be used to control the receive impedance state for Hitless Protection applications. Refer to Section 4.4 Hitless Protection Switching (HPS) Summary for details. In Receive Single Ended mode, this pin should be left open.

Name	I / O	Pin No.	Description
OE	Input	AJ10	**OE: Output Enable** OE enables or disables all Line Drivers globally. A high level on this pin enables all Line Drivers while a low level on this pin places all Line Drivers in High-Z state and independent from related register settings. Note that the functionality of the internal circuit is not affected by OE. If this pin is not used, it should be tied to VDDIO. This pin can be used to control the transmit impedance state for Hitless protection applications. Refer to Section 4.4 Hitless Protection Switching (HPS) Summary for details.
TEHWE	Input (Pull-Up)	AF11	**TEHWE: Hardware T1/J1 or E1 Mode Selection Enable** When this pin is open, the T1/J1 or E1 operation mode is selected by TEHW globally. When this pin is low, the T1/J1 or E1 operation mode is selected by the T1E1 bit (b0, CHCF,...) on a per-channel basis.
TEHW	Input (Pull-Up)	AF12	**TEHW: Hardware T1/J1 or E1 Mode Selection** When TEHWE is open, this pin selects the T1/J1 or E1 operation mode globally: Low - E1 mode; Open - T1/J1 mode. When TEHWE is low, the input on this pin is ignored.
GPIO[0] GPIO[1]	Output / Input	AF9 AF10	**GPIO: General Purpose I/O [1:0]** These two pins can be defined as input pins or output pins by the DIR[1:0] bits (b1~0, GPIO) respectively. When the pins are input, their polarities are indicated by the LEVEL[1:0] bits (b3~2, GPIO) respectively. When the pins are output, their polarities are controlled by the LEVEL[1:0] bits (b3~2, GPIO) respectively.
$\overline{RST}$	Input	AG10	**$\overline{RST}$: Reset (Active Low)** A low pulse on this pin resets the device. This hardware reset process completes in 2 µs maximum. Refer to Section 4.1 Reset for an overview on reset options.
			MCU Interface
$\overline{INT}$	Output	AK16	**$\overline{INT}$: Interrupt Request** This pin indicates interrupt requests for all unmasked interrupt sources. The output characteristics (open drain or push-pull internally) and the active level are determined by the INT_PIN[1:0] bits (b3~2, GCF).
$\overline{CS}$	Input	AJ17	**$\overline{CS}$: Chip Select (Active Low)** This pin must be asserted low to enable the microprocessor interface. A transition from high to low must occur on this pin for each Read/Write operation and $\overline{CS}$ should remain low until the operation is over.
P/$\overline{S}$	Input	AG16	**P/$\overline{S}$: Parallel or Serial Microprocessor Interface Select** P/$\overline{S}$ selects Serial or Parallel microprocessor interface for the device: GNDD - Serial microprocessor interface. VDDIO - Parallel microprocessor interface. Serial microprocessor interface consists of the $\overline{CS}$, SCLK, SDI, SDO pins. Parallel microprocessor interface consists of the $\overline{CS}$, INT/$\overline{MOT}$, IM, $\overline{DS}$/$\overline{RD}$, ALE/AS, R/$\overline{W}$/$\overline{WR}$, $\overline{ACK}$/RDY, D[7:0], A[10:0] pins.
INT/$\overline{MOT}$	Input (Pull-Up)	AF14	**INT/$\overline{MOT}$: Intel or Motorola Microprocessor Interface Select** In Parallel microprocessor interface, INT/$\overline{MOT}$ selects Intel or Motorola microprocessor interface for the device: GNDD - Parallel Motorola microprocessor interface. Open - Parallel Intel microprocessor interface. In Serial microprocessor interface, this pin should be left open.

Name	I / O	Pin No.	Description
IM	Input (Pull-Up)	AF15	**IM: Interface Mode Selection** In Parallel Motorola or Intel microprocessor interface, IM selects multiplexed bus or non-multiplexed bus for the device: GNDD - Parallel Motorola /Intel Non-Multiplexed microprocessor interface. Open - Parallel Motorola /Intel Multiplexed microprocessor interface. In Serial microprocessor interface, this pin should be connected to GNDD.
ALE / AS	Input	AG15	**ALE: Address Latch Enable** In Parallel Intel Multiplexed microprocessor interface, this multiplex pin is used as ALE. The address on A[10:8] and D[7:0] (A[7:0] are ignored) is sampled into the device on the falling edges of ALE. **AS: Address Strobe** In Parallel Motorola Multiplexed microprocessor interface, this multiplex pin is used as AS. The address on A[10:8] and D[7:0] (A[7:0] are ignored) is latched into the device on the falling edges of AS. In Parallel Motorola /Intel Non-Multiplexed microprocessor interface, this pin should be pulled high. In Serial microprocessor interface, this pin should be connected to GNDD.
SCLK / $\overline{DS}$ / $\overline{RD}$	Input	AK17	**SCLK: Shift Clock** In Serial microprocessor interface, this multiplex pin is used as SCLK. SCLK inputs the shift clock for the Serial microprocessor interface. Data on SDI is sampled by the device on the rising edge of SCLK. Data on SDO is updated on the falling edge of SCLK. **$\overline{DS}$: Data Strobe (Active Low)** In Parallel Motorola microprocessor interface, this multiplex pin is used as $\overline{DS}$. During a write operation (R/$\overline{W}$ = 0), data on D[7:0] is sampled into the device. During a read operation (R/$\overline{W}$ = 1), data is driven to D[7:0] by the device. **$\overline{RD}$: Read Strobe (Active Low)** In Parallel Intel microprocessor interface, this multiplex pin is used as $\overline{RD}$. $\overline{RD}$ is asserted low by the microprocessor to initiate a read operation. Data is driven to D[7:0] by the device during the read operation.
SDI / R/$\overline{W}$ / $\overline{WR}$	Input	AH16	**SDI: Serial Data Input** In Serial microprocessor interface, this multiplex pin is used as SDI. Address and data on this pin are serially clocked into the device on the rising edge of SCLK. **R/$\overline{W}$: Read / Write Select** In Parallel Motorola microprocessor interface, this multiplex pin is used as R/$\overline{W}$. R/$\overline{W}$ is asserted low for write operation or high for read operation. **$\overline{WR}$: Write Strobe (Active Low)** In Parallel Intel microprocessor interface, this multiplex pin is used as $\overline{WR}$. $\overline{WR}$ is asserted low by the microprocessor to initiate a write operation. Data on D[7:0] is sampled into the device during a write operation.