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Highlights

- Synchronous Equipment Timing Source (SETS) for Synchronous Ethernet (SyncE) per ITU-T G.8264
- DPLL1 generates ITU-T G.8262 compliant SyncE clocks, Telcordia GR-1244-CORE/GR-253-CORE, and ITU-T G.813 compliant SONET/SDH clocks
- DPLL2 performs rate conversions for synchronization interfaces or for other general purpose timing applications
- DPLL1 can be configured as a Digitally Controlled Oscillators (DCOs) for PTP clock synthesis
- DCO frequency resolution is [(77760 / 1638400) * 2^-48] or ~1.686305041e-10 ppm
- APLL1 and APLL2 generate clocks with jitter < 1 ps RMS (12 kHz to 20 MHz) for: 1000BASE-T and 1000BASE-X
- Fractional-N input dividers support a wide range of reference frequencies
- Locks to 1 Pulse Per Second (PPS) references
- DPLLs, APLL1 and APLL2 can be configured from an external EEPROM after reset

Features

- Differential reference inputs (IN1 to IN4) accept clock frequencies between 1 PPS and 650 MHz
- Single ended inputs (IN5 to IN6) accept reference clock frequencies between 1 PPS and 162.5 MHz
- Loss of Signal (LOS) pins (LOS0 to LOS3) can be assigned to any clock reference input
- Reference monitors qualify/disqualify references depending on activity, frequency and LOS pins
- Automatic reference selection state machines select the active reference for each DPLL based on the reference monitors, priority tables, revertive and non-revertive settings and other programmable settings
- Fractional-N input dividers enable the DPLLs to lock to a wide range of reference clock frequencies including: 10/100/1000 Ethernet, 10G Ethernet, OTN, SONET/SDH, PDH, TDM, GSM, CPRI, and GNSS frequencies
- Any reference inputs (IN1 to IN6) can be designated as external sync pulse inputs (1 PPS, 2 kHz, 4 kHz or 8 kHz) associated with a selectable reference clock input
- FRSYNC_8K_1PPS and MFRSYNC_2K_1PPS output sync pulses that are aligned with the selected external input sync pulse input and frequency locked to the associated reference clock input
- DPLL1 can be configured with bandwidths between 0.09 mHz and 567 Hz
- DPLL1 locks to input references with frequencies between 1 PPS and 650 MHz
- DPLL2 locks to input references with frequencies between 8 kHz and 650 MHz
- DPLL1 complies with ITU-T G.8262 for Synchronous Ethernet Equipment Clock (EEC), and G.813 for Synchronous Equipment Clock (SEC); and Telcordia GR-253-CORE/ GR-1244-CORE for Stratum 3 and SONET Minimum Clock (SMC)
- DPLL1 generates clocks with PDH, TDM, GSM, CPRI/OBSAI, 10/100/1000 Ethernet and GNSS frequencies; these clocks are directly available on OUT1 and OUT8
- DPLL2 generates N x 8 kHz clocks up to 100 MHz that are output on OUT9 and OUT10
- APLL1 and APLL2 are connected to DPLL1
- APLL1 and APLL2 generate 10/100/1000 Ethernet, 10G Ethernet, or SONET/SDH frequencies
- Any of eight common TCXO/OCXO frequencies can be used for the System Clock: 10 MHz, 12.8 MHz, 13 MHz, 19.44 MHz, 20 MHz, 24.576 MHz, 25 MHz or 30.72 MHz
- The I2C slave, SPI or the UART interface can be used by a host processor to access the control and status registers
- The I2C master interface can automatically load a device configuration from an external EEPROM after reset
- Differential outputs OUT3 to OUT6 output clocks with frequencies between 1 PPS and 650 MHz
- Single ended outputs OUT1, OUT2, OUT7 and OUT8 output clocks with frequencies between 1 PPS and 125 MHz
- Single ended outputs OUT9 and OUT10 output clocks N*8 kHz multiples up to 100 MHz
- DPLL1 supports independent programmable delays for each of IN1 to IN6; the delay for each input is programmable in steps of 0.61 ns with a range of ~±78 ns
- The input to output phase delay of DPLL1 is programmable in steps of 0.0745 ps with a total range of ±20 µs
- The clock phase of each of the output dividers for OUT1 (from APLL1) to OUT8 is individually programmable in steps of ~200 ps with a total range of +/-180°
- 1149.1 JTAG Boundary Scan
- 72-pin QFN green package

Applications

- Access routers, edge routers, core routers
- Carrier Ethernet switches
- Multi-service access platforms
- PON OLT
- LTE eNodeB
- ITU-T G.8264 Synchronous Equipment Timing Source (SETS)
- ITU-T G.8262 Synchronous Ethernet Equipment Clock (EEC)
- ITU-T G.813 Synchronous Equipment Clock (SEC)
- Telcordia GR-253-CORE/GR1244-CORE Stratum 3 Clock (S3) and SONET Minimum Clock (SMC)

Description

The 82P33714 Synchronous Equipment Timing Source (SETS) for Synchronous Ethernet (SyncE) provides tools to manage timing references, clock generation and timing paths for SyncE based clocks, per ITU-T G.8264 and ITU-T G.8262. 82P33714 meets the requirements of ITU-T G.8262 for synchronous Ethernet Equipment Clocks (EECs) and ITU-T G.813 for Synchronous Equipment Clocks (SEC). The device outputs low-jitter clocks that can directly synchronize Ethernet interfaces; as well as SONET/SDH and PDH interfaces.

The 82P33714 accepts four differential reference inputs and two single ended reference inputs that can operate at common GNSS, Ethernet, SONET/SDH and PDH frequencies that range from 1 Pulse Per Second (PPS) to 650 MHz. The references are continually monitored for loss of signal and for frequency offset per user programmed thresholds. All of the references are available to both Digital PLLs (DPLLs). The active reference for each DPLL is determined by forced selection or by automatic selection based on user programmed priorities and locking allowances and based on the reference monitors and LOS inputs.

The 82P33714 can accept a clock reference and an associated phase locked sync signal as a pair. DPLL1 can lock to the clock reference and align the frame sync and multi-frame sync outputs with the paired sync input. The device allows any of the differential or single ended reference inputs to be configured as sync inputs that can be associated with any of the other differential or single ended reference inputs. The input sync signals can have a frequency of 1 PPS, 2 kHz, 4 kHz or 8 kHz. This feature enables DPLL1 to phase align its frame sync and multi-frame sync outputs with a sync input without the need use a low bandwidth setting to lock directly to the sync input.

The DPLLs support three primary operating modes: Free-Run, Locked and Holdover. In Free-Run mode the DPLLs synthesize clocks based on the system clock alone. In Locked mode the DPLLs filter reference clock jitter with the selected bandwidth. In Locked mode, the long-term output frequency accuracy is the same as the long term frequency accuracy of the selected input reference. In Holdover mode, the DPLL uses frequency data acquired while in Locked mode to generate accurate frequencies when input references are not available.

DPLL1 also supports DCO mode. In DCO mode the DPLL control loop is opened and the DCO can be controlled by an IEEE 1588 clock recovery servo running on an external processor to synthesize IEEE 1588 clocks.

The 82P33714 requires a system clock for its reference monitors and other digital circuitry. The frequency accuracy of the system clock determines the frequency accuracy of the DPLLs in Free-Run mode. The frequency stability of the system clock determines the frequency stability of the DPLLs in Free-Run mode and in Holdover mode; and it affects the wander generation of the DPLLs in Locked mode.

When used with a suitable system clock, DPLL1 meets the frequency accuracy, pull-in, hold-in, pullout, noise generation, noise tolerance, transient response, and holdover performance requirements of the following applications: ITU-T G.8262/G.813 EEC/SEC options 1 and 2, Telcordia GR-1244 Stratum 3 (S3), Telcordia GR-253-CORE S3 and SONET Minimum Clock (SMC).

DPLL1 can be configured with a range of selectable filtering bandwidths from 0.09 mHz to 567 Hz. The 17 mHz bandwidth can be used to lock the DPLL directly to a 1 PPS reference. The 92 mHz bandwidth can be used for G.8262/G.813 Option 2, or Telcordia GR-253-CORE S3, or SMC applications. The bandwidths in the range 1.1 Hz to 8.9 Hz can be used for G.8262/G.813 Option 1 applications. The bandwidth of 1.1 Hz or 2.2 Hz can be used for Telcordia GR-1244-CORE S3 applications. Bandwidths above 10 Hz can be used in jitter attenuation and rate conversion applications.

DPLL2 is a wideband (BW > 25Hz) frequency translator that can be used, for example, to convert a recovered line clock to a 1.544 MHz or 2.048 MHz synchronization interface clock.

For SETS applications per ITU-T G.8264, DPLL1 is configured as an EEC/SEC to output clocks for the T0 reference point and DPLL2 is used to output clocks for the T4 reference point.

Clocks generated by DPLL1 can be passed through APLL1 or APLL2 which are LC based jitter attenuating Analog PLLs (APLLs). The output clocks generated by APLL1 and APLL2 are suitable for serial GbE and lower rate interfaces.

All 82P33714 control and status registers are accessed through an I2C slave, SPI or UART interface. For configuring the DPLLs, APLL1 and APLL2, the I2C master interface can automatically load a configuration from an external EEPROM after reset.

Block Diagram

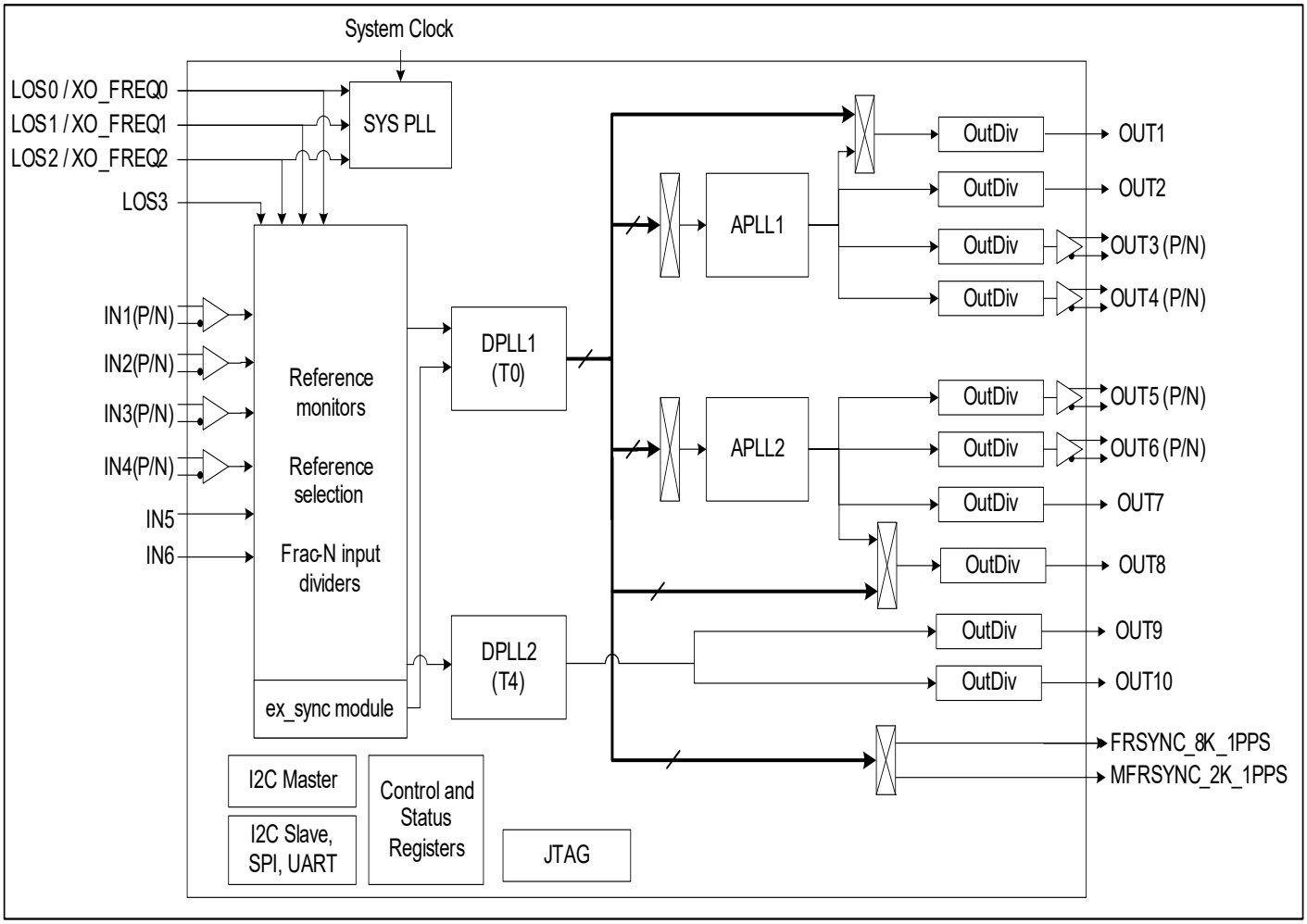


Figure 1. Functional Block Diagram

Contents

1 PIN ASSIGNMENT

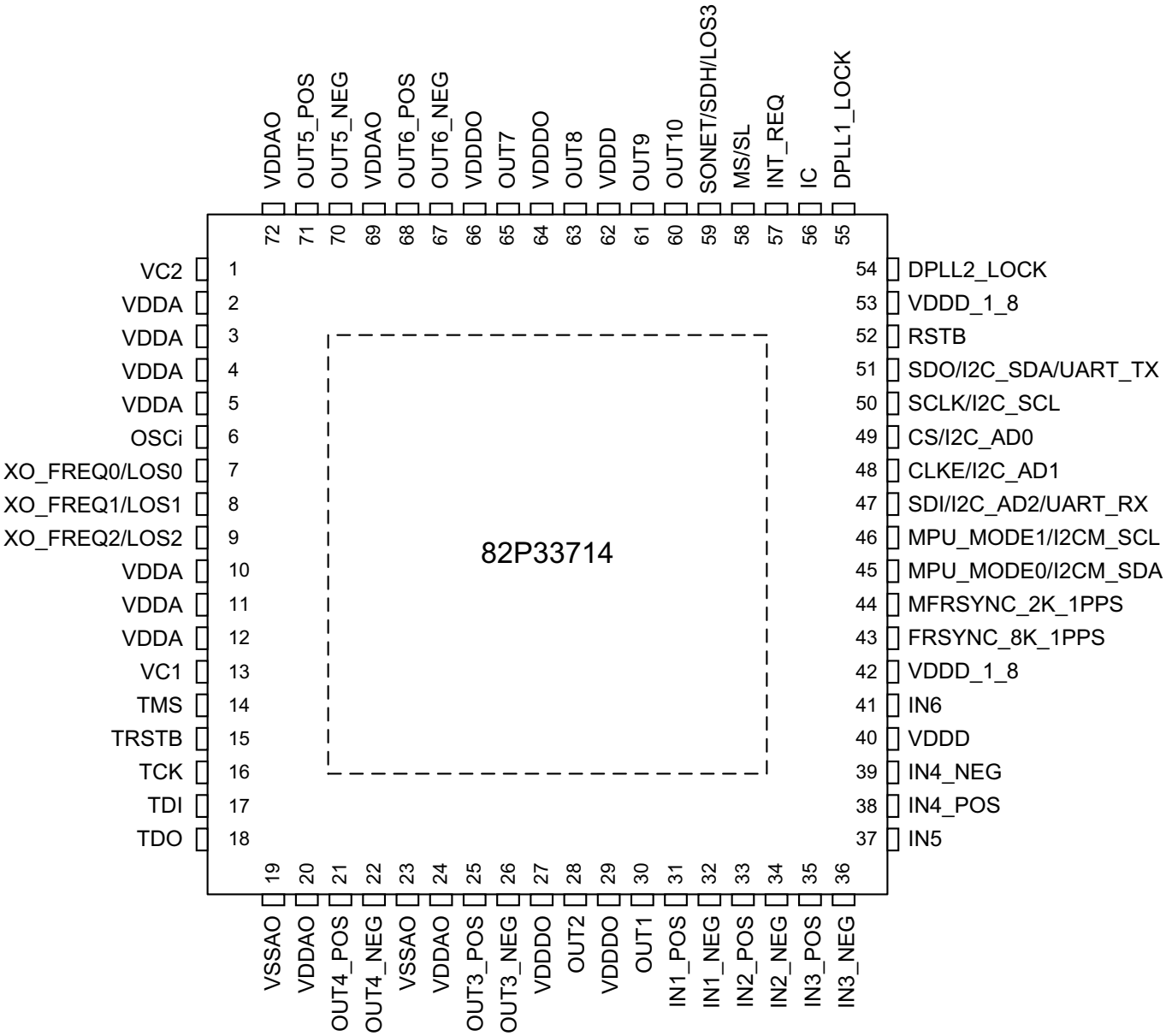


Figure 1. Pin Assignment (Top View)

2 PIN DESCRIPTION

Table 1: Pin Description

Pin No.	Name	I/O	Type	Description
Global Control Signal				
6	OSCI	I	CMOS	**OSCI: Crystal Oscillator System Clock** A clock provided by a crystal oscillator is input on this pin. It is the system clock for the device. The oscillator frequency is selected via pins XO_FREQ0 ~ XO_FREQ2
58	MS/SL	I pull-up	CMOS	**MS/SL: Master / Slave Selection** This pin, together with the MS_SL_CTRL bit, controls whether the device is configured as the Master or as the Slave. The signal level on this pin is reflected by the MASTER_SLAVE bit. MS_SL = 0: Slave MS_SL = 1: Master (default with internal pull-up)
59	SONET/SDH/ LOS3	I pull-down	CMOS	**SONET/SDH: SONET / SDH Frequency Selection** During reset, this pin determines the default value of the IN_SONET_SDH bit: High: The default value of the IN_SONET_SDH bit is '1' (SONET); Low: The default value of the IN_SONET_SDH bit is '0' (SDH). After reset, the value on this pin takes no effect. LOS3- This pin is used to disqualify input clocks. See input clocks section for more details.
52	RSTB	I pull-up	CMOS	**RSTB: Reset** Refer to section 2.2 reset operation for details.
7 8 9	XO_FREQ0/ LOS0 XO_FREQ1/ LOS1 XO_FREQ2/ LOS2	I pull-down	CMOS	**XO_FREQ0 ~ XO_FREQ2:** These pins set the oscillator frequency. XO_FREQ[2:0] Oscillator Frequency (MHz) 000 10.000 001 12.800 010 13.000 011 19.440 100 20.000 101 24.576 110 25.000 111 30.720 **LOS0 ~ LOS2 -** These pins are used to disqualify input clocks. See input clocks section for more details. After reset, this pin takes on the operation of LOS0-LOS2
Input Clock and Frame Synchronization Input Signal				
31 32	IN1_POS IN1_NEG	I	PECL/LVDS	**IN1_POS / IN1_NEG: Positive / Negative Input Clock 1** A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
33 34	IN2_POS IN2_NEG	I	PECL/LVDS	**IN2_POS / IN2_NEG: Positive / Negative Input Clock 1** A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
35 36	IN3_POS IN3_NEG	I	PECL/LVDS	**IN3_POS / IN3_NEG: Positive / Negative Input Clock 3** A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
38 39	IN4_POS IN4_NEG	I	PECL/LVDS	**IN4_POS / IN4_NEG: Positive / Negative Input Clock 4** A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
37	IN5	I pull-down	CMOS	**IN5: Input Clock 5** A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
41	IN6	I pull-down	CMOS	**IN6: Input Clock 6** A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.

Table 1: Pin Description (Continued)

Pin No.	Name	I/O	Type	Description
Output Frame Synchronization Signal				
43	FRSYNC _8K_1PPS	O	CMOS	**FRSYNC_8K_1PPS: 8 kHz Frame Sync Output** An 8 kHz signal or a 1PPS sync signal is output on this pin.
44	MFRSYNC _2K_1PPS	O	CMOS	**MFRSYNC_2K_1PPS: 2 kHz Multiframe Sync Output** A 2 kHz signal or a 1PPS sync signal is output on this pin.
Output Clock				
30 28	OUT1 OUT2	O	CMOS	**OUT1 ~ OUT2: Output Clock 1 ~ 2**
25 26	OUT3_POS OUT3_NEG	O	PECL/LVDS	**OUT3_POS / OUT3_NEG: Positive / Negative Output Clock 3** This output is set to LVDS by default.
21 22	OUT4_POS OUT4_NEG	O	PECL/LVDS	**OUT4_POS / OUT4_NEG: Positive / Negative Output Clock 4** This output is set to LVDS by default.
71 70	OUT5_POS OUT5_NEG	O	PECL/LVDS	**OUT5_POS / OUT5_NEG: Positive / Negative Output Clock 5** This output is set to LVDS by default.
68 67	OUT6_POS OUT6_NEG	O	PECL/LVDS	**OUT6_POS / OUT6_NEG: Positive / Negative Output Clock 6** This output is set to LVDS by default.
65 63	OUT7 OUT8	O	CMOS	**OUT7 ~ OUT8: Output Clock 7 ~ 8**
61 60	OUT9 OUT10	O	CMOS	**OUT9 ~ OUT10: Output Clock 9 ~ 10**
Miscellaneous				
13	VC1	O	Analog	**VC1: APLL1 VC Output** An external RC filter (a resistor in series with a capacitor to ground, and another capacitor in parallel) should be connected to this pin.
1	VC2	O	Analog	**VC2: APLL2 VC Output** An external RC filter (a resistor in series with a capacitor to ground, and another capacitor in parallel) should be connected to this pin.
Lock Signal				
54	DPLL2_LOCK	O	CMOS	DPLL2_LOCK This pin goes high when DPLL2 is locked
55	DPLL1_LOCK	O	CMOS	DPLL1_LOCK This pin goes high when DPLL1 is locked
Microprocessor Interface				
57	INT_REQ	O Tri-state	CMOS	**INT_REQ: Interrupt Request** This pin is used as an interrupt request.
46 45	MPU_MODE1/ I2CM_SCL MPU_MODE0/ I2CM_SDA	I/O pull-up	CMOS/ Open Drain	**MPU_MODE[1:0]: Microprocessor Interface Mode Selection** During reset, these pins determine the default value of the MPU_SEL_CNFG[1:0] bits as follows: 00: I2C mode 01: SPI mode 10: UART mode 11: I2C master (EEPROM) mode **I2CM_SCL: Serial Clock Line** In I2C master mode, the serial clock is output on this pin. **I2CM_SDA: Serial Data Input for I2C Master Mode** In I2C master mode, this pin is used as the for the serial data.

Table 1: Pin Description (Continued)

Pin No.	Name	I/O	Type	Description
47	SDI/I2C_AD2/ UART_RX	I pull-down	CMOS	**SDI: Serial Data Input** In Serial mode, this pin is used as the serial data input. Address and data on this pin are serially clocked into the device on the rising edge of SCLK. **I2C_AD2: Device Address Bit 2** In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface. **UART_RX** In UART mode, this pin is used as the receive data (UART Receive)
48	CLKE/I2C_AD1	I pull-down	CMOS	**CLKE: SCLK Active Edge Selection** In Serial mode, this pin is an input, it selects the active edge of SCLK to update the SDO: High - The falling edge; Low - The rising edge. **I2C_AD1: Device Address Bit 1** In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface.
49	CS/I2C_AD0	I pull-up	CMOS	**$\overline{CS}$: Chip Selection** In Serial modes, this pin is an input.A transition from high to low must occur on this pin for each read or write operation and this pin should remain low until the operation is over. **I2C_AD0: Device Address Bit 0** In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface.
50	SCLK/I2C_SCL	I pull-down	CMOS	**SCLK: Shift Clock** In Serial mode, a shift clock is input on this pin. Data on SDI is sampled by the device on the rising edge of SCLK. Data on SDO is updated on the active edge of SCLK. The active edge is determined by the CLKE. **I2C_SCL: Serial Clock Line** In I2C mode, the serial clock is input on this pin.
51	SDO/I2C_SDA/ UART_TX I2C_SDA	I/O pull-up	CMOS/ Open Drain	**SDO: Serial Data Output** In Serial mode, this pin is used as the serial data output. Data on this pin is serially clocked out of the device on the active edge of SCLK. **I2C_SDA: Serial Data Input/Output** In I2C mode, this pin is used as the input/output for the serial data. **UART_TX:** In UART mode, this pin is used as the transmit data (UART Transmit)
JTAG (per IEEE 1149.1)				
14	TMS	I pull-up	CMOS	**TMS: JTAG Test Mode Select** The signal on this pin controls the JTAG test performance and is sampled on the rising edge of TCK.
15	TRSTB	I pull-up	CMOS	**TRSTB: JTAG Test Reset (Active Low)** A low signal on this pin resets the JTAG test port. This pin should be connected to ground when JTAG is not used.
16	TCK	I pull-down	CMOS	**TCK: JTAG Test Clock** The clock for the JTAG test is input on this pin. TDI and TMS are sampled on the rising edge of TCK and TDO is updated on the falling edge of TCK. If TCK is idle at a low level, all stored-state devices contained in the test logic will indefinitely retain their state.
17	TDI	I pull-up	CMOS	**TDI: JTAG Test Data Input** The test data are input on this pin. They are clocked into the device on the rising edge of TCK.

Table 1: Pin Description (Continued)

Pin No.	Name	I/O	Type	Description
18	TDO	O tri-state	CMOS	**TDO: JTAG Test Data Output** The test data are output on this pin. They are clocked out of the device on the falling edge of TCK. TDO pin outputs a high impedance signal except during the process of data scanning.
Power & Ground				
2, 3, 4, 5, 10 11, 12	VDDA	Power	-	**VDDA**: Analog Core Power - +3.3V DC nominal
20, 24, 69, 72	VDDAO	Power		**VDDAO**: Analog Output Power - +3.3V DC nominal
27, 29, 64, 66	VDDDO	Power		**VDDDO**: Digital Output Power - +3.3V DC nominal
40, 62	VDDD	Power		**VDDD**: Digital Core Power - +3.3V DC nominal
42, 53	VDDD_1_8	Power		**VDDD_1_8**: Digital Core Power - +1.8V DC nominal
19,23	VSSAO	Ground		**VSSAO**: Ground
73 (e_PAD)	VSS	Ground	-	**VSS**: Ground
Other				
56	IC	-	-	**IC**: Internal Connection Internal Use. This pin must be left open for normal operation.

2.1 RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

2.1.1 INPUTS

Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Single-Ended Clock Inputs

For protection, unused single-ended clock inputs should be tied to ground.

Differential Clock Inputs

For applications not requiring the use of a differential input, both *_POS and *_NEG can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from _POS to ground.

2.1.2 OUTPUTS

Status Pins

For applications not requiring the use of a status pin, we recommend bringing out to a test point for debugging purposes.

Single-Ended Clock Outputs

All unused single-ended clock outputs can be left floating, or can be brought out to a test point for debugging purposes.

Differential Clock Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

2.2 RESET OPERATION

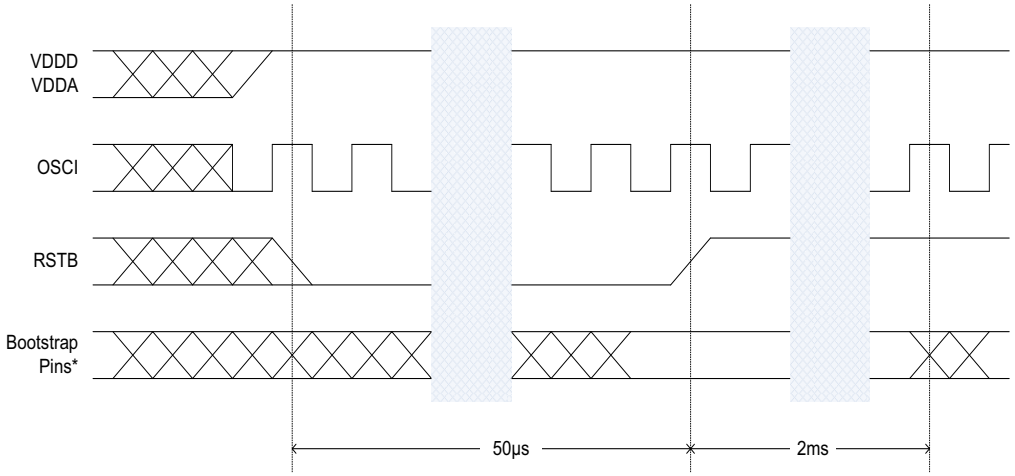
The device must be reset properly in order to ensure operations conform with specification.

To properly reset the device, the RSTB pin must be held at a low value for at least 50 usec. The device should be brought out of reset only at the time when power supplies are stabilized and the system clock is available on OSCi pin. The RSTB can be held low until this time, or pulsed low for at least 50us after this time.

The bootstrap pins (XO_FREQ[2:0], MPU_MODE[1:0], I2C_AD[2:0], MS/SL, SONET/SDH) need to be held at desired states for at least 2ms after de-assertion of RSTB pin to allow correct sampling. See Figure 3 for detail.

If loading from an EEPROM, the maximum time from RSTB de-assert to have stable clocks is 100ms. Note that if there is a bad EEPROM read sequence and the EEPROM loading is repeated once or twice (three times halts the device), then this time can be 2 or 3 times longer respectively. If not loading from EEPROM the maximum time from RSTB de-assert to have stable clocks is 10ms.

An on-board reset circuit or a commercially available voltage supervisory can be used to generate the reset signal. It is also feasible to use a standalone power-up RC reset circuit. When using a power-up RC reset circuit, careful consideration must be taken into account to fine tune the circuit properly based on each power supply's specification to ensure the power supply rise time is fast enough with respect to the RC time constant of the RC circuit.



* Bootstrap pins are: XO_FREQ[2:0], MPU_MODE[1:0], I2C_AD[2:0], MS/SL, SONET/SDH

Figure 2. Reset timing diagram

2.3 MS/SL PIN USAGE

The MS/SL pin is used for timing card redundancy applications where there is a primary and secondary timing card in the system. For other applications, this pin should be left unconnected or connected to an external pull-up.

For more information, see AN-901, *How to Implement Master/Slave for SETS and SMU Devices on Timing Redundancy Designs*.

3 FUNCTIONAL DESCRIPTION

3.1 SYNCHRONOUS ETHERNET, SONET, AND SDH ARCHITECTURE

82P33714 integrates key features that allows the device to be used in Synchronous Ethernet, SONET and SDH applications. There are several key synchronization standards that are important to meet for such a system, they are:

- ITU-T Recommendation G.8262, Timing characteristics of Synchronous Ethernet Equipment slave clock (EEC)
- ITU-T Recommendation G.8264, Distribution of timing through packet networks
- ITU-T Recommendation G.812, Timing requirements of slave clocks suitable for use as node clocks in synchronization networks.
- ITU-T Recommendation G.813, Timing characteristics of SDH equipment slave clocks (SEC).
- GR-253-CORE - Telcordia Technologies Generic Requirements - Issue 5, October 2009
- GR-1244-CORE - Telcordia Technologies Generic Requirements - Issue 4, October 2009
- ATIS-0900101.2006 - T1.101 - Synchronization Interface Standard

Figure 3 shows a single blade architecture that it is usually used in simple equipment.

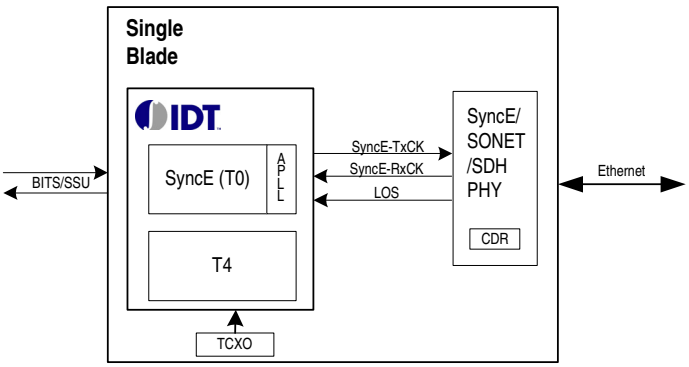


Figure 3. SyncE/SONET/SDH single blade application

Figure 4 shows an active/redundant architecture, as described before it is usually used in Telecom equipment that are designed to have a redundant timing card in case of primary timing card failure. The redundant timing card mimics the output of the active timing card, so in case of failure the system will still provide proper synchronization.

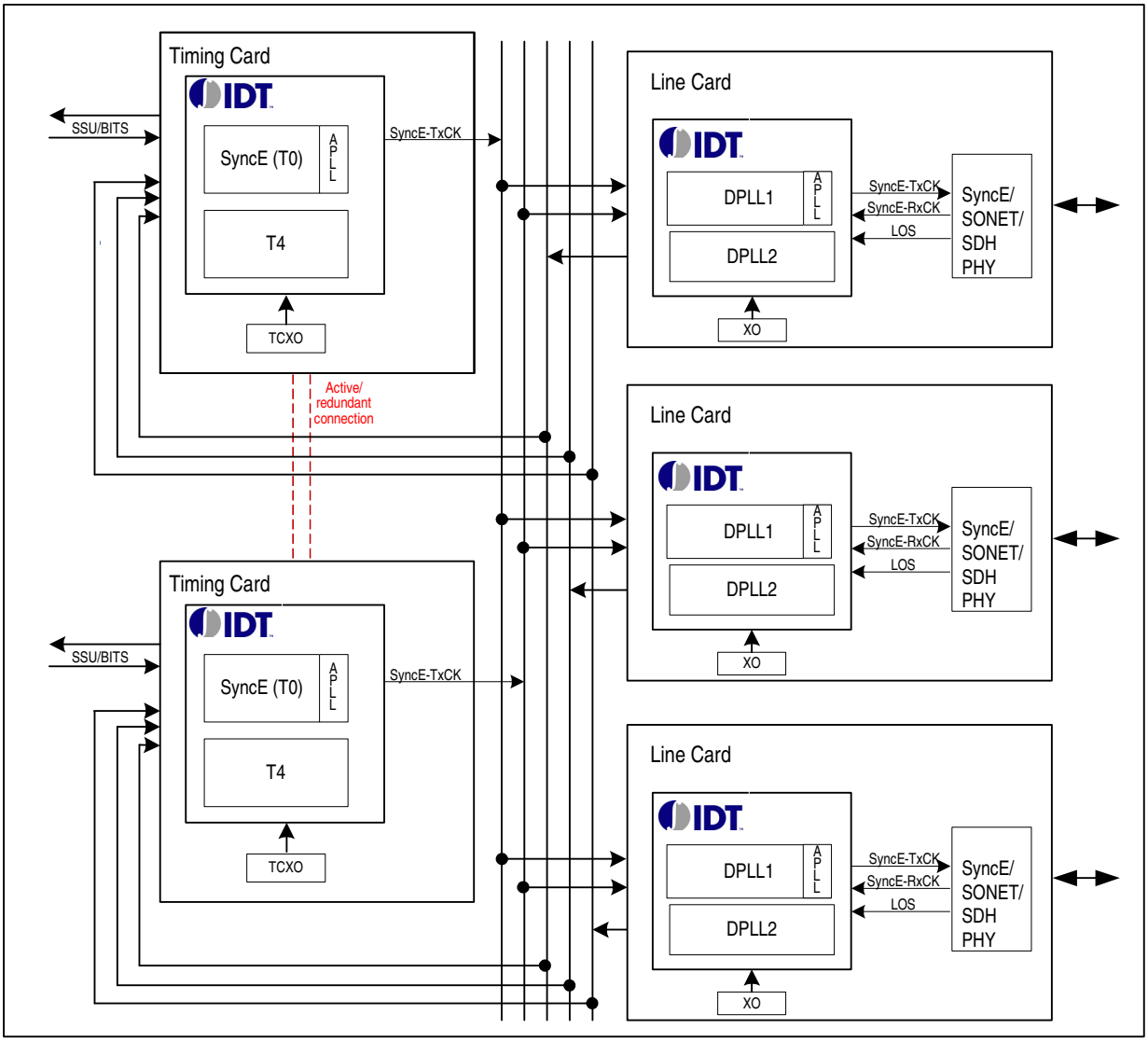


Figure 4. SyncE/SONET/SDH active/redundant application

3.2 HARDWARE FUNCTIONAL DESCRIPTION

3.2.1 SYSTEM CLOCK

A crystal oscillator should be used as an input on the OSCI pin. This clock is provided for the device as a system clock. The system clock is used as a reference clock for all the internal circuits. The active edge of the system clock can be selected by the OSC_EDGE bit in xo_freq_cnfg register.

Eight common oscillator frequencies can be used for the stable System Clock. The oscillator frequency can be set by pins or by xo_freq_cnfg register as shown in Table 2.

Table 2: Oscillator Frequencies

xo_freq[2:0] pins xo_freq_cnfg[2:0] bits	Oscillator Frequency (MHz)
000	10.000
001	12.800
010	13.000
011	19.440
100	20.000
101	24.576
110	25.000
111	30.720

An offset from the nominal frequency may be compensated by setting the NOMINAL_FREQ_VALUE[23:0] bits. The calibration range is within ±741 ppm.

The crystal oscillator should be chosen accordingly to meet different applications and standard requirements. (See AN-807 Recommended Crystal Oscillators for NetSynchro WAN PLL).

3.2.2 MODES OF OPERATION

3.2.2.1 DPLL1 Operating Mode

The DPLL1 can operate in several different modes as shown in Table 3.

The DPLL1 operating mode is controlled by the DPLL1_OPERATING_MODE[4:0] bits.

Table 3: DPLL1 Operating Mode Control

DPLL1_OPERATING_MODE[4:0]	DPLL1 Operating Mode
00000	Automatic
00001	Forced - Free-Run
00010	Forced - Holdover
00011	Reserved
00100	Forced - Locked
00101	Forced - Pre-Locked2
00110	Forced - Pre-Locked
00111	Forced - Lost-Phase
01000-01001	Reserved
01010	DCO write frequency see Chapter 3.2.2.1.6
10010 - 11111	Reserved
10011-11111	Reserved

When the operating mode is switched automatically, the operation of the internal state machine is shown in Figure 5.

Whether the operating mode is under external control or is switched automatically, the current operating mode is always indicated by the DPLL1_OPERATING_STS[4:0] bits. When the operating mode switches, the DPLL1_OPERATING_STS bit will be set. If the DPLL1_OPERATING_STS bit is ‘1’, an interrupt will be generated if the corresponding mask bit is set to “1”, the mask bit is set to “0” by default.

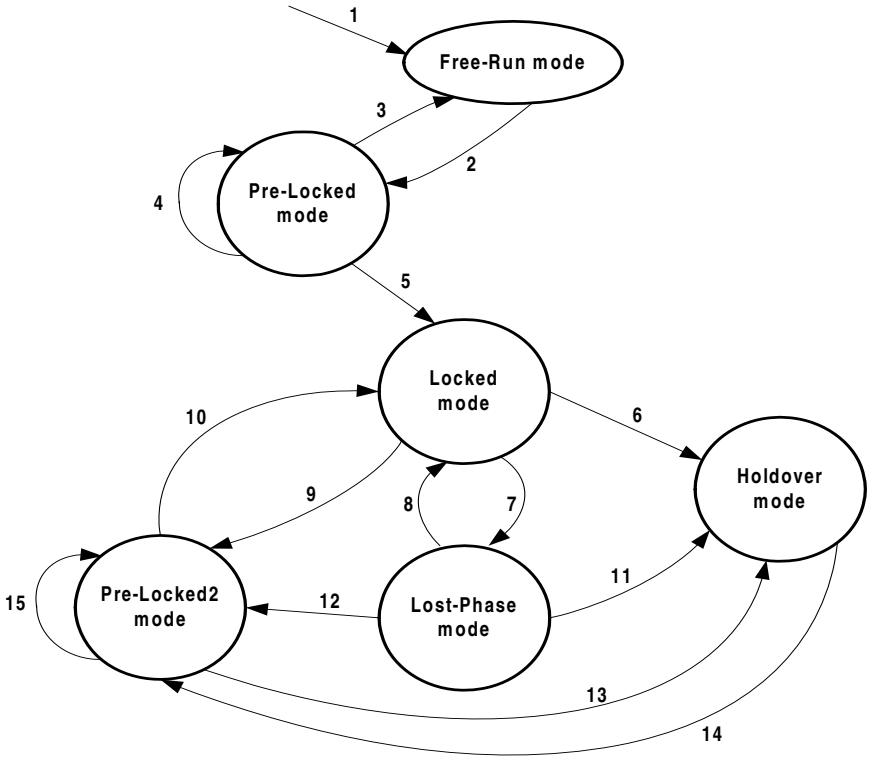


Figure 5. DPLL Automatic Operating Mode

Notes to Figure 5:

1. Reset.

2. An input clock is selected.

*3. The DPLL selected input clock is disqualified **AND** No qualified input clock is available.*

4. The DPLL selected input clock is switched to another one.

5. The DPLL selected input clock is locked (the DPLL_LOCK bit is '1').

*6. The DPLL selected input clock is disqualified **AND** No qualified input clock is available.*

7. The DPLL selected input clock is unlocked (the DPLL_LOCK bit is '0').

8. The DPLL selected input clock is locked again (the DPLL_LOCK bit is '1').

9. The DPLL selected input clock is switched to another one.

10. The DPLL selected input clock is locked (the DPLL_LOCK bit is '1').

*11. The DPLL selected input clock is disqualified **AND** No qualified input clock is available.*

12. The DPLL selected input clock is switched to another one.

*13. The DPLL selected input clock is disqualified **AND** No qualified input clock is available.*

14. An input clock is selected.

15. The DPLL selected input clock is switched to another one.

The causes of Item 4, 9, 12, 15 - 'the *DPLL* selected input clock is switched to another one' - are: (The *DPLL* selected input clock is disqualified **AND** Another input clock is switched to) **OR** (In Revertive switching, a qualified input clock with a higher priority is switched to) **OR** (The DPLL selected input clock is switched to another one Forced selection).

3.2.2.1.1 Free-Run Mode

In Free-Run mode, the DPLL1 output refers to the system clock and is not affected by any input clock. The accuracy of the DPLL1 output is equal to that of the system clock.

3.2.2.1.2 Pre-Locked Mode

In Pre-Locked mode, the DPLL1 output attempts to track the selected input clock.

The Pre-Locked mode is a secondary, temporary mode.

3.2.2.1.3 Locked Mode

In Locked mode, the DPLL1 is locked to the input clock. The phase and frequency offset of the DPLL1 output track those of the DPLL1 selected input clock.

For a closed loop, different bandwidths and damping factors can be used depending on DPLL locking stages: starting, acquisition and locked.

In the first two seconds when the DPLL1 attempts to lock to the selected input clock, the starting bandwidth and damping factor are used. They are set by the DPLL1_START_BW[4:0] bits and the DPLL1_START_DAMPING[2:0] bits respectively.

During the acquisition, the acquisition bandwidth and damping factor are used. They are set by the DPLL1_ACQ_BW[4:0] bits and the DPLL1_ACQ_DAMPING[2:0] bits respectively.

When the DPLL1 is locked, the locked bandwidth and damping factor are used. They are set by the DPLL1_LOCKED_BW[4:0] bits and the DPLL1_LOCKED_DAMPING[2:0] bits respectively.

The corresponding bandwidth and damping factor are used when the DPLL1 operates in different locking stages: starting, acquisition and locked, as controlled by the device automatically.

The locked bandwidth is selectable can be set as shown in Table 4.

Table 4: DPLL1 Locked Bandwidth

DPLL1_LOCKED_BW[4:0]	BW	Application
00000	0.090 mHz	
00001	0.27 mHz	
00010	0.90 mHz	stratum 3E, BW<1mHz
00011	2.9 mHz	G.812 Type I, BW< 3mHz
00100	4.3 mHz	
00101	8.7 mHz	
00110	17 mHz	
00111	35 mHz	
01000	69 mHz	
01001	92 mHz	GR-253 stratum 3, SMC and EEC-option, 2, BW ≤ 0.1Hz
01010	277 mHz	
01011	554 mHz	
01100	1.1 Hz	EEC-option 1, 1≤ BW ≤10 GR-1244 stratum 3, BW≤3Hz
01101	2.2 Hz	EEC-option 1, 1≤ BW ≤10 GR-1244 stratum 3, BW≤3Hz
01110	4.4 Hz	EEC-option 1, 1≤ BW ≤10
01111	8.9 Hz	EEC-option 1, 1≤ BW ≤10
10000	18 Hz	
10001	35 Hz	
10010	71 Hz	
10011	142 Hz	
10100	283 Hz	
10101	567 Hz	
10110-11111	Reserved	

3.2.2.1.4 Pre-Locked2 Mode

In Pre-Locked2 mode, the DPLL1 output attempts to track the selected input clock.

The Pre-Locked2 mode is a secondary, temporary mode.

3.2.2.1.5 Lost-Phase Mode

In Lost-Phase mode, the DPLL1 output attempts to track the selected input clock.

The Lost-Phase mode is a secondary, temporary mode.

3.2.2.1.6 DCO control modes

Figure 6 show a high level diagram of the DCO control architecture, it shows the DCO in DPLL1 being controlled. The DCO is a phase accumulator running at an internal clock. The DCO is controlled by a digital word that can represent phase offset or frequency offset. In the case of an IEEE 1588 application, the external processor will run the clock recovery servo algorithm and it will generate a frequency offset word to control the DCO.

The DCO control modes can be set by registers DPLL1_operating_mode_cnfg for DPLL1.

Figure 6 shows the DCO being controlled by writing a frequency offset word into the DCO, then by changing temporarily the DCO's frequency, the phase of the clock (or 1PPS) being generated by the DCO will also change. The output phase change is the product of the frequency change times the duration for which the frequency change is applied for. Because the DCO's frequency word has a very fine resolution, the output phase can be adjusted in very fine steps. In this case the clock recovery servo algorithm controls the bandwidth and phase slope limiting. The frequency offset word can be written into DPLL1_holdover_freq_cnfg[39:0] bits of frequency configuration registers for DPLL12. This value is 2's complement signed number. Total range is +/- 92 ppm, and the DCO programming resolution is [(77760 / 1638400) * 2^-48] or ~1.686305041e-10 ppm. The DCO resolution is affected by the offset applied into the DCO, so when writing into the DCO, the programming resolution is [(77760/1638400) * 2^-48] * (1 + offset-in-ppm / 1e6).

Controlling the DCO's frequency for smaller fine resolution phase changes is a good method, but for bigger phase changes it is better to use the snap-alignment method. The snap phase alignment is fast but only provides coarse adjustment. The 82P33714 allows for both the fine phase adjustment by controlling the frequency of the DCO and the coarse phase adjustment by snap-aligning the output clock (or 1PPS), for details, see section 3.2.7.3 Output Phase control on page 28.

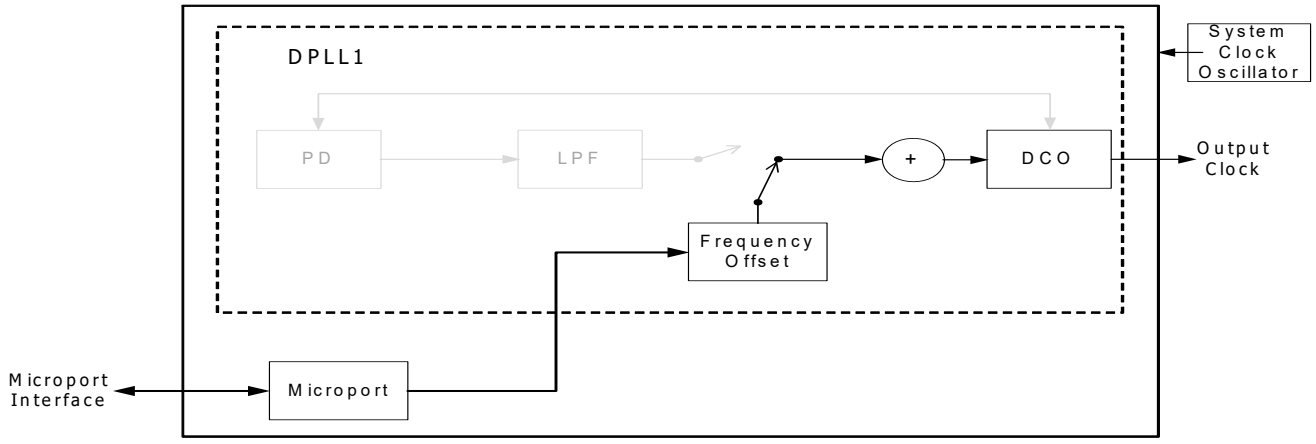


Figure 6. DCO frequency offset control functional block diagram

3.2.2.1.7 Holdover Mode

In Holdover mode, the DPLL1 resorts to the stored frequency data acquired in Locked mode to control its output. The DPLL1 output is not phase locked to any input clock. The frequency offset acquiring method is selected by the man_holdover bit, auto_avg bit, the hist_mode [1:0] bits, and the avg_mode[1:0] bits in DPLL1_holdover_mode_cnfg registers as shown in Table 5.

Table 5: Frequency Offset Control in Holdover Mode

man_holdover	auto_avg	hist_mode [1:0]		avg_mode[1:0]		Frequency Offset Acquiring Method
0	0	don't-care		don't-care		Averaged
	1	0	0	0	0	Current averaged value with holdover filter BW of ~0.18mHz
				0	1	Current averaged value with holdover filter BW of ~1.5mHz
				1	0	Current averaged value with holdover filter BW of ~12mHz
				1	1	Current averaged value with holdover filter BW of ~0.15Hz
		0	0	0	0	Averaged value 1 second before with holdover filter BW of ~0.18mHz
				0	1	Averaged value 1 second before with holdover filter BW of ~1.5mHz
				1	0	Averaged value 1 second before with holdover filter BW of ~12mHz
				1	1	Averaged value 1 second before with holdover filter BW of ~0.15Hz
		0	1	0	0	Averaged value 8 seconds before with holdover filter BW of ~0.18mHz
				0	1	Averaged value 8 seconds before with holdover filter BW of ~1.5mHz
				1	0	Averaged value 8 seconds before with holdover filter BW of ~12mHz
				1	1	Averaged value 8 seconds before with holdover filter BW of ~0.15Hz
		1	0	0	0	Averaged value 64 seconds before with holdover filter BW of ~0.18mHz
				0	1	Averaged value 64 seconds before with holdover filter BW of ~1.5mHz
				1	0	Averaged value 64 seconds before with holdover filter BW of ~12mHz
				1	1	Averaged value 64 seconds before with holdover filter BW of ~0.15Hz
1	don't-care					Manual - values is set by DPLL1_holdover_freq_cnfg register

The default value for holdover mode is set to current averaged value with holdover filter BW of ~1.5mHz. In this mode the initial frequency offset is better than 1.1e-5ppm assuming that there is no in-band jitter/wander at the input just before entering holdover state. The default mode is used for Telcordia GR-1244, Telcordia GR-253, ITU-T G.8262 and ITU-T G.813 to meet holdover requirements.

In Manual Mode, the frequency offset is set by the DPLL1_holdover_freq_cnfg[39:0] bits. The accuracy is1.686305041e-10 ppm, however the resolution is affected by the frequency offset applied, so when writing the frequency offset, the programming resolution is [(77760/1638400) * 2^-48] * (1 + offset-in-ppm / 1e6).

The offset value, which is acquired by the modes shown in Table 5, can be read from the holdover_freq_cnfg[39:0] bits by setting the read_avg bit to "1". If read_avg bit is set to "0" then the value in holdover_freq_cnfg[39:0] bits is the value written into it. The value is 2's complement signed number, and the total range is +/- 92 ppm.

The holdover frequency resolution is calculated as follows:

Holdover Frequency resolution: HO_freq_res = (77760/1638400) * 2^-48

The Holdover value read from register bits holdover_freq_cnfg[[39:0] must be converted to decimal:

HO_value_dec = holdover_freq_cnfg[39:0] value in decimal

The frequency offset in ppm is calculated as follows:

Holdover Frequency Offset (ppm) = (HO_freq_res * HO_value_dec)/(1-((HO_freq_res * HO_value_dec)/1e6))

3.2.2.1.8 Hitless Reference Switching

Bit hitless_switch_en in DPLL1_mon_sw_pbo_cnfg register can be used to set hitless reference switching. When a Hitless Switching (HS) event is triggered, the phase offset of the selected input clock with respect to the DPLL1 output is measured. The device then automatically accounts for the measured phase offset and compensates for the appropriate phase offset into the DPLL output so that the phase transients on the DPLL1 output are minimized. The input frequencies should be set to frequencies equal to 8 kHz or higher.

If hitless_switch_en is set to "1", a HS event is triggered if any one of the following conditions occurs:

- DPLL1 selected input clock switches to a different reference
- DPLL1 exits from Holdover mode or Free-Run mode

For the two conditions, the phase transients on the DPLL1 output are minimized to be no more than 0.61 ns with HS. The HS can also be frozen at the current phase offset by setting the hitless_switch_freeze bit in DPLL1_mon_sw_pbo_cnfg register. When the HS is frozen, the device will ignore any further HS events triggered by the above two conditions, and maintain the current phase offset.

When the HS is disabled, there may be a phase shift on the DPLL1 output, as the DPLL1 output tracks back to 0 degree phase offset with respect to the DPLL1 selected input clock. This phase shift can be limited; see section 3.2.2.1.9 Phase Slope Limit.

3.2.2.1.9 Phase Slope Limit

To meet the phase slope requirements of Telcordia and new ITU-T standards, both DPLL1 provides a phase slope limiting feature to limit the rate of output phase movement. The limit level is selectable via DPLL1_ph_limit[2:0] bits in DPLL1_bw_overshoot_cnfg register. The options are shown in Table 6.

Table 6: DPLL1 Phase Slope Limit

DPLL1_ph_limit[2:0]	Phase Slope Limit
000	61µs/s (GR-1244 ST3)
001	885ns/s (GR-1244-CORE ST2 and 3E, GR-253-CORE ST3 and G.8262 EEC option 2)
010	7.5 µs/s (G.813 opt1, G.8262 EEC-option 1)
011	unlimited / 1.4 ms/s (default)
100	1 ns/s
101	5 ns/s
110	10 ns/s
111	programmable (default)*
*Note: The default phase slope limiting is set to programmable with a default value set to 0 ns/s, therefore the phase slope limiting must be set to the proper value to meet different standards according to this table.	

The programmable phase slope limiting can be set by writing into registers DPLL1_prog_ph_limit_cnfg[23:0]. The range of the programmable limit is 1484.3614 us/s.

3.2.2.1.10 Frequency Offset Limit

The DPLL1 output is limited to be within the programmed DPLL hard limit (refer to Chapter 3.2.4.3).

3.2.2.2 DPLL2 Operating Mode

The DPLL2 operating mode is controlled by the DPLL2_OPERATING_MODE[2:0] bits, as shown in Table 7. DPLL2 is disabled by default, write “0” to bit DPLL2_pdn in pdn_conf register to enable it.

Table 7: DPLL2 Operating Mode Control

DPLL2_OPERATING_MODE[2:0]	DPLL2 Operating Mode
000	Automatic
001	Forced - Free-Run
010	Forced - Holdover
100	Forced - Locked

When the operating mode is switched automatically, the operation of the internal state machine is shown in Figure 7:

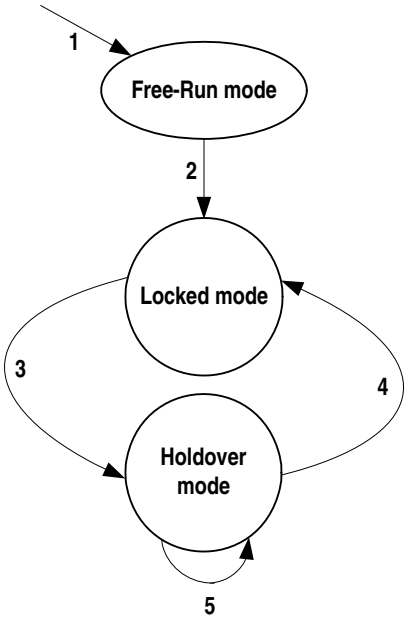


Figure 7. DPLL2 Automatic Operating Mode

Notes to Figure 7:

1. *Reset.*
2. *An input clock is selected.*
3. *(The* DPLL2 *selected input clock is disqualified)* ***OR*** *(A qualified input clock with a higher priority is switched to)* ***OR*** *(The* DPLL2 *selected input clock is switched to another one by Forced selection).*
4. *An input clock is selected.*
5. *No input clock is selected.*

3.2.2.2.1 Free-Run Mode

In Free-Run mode, the DPLL2 output refers to the system clock and is not affected by any input clock. The accuracy of the DPLL2 output is equal to that of the system clock.

3.2.2.2.2 Locked Mode

In Locked mode, the DPLL2 is locked to the input clock. The phase and frequency offset of the DPLL2 output track those of the DPLL2 selected input clock.

DPLL2 is a wide BW DPLL, with loop bandwidth higher than 25Hz.

3.2.2.2.3 Holdover Mode

In Holdover mode, the DPLL2 has 2 modes of operation for the holdover set by DPLL2_auto_avg bit in DPLL2_holdover_mode_cnfg register.

DPLL2_auto_avg = 0: holdover frequency is the instantaneous value of integral path just before entering holdover. If the DPLL2 was locked to an input clock reference that has no in-band jitter/wander and was then manually set to go into holdover, the initial frequency accuracy is 4.4X10-8 ppm.

DPLL2_auto_avg = 1: averaged frequency value is used as holdover frequency. The holdover average bandwidth is about 1.5mHz. In this mode the initial frequency offset is 1.1e-5ppm assuming that there is no in-band jitter/wander at the input just before entering holdover state.

3.2.2.2.4 Frequency Offset Limit

The DPLL2 output is limited to be within the DPLL hard limit (refer to Chapter 3.2.4.3).

3.2.3 INPUT CLOCKS AND FRAME SYNC

The 82P33714 has 6 input clocks that can also be used for frame sync pulses.

The 82P33714 supports Telecom and Ethernet frequencies from 1PPS up to 650 MHz.

Any of the input clocks can be used as a frame pulse or sync signal. The SYNC_sel[3:0] bits in IN*n*_los_sync_cnfg ($1 \leq n \leq 6$) registers sets which pin is used as frame pulse or sync signal.

IN1 to IN6 can be used for 2 kHz, 4 kHz or 8 kHz frame pulses or 1PPS sync signal.The input frequency should match the setting in the sync_freq[1:0] bits in DPLL1_input_mode_cnfg register.

3.2.3.1 Input Clock Pre-divider

Each input clock is assigned an internal Pre-divider. The Pre-divider can be used to divide the clock frequency down to a convenient frequency, such as 8 kHz for the internal DPLL1. Note that T1 and E1 references can exhibit substantial jitter with frequencies above 4 kHz. These references should be applied to DPLL1 without being divided down to 8kHz.

For IN1 ~ IN6, the DPLL required frequency is set by the corresponding IN_FREQ[3:0] bits.

Table 8: IN_FREQ[3:0] DPLL Frequency

IN_FREQ[3:0] Bits	DPLL Frequency
0000	8 kHz
0001	1.544 MHz / 2.048 MHz (depends on SONET/ SDH bit)
0010	6.48 MHz
0011–1000	Reserved
1001	2 kHz
1010	4 kHz
1011	1 PPS
1100	6.25 MHz
1101–1111	Reserved

Each Pre-divider consists of an FEC divider and a DivN divider,. IN1~IN4 also include an HF (High Frequency) divider. Figure 8 shows a block diagram of the pre-dividers for an input clock.

For 1 PPS, 2 kHz, 4 kHz or 8 kHz input clock frequency only, the Pre-divider should be bypassed by setting INn_DIV[1:0] bits = “0” ($1 \leq n \leq 4$), DIRECT_DIV bit = “0”, and LOCK_8K bit = “0”. The corresponding IN_FREQ[3:0] bits should be set to match the input frequency.

The HF divider, which is available for IN1 ~ IN4, should be used when the input clock is higher than (>) 162.5 MHz. The input clock can be divided by 4, 5 or can bypass the HF divider, as determined by the INn_DIV[1:0] bits ($1 \leq n \leq 4$).

The DivN divider can be bypassed, as determined by the DIRECT_DIV bit and the LOCK_8K bit. When DivN divider is bypassed, the corresponding IN_FREQ[3:0] bits should be set to match the input frequency. DIVN must be bypassed on a reference clock input that is also associated with another reference input used as SYNC.

When the DivN divider is used for INn ($1 \leq n \leq 6$), the division factor setting should observe the following order:

1. *Write the lower eight bits of the division factor to the PRE_DIVN_VALUE[7:0] bits;*
2. *Write the higher eight bits of the division factor to the PRE_DIVN_VALUE[14:8] bits.*

The division factor is calculated as follows:

Division Factor = (the frequency of the clock input to the DivN divider ÷ the frequency of the DPLL required clock set by the IN_FREQ[3:0] bits) - 1

The Pre-divider configuration and the division factor setting depend on the input clock on one of the IN1 ~ IN6 pins and the DPLL required clock.

For the fractional input divider, the FEC divider, each input clock has a 16-bit (fec_divp_cnfg[15:0]) that represents the value of the numerator and a 16-bit (fec_divq_cnfg[15:0]) that represents the value of the

denominator of FEC divider. The FEC division factor is calculated as follows:

FEC Division Factor = (fec_divp_cnfg[15:0]) ÷ (fec_divq_cnfg[15:0])

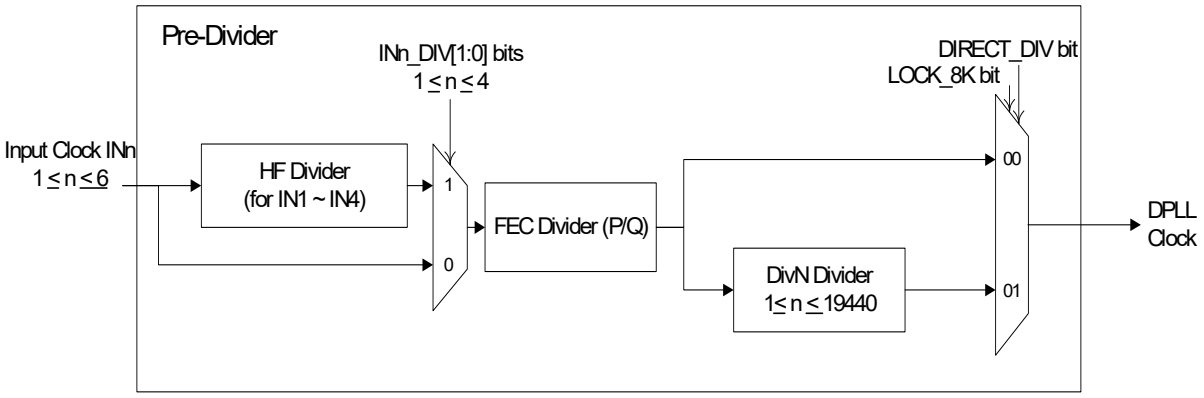


Figure 8. Pre-divider for an input clock

3.2.3.2 Input Clock Quality Monitoring

The qualities of all the input clocks are always monitored in the following aspects:

- Activity
- Frequency

Activity and frequency monitoring are conducted on all the input clocks.

The qualified clocks are available for selection for the 2 DPLLs.

3.2.3.2.1 Activity Monitoring

Activity is monitored by using an internal leaky bucket accumulator, as shown in Figure 9.

Each input clock is assigned an internal leaky bucket accumulator. The input clock is monitored for each period of 128 ms, the internal leaky bucket accumulator is increased by 1 when an event is detected; and it is decreased by 1 when no event is detected within the period set by the decay rate. The event is that an input clock drifts outside (>) ±500 ppm with respect to the system clock within a 128 ms period.

There are four configurations (0 - 3) for a leaky bucket accumulator. The leaky bucket configuration for an input clock is selected by the corresponding BUCKET_SEL[1:0] bits. Each leaky bucket configuration consists of four elements: upper threshold, lower threshold, bucket size and decay rate.

The bucket size is the capability of the accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected. The upper threshold is a point above which a no-activity alarm is raised. The lower threshold is a point below which the no-activity alarm is cleared. The decay rate is a certain period during which the accumulator decreases by 1 if no event is detected.

The leaky bucket configuration is programmed by one of four groups of register bits: the BUCKET_SIZE_n_DATA[7:0] bits, the UPPER_THRESHOLD_n_DATA[7:0] bits, the LOWER_THRESHOLD_n_DATA[7:0] bits and the DECAY_RATE_n_DATA[1:0] bits respectively; ‘n’ is 0 ~ 3.

The no-activity alarm status of the input clock is indicated by the INn_NO_ACTIVITY_ALARM bit ($6 \geq n \geq 1$).

The input clock with a no-activity alarm is disqualified for clock selection for the DPLLs.

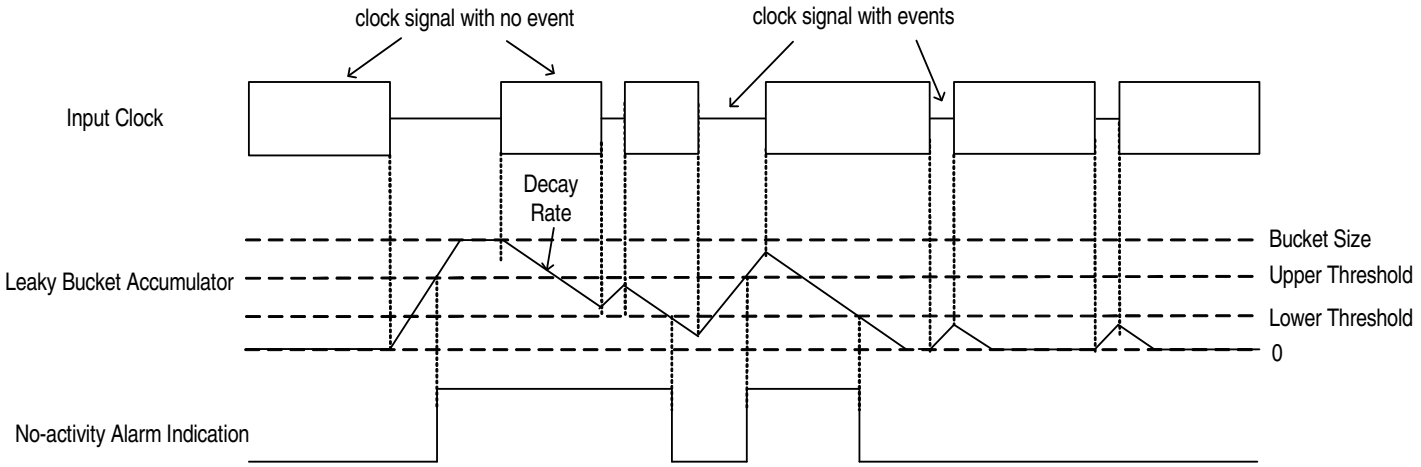


Figure 9. Input Clock Activity Monitoring

3.2.3.2.2 Frequency Monitoring

Frequency is monitored by comparing the input clock with a reference clock. The reference clock can be derived from the system clock or the output of DPLL1, as determined by the FREQ_MON_CLK bit.

Each reference clock has a hard frequency monitor and a soft frequency monitor. Both monitors have two thresholds, rejecting threshold and accepting threshold, which are set in HARD_FREQ_MON_-THRESHOLD[7:0] and SOFT_FREQ_MON_THRESHOLD[7:0]. So four frequency alarm thresholds are set for frequency monitoring: Hard Alarm Accepting Threshold, Hard Alarm Rejecting Threshold, Soft Alarm Accepting Threshold and Soft Alarm Rejecting Threshold.

The frequency hard alarm accepting threshold can be calculated as follows:

Frequency Hard Alarm Accepting Threshold (ppm) = (HARD_FREQ_MON_THRESHOLD[7:4] + 1) X FREQ_MON_FACTOR[3:0] (b3~0, FREQ_MON_FACTOR_CNFG)

The frequency hard alarm rejecting threshold can be calculated as follows:

Frequency Hard Alarm Rejecting Threshold (ppm) = (HARD_FREQ_MON_THRESHOLD[3:0] + 1) X FREQ_MON_FACTOR[3:0] (b3~0, FREQ_MON_FACTOR_CNFG)

When the input clock frequency rises to above the hard alarm rejecting threshold, the INn_FREQ_HARD_ALARM bit ($6 \geq n \geq 1$) will alarm and indicate '1'. The alarm will remain until the frequency is down to below the hard alarm accepting threshold, then the INn_FREQ_HARD_ALARM bit will return to '0'. There is a hysteresis between frequency monitoring, refer to Figure 10.

The soft alarm is indicated by the INn_FREQ_SOFT_ALARM bit ($6 \geq n \geq 1$) in the same way as hard alarm.

The input clock with a frequency hard alarm is disqualified for clock selection for the DPLLs, but the soft alarm doesn't affect the clock selection for the DPLLs.

The frequency of each input clock with respect to the reference clock can be read by doing the following step:

1. *Read the value in the IN_FREQ_VALUE[7:0] bits and calculate as follows:*

   Input Clock Frequency (ppm) = IN_FREQ_VALUE[7:0] * FREQ_MON_FACTOR[3:0]

Note that the value set by the FREQ_MON_FACTOR[3:0] bits depends on the application.

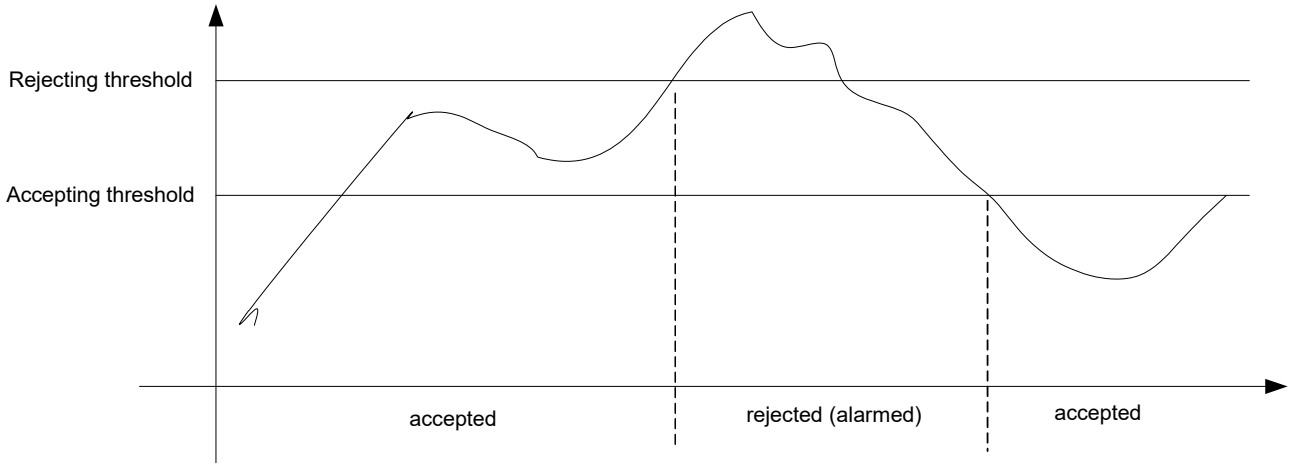


Figure 10. Hysteresis Frequency Monitoring

3.2.3.3 Input Clock Selection

For DPLL1 and DPLL2, the DPLL1/2_INPUT_SEL[3:0] bits (register DPLL1/2_input_sel_cnfg) determine the input clock selection, as shown in Table 9:

Table 9: Input Clock Selection for DPLL1 and DPLL2

DPLL1/2 _INPUT_SEL[3:0]	Input Clock Selection
0000	Automatic selection
0001 ~ 0010	Reserved
0011 ~ 0110	Forced selection (IN1 ~ IN4)
0111 ~ 1000	Reserved
1001 ~ 1010	Forced selection (IN5 ~ IN6)
1011 ~ 1111	Reserved

3.2.3.3.1 Forced Selection

In Forced selection, the selected input clock is set by the DPLL1_INPUT_SEL[3:0] and DPLL2_INPUT_SEL[4:0] bits. The results of input clocks quality monitoring do not affect the input clock selection if Forced selection is used.

3.2.3.3.2 Automatic Selection

In Automatic selection, the input clock selection is determined by input clock being valid, priority and input clock configuration. The input clock is declared valid depending on the results of input clock quality monitoring (refer to Chapter 3.2.3.2). The input clock can be configured to be valid and therefore be allowed to participate in the locking process by setting to “0” the corresponding INn_VALID bit ($6 \geq n \geq 1$) in DPLL_remote_input_valid_cnfg register, by default all the inputs are not valid, and therefore the user must set the corresponding bit to “0” in order to allow the DPLL to lock to a particular input clock. Within all the qualified input clocks, the one with the highest priority is selected. The priority is set by the corresponding INn_SEL_PRIORITY[3:0] bits in DPLL_INn_sel_priority_cnfg ($6 \geq n \geq 1$). If more than one qualified input clock INn is available, then it is important to set appropriate priorities to the input clocks, two input clocks must not have the same priority. This process is shown in Figure 11.

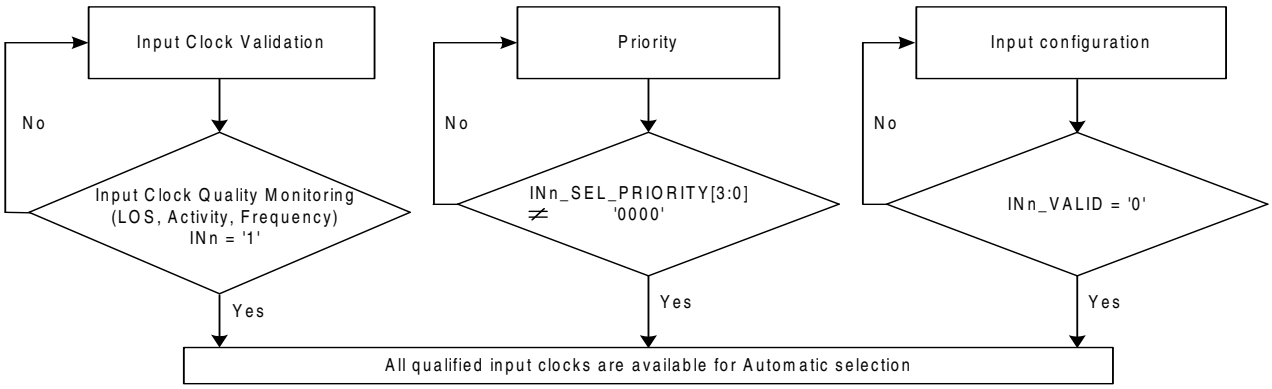


Figure 11. Qualified Input Clocks for Automatic Selection

3.2.3.3.2.1 Input Clock Validation

For all the input clocks, the input is declared valid depending on the results of input clock quality monitoring (refer to Chapter 3.2.3.2). The IN_NOISE_WINDOW bit should be set to ‘1’ if any of INn_FREQ[3:0] is set for frequencies ≤ 8 kHz, by default it is set to ‘0’.

For DPLL1, the following conditions must be satisfied for the input clock to be valid; otherwise, it is invalid.

- No no-activity alarm (the INn_NO_ACTIVITY_ALARM bit is ‘0’);
- No frequency hard alarm (the INn_FREQ_HARD_ALARM bit is ‘0’);
- No phase lock alarm, i.e., the INn_PH_LOCK_ALARM bit is ‘0’;
- If the ULTR_FAST_SW bit is ‘1’, the DPLL selected input clock misses less than (<) 2 consecutive clock cycles; if the ULTR_FAST_SW bit is ‘0’, this condition is ignored;
- LOS[3:0] are not set to disqualify the input clock

For DPLL2, the following conditions must be satisfied for the input clock to be valid; otherwise, it is invalid.

- No no-activity alarm (the INn_NO_ACTIVITY_ALARM bit is ‘0’);
- No frequency hard alarm (the INn_FREQ_HARD_ALARM bit is ‘0’);
- LOS[3:0] are not set to disqualify the input clock

The INn bit ($6 \geq n \geq 1$) indicates whether or not the clock is valid. When the input clock changes from ‘valid’ to ‘invalid’, or from ‘invalid’ to ‘valid), the INn bit will be set. If the INn bit is ‘1’, an interrupt will be generated.

When the DPLL selected input clock has failed, i.e., the selected input clock changes from ‘valid’ to ‘invalid’, the DPLL_MAIN_REF_FAILED bit will be set. If the DPLL_MAIN_REF_FAILED bit is ‘1’, an interrupt will be generated.