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DUAL CHANNEL E1 SHORT HAUL LINE INTERFACE UNIT

IDT82V2052E

FEATURES:

- **Dual channel E1 short haul line interfaces**
- **Supports HPS (Hitless Protection Switching) for 1+1 protection without external relays**
- **Single 3.3 V power supply with 5 V tolerance on digital interfaces**
- **Meets or exceeds specifications in**
  - ANSI T1.102
  - ITU I.431, G.703, G.736, G.775 and G.823
  - ETSI 300-166, 300-233 and TBR12/13
- **Software programmable or hardware selectable on:**
  - Wave-shaping templates
  - Line terminating impedance (E1: 75 Ω/120 Ω)
  - Adjustment of arbitrary pulse shape
  - JA (Jitter Attenuator) position (receive path or transmit path)
  - Single rail/dual rail system interfaces
  - HDB3/AMI line encoding/decoding
  - Active edge of transmit clock (TCLK) and receive clock (RCLK)
  - Active level of transmit data (TDATA) and receive data (RDATA)
  - Receiver or transmitter power down
  - High impedance setting for line drivers
  - PRBS (Pseudo Random Bit Sequence) generation and detection with 2^{15}-1 PRBS polynomials
  - 16-bit BPV (Bipolar Pulse Violation) / Excess Zero/ PRBS error counter
  - Analog loopback, Digital loopback, Remote loopback
- **Adaptive receive sensitivity up to -20 dB (Host Mode only)**
- **Non-intrusive monitoring per ITU G.772 specification**
- **Short circuit protection and internal protection diode for line drivers**
- **LOS (Loss Of Signal) detection with programmable LOS levels (Host Mode only)**
- **AIS (Alarm Indication Signal) detection**
- **JTAG interface**
- **Supports serial control interface, Motorola and Intel Non-Multiplexed interfaces and hardware control mode**
- **Pin compatible to 82V2082 T1/E1/J1 Long Haul/Short Haul LIU and 82V2042E T1/E1/J1 Short Haul LIU**
- **Available in 80-pin TQFP**
  Green package options available

DESCRIPTION:

The IDT82V2052E is a dual channel E1 Line Interface Unit. The IDT82V2052E performs clock/data recovery, AMI/HDB3 line decoding and detects and reports the LOS conditions. An integrated Adaptive Equalizer is available to increase the receive sensitivity and enable programming of LOS levels. In transmit path, there is an AMI/HDB3 encoder and Waveform Shaper. There is one Jitter Attenuator, which can be placed in either the receive path or the transmit path. The Jitter Attenuator can also be disabled. The IDT82V2052E supports both Single Rail and Dual Rail system interfaces. To facilitate the network maintenance, a PRBS generation/detection circuit is integrated in the chip, and different types of loopbacks can be set according to the applications. Two different kinds of line terminating impedance, 75 Ω and 120 Ω are selectable on a per channel basis. The chip also provides driver short-circuit protection and internal protection diode and supports JTAG boundary scanning. The chip can be controlled by either software or hardware.

The IDT82V2052E can be used in LAN, WAN, Routers, Wireless Base Stations, IADs, IMAs, IMAPs, Gateways, Frame Relay Access Devices, CSU/DSU equipment, etc.

FUNCTIONAL BLOCK DIAGRAM

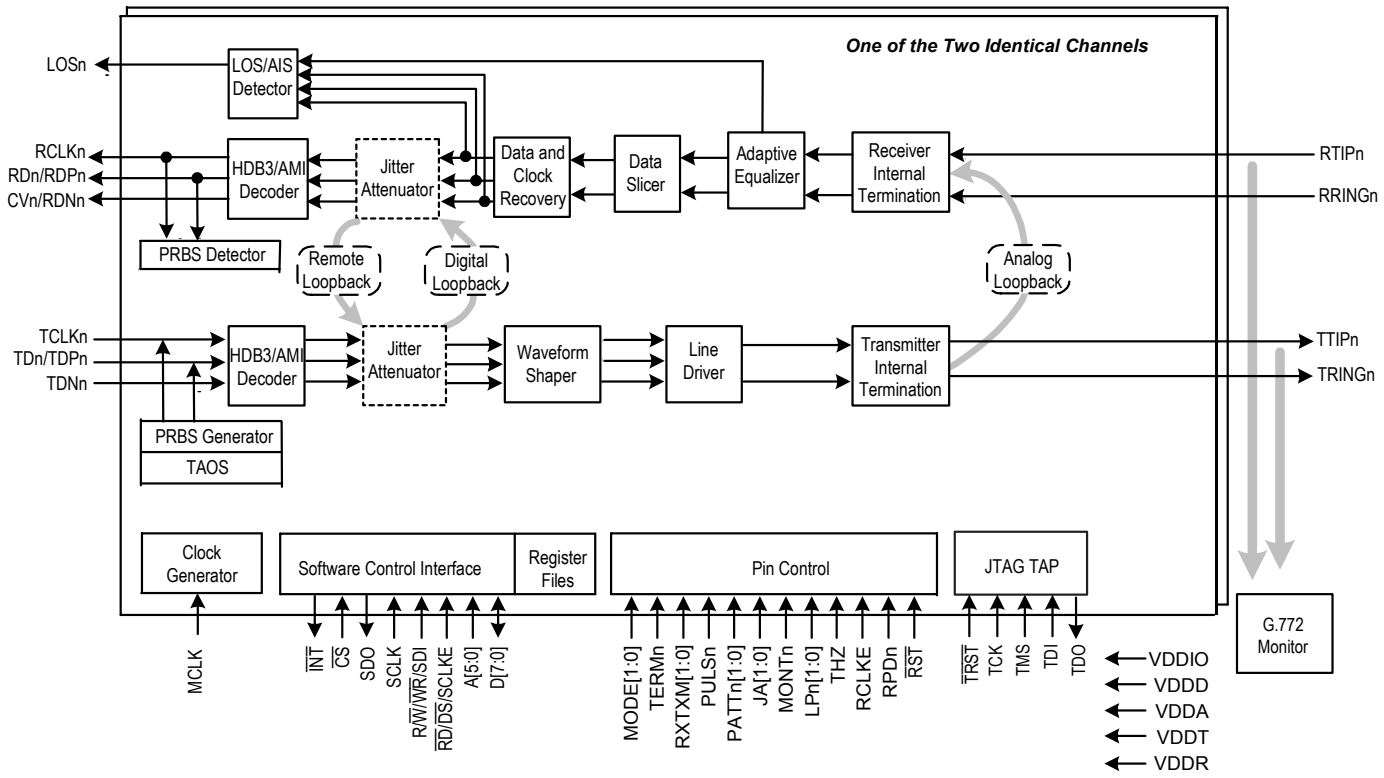

Figure-1 Block Diagram

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1 IDT82V2052E PIN CONFIGURATIONS

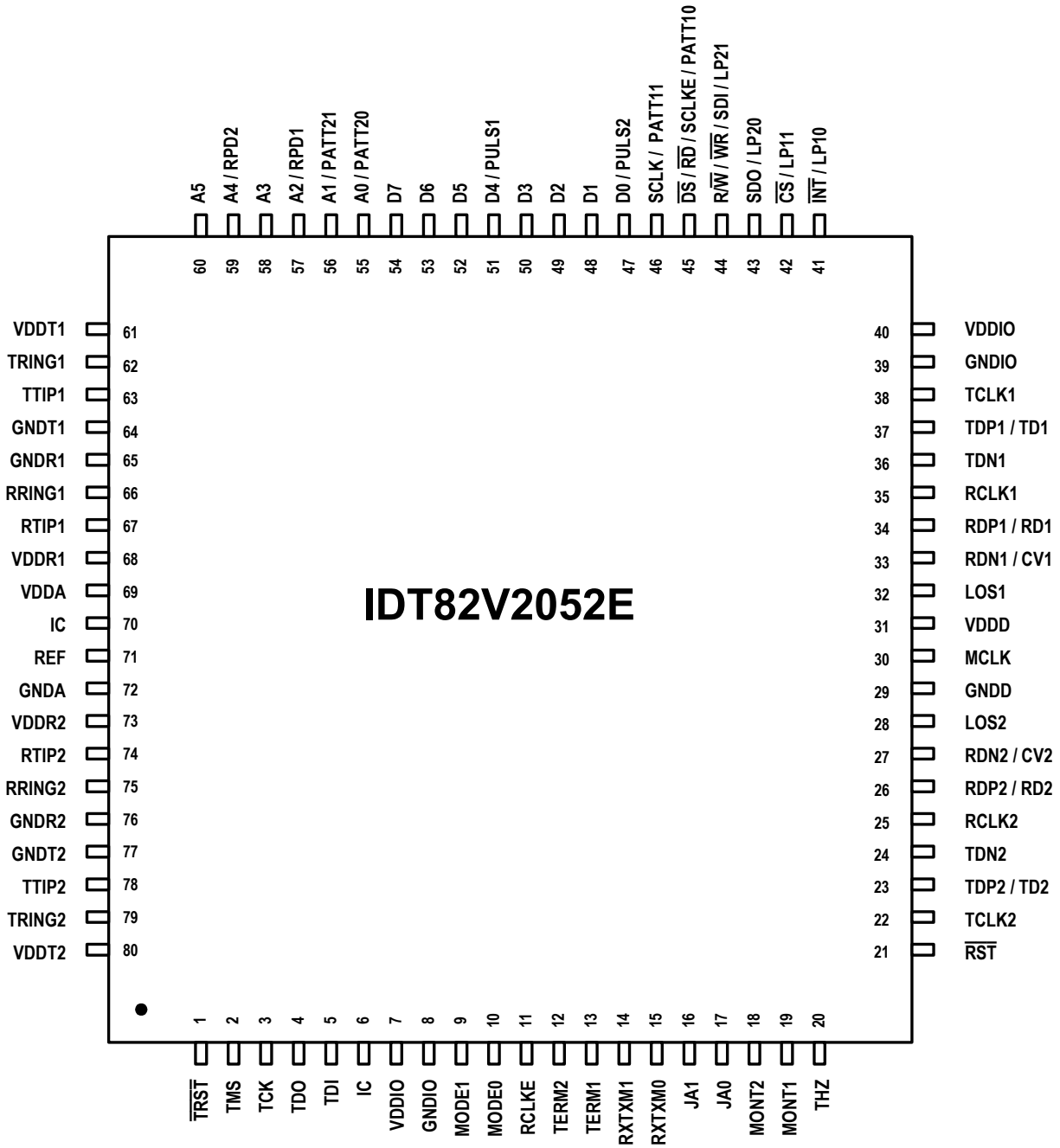


Figure-2 IDT82V2052E TQFP80 Package Pin Assignment

2 PIN DESCRIPTION

Table-1 Pin Description

<table>
<tr><th>Name</th><th>Type</th><th>Pin No.</th><th>Description</th></tr>
<tr><td>TTIP1
TTIP2

TRING1
TRING2</td><td>Analog Output</td><td>63
78

62
79</td><td>TTIPn[1]/TRINGn: Transmit Bipolar Tip/Ring for Channel 1~2
These pins are the differential line driver outputs and can be set to high impedance state globally or individually. A logic high on THZ pin turns all these pins into high impedance state. When THZ bit (TCF1, 03H...)[2] is set to ‘1’, the TTIPn/TRINGn in the corresponding channel is set to high impedance state.
In summary, these pins will become high impedance in the following conditions:
• THZ pin is high: all TTIPn/TRINGn enter high impedance;
• THZn bit is set to 1: the corresponding TTIPn/TRINGn become high impedance;
• Loss of MCLK: all TTIPn/TRINGn pins become high impedance; ·
• Loss of TCLKn: the corresponding TTIPn/TRINGn become HZ (exceptions: Remote Loopback; Transmit internal pattern by MCLK);
• Transmitter path power down: the corresponding TTIPn/TRINGn become high impedance;
• After software reset; pin reset and power on: all TTIPn/TRINGn enter high impedance.</td></tr>
<tr><td>RTIP1
RTIP2

RRING1
RRING2</td><td>Analog Input</td><td>67
74

66
75</td><td>RTIPn/RRINGn: Receive Bipolar Tip/Ring for Channel 1~2
These signals are the differential receiver inputs.</td></tr>
<tr><td>TD1/TDP1
TD2/TDP2

TDN1
TDN2</td><td>I</td><td>37
23

36
24</td><td>TDn: Transmit Data for Channel 1~2
When the device is in single rail mode, the NRZ data to be transmitted is input on this pin. Data on TDn pin is sampled into the device on the active edge of TCLKn and is encoded by AMI or HDB3 line code rules before being transmitted. In this mode, TDNn should be connected to ground.

TDPn/TDNn: Positive/Negative Transmit Data
When the device is in dual rail mode, the NRZ data to be transmitted for positive/negative pulse is input on these pins. Data on TDPn/TDNn pin is sampled into the device on the active edge of TCLKn. The active polarity is also selectable. Refer to 3.2.1 TRANSMIT PATH SYSTEM INTERFACE for details. The line code in dual rail mode is as follows:
<table>
<tr><th>TDPn</th><th>TDNn</th><th>Output Pulse</th></tr>
<tr><td>0</td><td>0</td><td>Space</td></tr>
<tr><td>0</td><td>1</td><td>Positive Pulse</td></tr>
<tr><td>1</td><td>0</td><td>Negative Pulse</td></tr>
<tr><td>1</td><td>1</td><td>Space</td></tr>
</table></td></tr>
<tr><td>TCLK1
TCLK2</td><td>I</td><td>38
22</td><td>TCLKn: Transmit Clock for Channel 1~2
This pin inputs a 2.048 MHz transmit clock. The transmit data at TDn/TDPn or TDNn is sampled into the device on the active edge of TCLKn. If TCLKn is missing[3] and the TCLKn missing interrupt is not masked, an interrupt will be generated.</td></tr>
</table>

Notes:

1. The footprint ‘n’ (n = 1~2) represents one of the two channels.
2. The name and address of the registers that contain the preceding bit. Only the address of channel 1 register is listed, the rest addresses are represented by ‘...’. Users can find these omitted addresses in the *Register Description* section.
3. TCLKn missing: the state of TCLKn continues to be high level or low level over 70 MCLK cycles.

Table-1 Pin Description (Continued)

Name	Type	Pin No.	Description
RD1/RDP1 RD2/RDP2 CV1/RDN1 CV2/RDN2	O	34 26 33 27	**RDn: Receive Data output for Channel 1~2** In single rail mode, this pin outputs NRZ data. The data is decoded according to AMI or HDB3 line code rules. **CVn: Code Violation indication** In single rail mode, the BPV/CV errors in received data stream will be reported by driving the CVn pin to high level for a full clock cycle. HDB3 line code violation can be indicated if the HDB3 decoder is enabled. When AMI decoder is selected, bipolar violation will be indicated. In hardware control mode, the EXZ, BPV/CV errors in received data stream are always monitored by the CVn pin if single rail mode is chosen. **RDPn/RDNn: Positive/Negative Receive Data output for Channel 1~2** In dual rail mode, these pins output the re-timed NRZ data when CDR is enabled, or directly outputs the raw RZ slicer data if CDR is bypassed. **Active edge and level select:** Data on RDPn/RDNn or RDn is clocked with either the rising or the falling edge of RCLKn. The active polarity is also selectable. Refer to 3.3.8 RECEIVE PATH SYSTEM INTERFACE for details.
RCLK1 RCLK2	O	35 25	**RCLKn: Receive Clock output for Channel 1~2** This pin outputs a 2.048 MHz receive clock. Under LOS conditions with AIS enabled (bit AISE=1), RCLKn is derived from MCLK. In clock recovery mode, this signal provides the clock recovered from the RTIPn/RRINGn signal. The receive data (RDn in single rail mode or RDPn and RDNn in dual rail mode) is clocked out of the device on the active edge of RCLKn. If clock recovery is bypassed, RCLKn is the exclusive OR (XOR) output of the dual rail slicer data RDPn and RDNn. This signal can be used in applications with external clock recovery circuitry.
MCLK	I	30	**MCLK: Master Clock input** A built-in clock system that accepts a 2.048 MHz reference clock. This reference clock is used to generate several internal reference signals: • Timing reference for the integrated clock recovery unit. • Timing reference for the integrated digital jitter attenuator. • Timing reference for microcontroller interface. • Generation of RCLKn signal during a loss of signal condition. • Reference clock to transmit All Ones, all zeros and PRBS pattern. Note that for ATAO and AIS, MCLK is always used as the reference clock. • Reference clock during Transmit All Ones (TAO) condition or sending PRBS in hardware control mode. The loss of MCLK will turn TTIP/TRING into high impedance status.
LOS1 LOS2	O	32 28	**LOSn: Loss of Signal Output for Channel 1~2** These pins are used to indicate the loss of received signals. When LOSn pin becomes high, it indicates the loss of received signal in channel n. The LOS pin will become low automatically when valid received signal is detected again. The criteria of loss of signal are described in 3.5 LOS AND AIS DETECTION.
REF	I	71	**REF: reference resister** An external resistor (3kΩ, 1%) is used to connect this pin to ground to provide a standard reference current for internal circuit.

Table-1 Pin Description (Continued)

<table>
<tr><th>Name</th><th>Type</th><th>Pin No.</th><th>Description</th></tr>
<tr><td>MODE1
MODE0</td><td>I</td><td>9
10</td><td>MODE[1:0]: operation mode of control interface select
The level on this pin determines which control mode is used to control the device as follows:

<table>
<tr><th>MODE[1:0]</th><th>Control Interface mode</th></tr>
<tr><td>00</td><td>Hardware interface</td></tr>
<tr><td>01</td><td>Serial Microcontroller Interface</td></tr>
<tr><td>10</td><td>Motorola non-multiplexed</td></tr>
<tr><td>11</td><td>Intel non-multiplexed</td></tr>
</table>
• The serial microcontroller interface consists of $\overline{CS}$, SCLK, SCLKE, SDI, SDO and $\overline{INT}$ pins. SCLKE is used for the selection of the active edge of SCLK.
• The parallel non-multiplexed microcontroller interface consists of $\overline{CS}$, A[5:0], D[7:0], $\overline{DS}$/$\overline{RD}$, R/$\overline{W}$/$\overline{WR}$ and $\overline{INT}$ pins. (Refer to 3.11 MICROCONTROLLER INTERFACES for details)
• Hardware interface consists of PULSn, THZ, RCLKE, LPn[1:0], PATTn[1:0], JA[1:0], MONTn, TERMn, RPDn, MODE[1:0] and RXTXM[1:0] (n=1, 2).</td></tr>
<tr><td>RCLKE</td><td>I</td><td>11</td><td>RCLKE: the active edge of RCLKn select
In hardware control mode, this pin selects the active edge of RCLKn
• L= update RDPn/RDNn on the rising edge of RCLKn
• H= update RDPn/RDNn on the falling edge of RCLKn
In software control mode, this pin should be connected to GNDIO.</td></tr>
<tr><td>RXTXM1
RXTXM0</td><td>I</td><td>14
15</td><td>RXTXM[1:0]: Receive and transmit path operation mode select
In hardware control mode, these pins are used to select the single rail or dual rail operation modes as well as AMI or HDB3 line coding:
• 00= single rail with HDB3 coding
• 01= single rail with AMI coding
• 10= dual rail interface with CDR enabled
• 11= slicer mode (dual rail interface with CDR disabled)
In software control mode, these pins should be connected to ground.</td></tr>
<tr><td>$\overline{CS}$

LP11</td><td>I</td><td>42</td><td>$\overline{CS}$: Chip Select
In serial or parallel microcontroller interface mode, this is the active low enable signal. A low level on this pin enables serial or parallel microcontroller interface.

LP11/LP10: Loopback mode select for channel 1
When the chip is configured by hardware, this pin is used to select loopback operation modes for channel 1.:
• 00 = no loopback
• 01 = analog loopback
• 10 = digital loopback
• 11 = remote loopback</td></tr>
<tr><td>$\overline{INT}$

LP10</td><td>O

I</td><td>41</td><td>$\overline{INT}$: Interrupt Request
In software control mode, this pin outputs the general interrupt request for all interrupt sources. If INTM_GLB bit (GCF, 20H) is set to ‘1’, all the interrupt sources will be masked. These interrupt sources can be masked individually via registers (INTM0, 13H...) and (INTM1, 14H...). The interrupt status is reported via the registers (INTCH, 21H), (INTS0, 18H...) and (INTS1, 19H...).

Output characteristics of this pin can be defined to be push-pull (active high or active low) or open-drain (active low) by setting bits INT_PIN[1:0] (GCF, 20H)

LP11/LP10: Loopback mode select for channel 1
See above LP11.</td></tr>
</table>

Table-1 Pin Description (Continued)

<table>
<tr><th>Name</th><th>Type</th><th>Pin No.</th><th>Description</th></tr>
<tr><td>SCLK</td><td>I</td><td>46</td><td>SCLK: Shift Clock
In serial microcontroller interface mode, this signal is the shift clock for the serial interface. Configuration data on SDI pin is sampled on the rising edge of SCLK. Configuration and status data on SDO pin is clocked out of the device on the rising edge of SCLK if SCLKE pin is low, or on the falling edge of SCLK if SCLKE pin is high.
In parallel non-multiplexed interface mode, this pin should be connected to ground.</td></tr>
<tr><td>PATT11</td><td></td><td></td><td>PATT11/PATT10: Transmit pattern select for channel 1
In hardware control mode, this pin selects the transmit pattern
• 00 = normal
• 01= All Ones
• 10= PRBS
• 11= transmitter power down</td></tr>
<tr><td>SCLKE</td><td>I</td><td>45</td><td>SCLKE: Serial Clock Edge Select
In serial microcontroller interface mode, this signal selects the active edge of SCLK for outputting SDO. The output data is valid after some delay from the active clock edge. It can be sampled on the opposite edge of the clock. The active clock edge which clocks the data out of the device is selected as shown below:
<table><tr><th>SCLKE</th><th>SCLK</th></tr><tr><td>Low</td><td>Rising edge is the active edge.</td></tr><tr><td>High</td><td>Falling edge is the active edge.</td></tr></table></td></tr>
<tr><td>$\overline{DS}$</td><td></td><td></td><td>$\overline{DS}$: Data Strobe
In Motorola parallel non-multiplexed interface mode, this signal is the data strobe of the parallel interface. In a write operation (R/$\overline{W}$ = 0), the data on D[7:0] is sampled into the device. In a read operation (R/$\overline{W}$ = 1), the data is driven to D[7:0] by the device.</td></tr>
<tr><td>$\overline{RD}$</td><td></td><td></td><td>$\overline{RD}$: Read Strobe
In Intel parallel non-Multiplexed interface mode, the data is driven to D[7:0] by the device during low level of $\overline{RD}$ in a read operation.</td></tr>
<tr><td>PATT10</td><td></td><td></td><td>PATT11/PATT10: Transmit pattern select for channel 1
See above PATT11.</td></tr>
<tr><td>SDI</td><td>I</td><td>44</td><td>SDI: Serial Data Input
In serial microcontroller interface mode, this signal is the input data to the serial interface. Configuration data at SDI pin is sampled by the device on the rising edge of SCLK.</td></tr>
<tr><td>R/$\overline{W}$</td><td></td><td></td><td>R/$\overline{W}$: Read/Write Select
In Motorola parallel non-multiplexed interface mode, this pin is low for write operation and high for read operation.</td></tr>
<tr><td>$\overline{WR}$</td><td></td><td></td><td>$\overline{WR}$: Write Strobe
In Intel parallel non-multiplexed interface mode, this pin is asserted low by the microcontroller to initiate a write cycle. The data on D[7:0] is sampled into the device in a write operation.</td></tr>
<tr><td>LP21</td><td></td><td></td><td>LP21/LP20: loopback mode select for channel 2
When the chip is configured by hardware, this pin is used to select loopback operation modes for channel 2:.
• 00 = no loopback
• 01 = analog loopback
• 10 = digital loopback
• 11 = remote loopback</td></tr>
</table>

Table-1 Pin Description (Continued)

Name	Type	Pin No.	Description
SDO	O	43	**SDO: Serial Data Output** In serial microcontroller interface mode, this signal is the output data of the serial interface. Configuration or Status data at SDO pin is clocked out of the device on the rising edge of SCLK if SCLKE pin is low, or on the falling edge of SCLK if SCLKE pin is high. In parallel non-multiplexed interface mode, this pin should be left open.
LP20	I		**LP21/LP20: loopback mode select for channel 2** See above LP21.
D7	I/O	54	**D7: Data Bus bit7** In Intel/Motorola non-multiplexed interface mode, this signal is the bi-directional data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor. In Hardware mode, this pin has to be tied to GND.
D6	I/O	53	**D6: Data Bus bit6** In Intel/Motorola non-multiplexed interface mode, this signal is the bi-directional data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor. In Hardware mode, this pin has to be tied to GND.
D5	I/O	52	**D5: Data Bus bit5** In Intel/Motorola non-multiplexed interface mode, this signal is the bi-directional data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor. In Hardware mode, this pin has to be tied to GND.
D4	I/O	51	**D4: Data Bus bit4** In Intel/Motorola non-multiplexed interface mode, this signal is the bi-directional data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor.
PULS1	I		PULS1: This pin is used to select the following functions for Channel 1 in Hardware control mode: • Transmit pulse template • Internal termination impedance (75 Ω / 120 Ω) Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.
D3	I/O	50	**D3: Data Bus bit3** In Intel/Motorola non-multiplexed interface mode, this signal is the bi-directional data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor. In Hardware mode, this pin has to be tied to GND.
D2	I/O	49	**D2: Data Bus bit2** In Intel/Motorola non-multiplexed interface mode, this signal is the bi-directional data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor. In Hardware mode, this pin has to be tied to GND.
D1	I/O	48	**D1: Data Bus bit1** In Intel/Motorola non-multiplexed interface mode, this signal is the bi-directional data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor. In Hardware mode, this pin has to be tied to GND.

Table-1 Pin Description (Continued)

Name	Type	Pin No.	Description
D0	I/O	47	**D0: Data Bus bit0** In Intel/Motorola non-multiplexed interface mode, this signal is the bi-directional data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor.
PULS2	I		PULS2: This pin is used to select the following functions for Channel 2 in Hardware control mode: • Transmit pulse template • Internal termination impedance (75 Ω / 120 Ω) Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.
A5	I	60	**A5: Address Bus bit5** In Intel/Motorola non-multiplexed interface mode, this signal is the address bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground. In Hardware mode, this pin has to be tied to GND.
A4	I	59	**A4: Address Bus bit4** In Intel/Motorola non-multiplexed interface mode, this signal is the address bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground.
RPD2			**RPD2: Power down control for receiver2 in hardware control mode** 0= receiver 2 normal operation 1= receiver 2 power down
A3	I	58	**A3: Address Bus bit3** In Intel/Motorola non-multiplexed interface mode, this signal is the address bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground. In Hardware mode, this pin has to be tied to GND.
A2	I	57	**A2: Address Bus bit2** In Intel/Motorola non-multiplexed interface mode, this signal is the address bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground.
RPD1			**RPD1: Power down control for receiver1 in hardware control mode** 0= receiver 1 normal operation 1= receiver 1 power down
A1	I	56	**A1: Address Bus bit1** In Intel/Motorola non-multiplexed interface mode, this signal is the address bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground.
PATT21			**PATT21/PATT20: Transmit pattern select for channel 2** In hardware control mode, this pin selects the transmit pattern 00 = normal 01= All Ones 10= PRBS 11= transmitter power down
A0	I	55	**A0: Address Bus bit 0** In Intel/Motorola non-multiplexed interface mode, this signal is the address bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground.
PATT20			See above
TERM1 TERM2	I	13 12	**TERMn: Selects internal or external impedance matching for channel 1 and channel 2 in hardware control mode** 0 = ternary interface with internal impedance matching network 1 = ternary interface with external impedance matching network In software control mode, this pin should be connected to ground.

Table-1 Pin Description (Continued)

Name	Type	Pin No.	Description
JA1	I	16	**JA[1:0]: Jitter attenuation position, bandwidth and the depth of FIFO select for channel 1 and channel 2 (only used in hardware control mode)** • 00 = JA is disabled • 01= JA in receiver, broad bandwidth, FIFO=64 bits • 10 = JA in receiver, narrow bandwidth, FIFO=128 bits • 11= JA in transmitter, narrow bandwidth, FIFO=128 bits In software control mode, this pin should be connected to ground.
JA0	I	17	See above.
MONT2	I	18	**MONT2: Receive Monitor gain select for channel 2** In hardware control mode with ternary interface, this pin selects the receive monitor gain of receiver: 0= 0dB 1= 26dB In software control mode, this pin should be connected to ground.
MONT1	I	19	**MONT1: Receive Monitor gain select for channel 1** In hardware control mode with ternary interface, this pin selects the receive monitor gain of receiver: 0= 0dB 1= 26dB In software control mode, this pin should be connected to ground.
$\overline{\text{RST}}$	I	21	**$\overline{\text{RST}}$: Hardware Reset** The chip is forced to reset state if a low signal is input on this pin for more than 100ns. MCLK must be active during reset.
THZ	I	20	**THZ: Transmitter Driver High Impedance Enable** This signal enables or disables all transmitter drivers on a global basis. A low level on this pin enables the driver while a high level on this pin places all drivers in high impedance state. Note that the functionality of the internal circuits is not affected by this signal.
JTAG Signals			
$\overline{\text{TRST}}$	I Pullup	1	**$\overline{\text{TRST}}$: JTAG Test Port Reset** This is the active low asynchronous reset to the JTAG Test Port. This pin has an internal pull-up resistor. To ensure deterministic operation of the test logic, TMS should be held high while the signal applied to $\overline{\text{TRST}}$ changes from low to high. For normal signal processing, this pin should be connected to ground. If JTAG is not used, this pin must be connected to ground.
TMS	I Pullup	2	**TMS: JTAG Test Mode Select** This pin is used to control the test logic state machine and is sampled on the rising edge of TCK. TMS has an internal pull-up resistor. If JTAG is not used, this pin may be left unconnected.
TCK	I	3	**TCK: JTAG Test Clock** This is the input clock for JTAG. The data on TDI and TMS are clocked into the device on the rising edge of TCK while the data on TDO is clocked out of the device on the falling edge of TCK. When TCK is idle at low state, all the stored-state devices contained in the test logic will retain their state indefinitely. If JTAG is not used, this pin may be left unconnected.
TDO	O	4	**TDO: JTAG Test Data Output** This output pin is high impedance normally and is used for reading all the serial configuration and test data from the test logic. The data on TDO is clocked out of the device on the falling edge of TCK. If JTAG is not used, this pin should be left unconnected.
TDI	I Pullup	5	**TDI: JTAG Test Data Input** This pin is used for loading instructions and data into the test logic and has an internal pull-up resistor. The data on TDI is clocked into the device on the rising edge of TCK. If JTAG is not used, this pin may be left unconnected.
Power Supplies and Grounds			
VDDIO	-	7,40	**3.3 V I/O power supply**
GNDIO	-	8,39	**I/O ground**

Table-1 Pin Description (Continued)

Name	Type	Pin No.	Description
VDDT1 VDDT2	-	61 80	3.3 V power supply for transmitter driver
GNDT1 GNDT2	-	64 77	Analog ground for transmitter driver
VDDR1 VDDR2	-	68 73	Power supply for receive analog circuit
GNDR1 GNDR2	-	65 76	Analog ground for receive analog circuit
VDDD	-	31	3.3V digital core power supply
GNDD	-	29	Digital core ground
VDDA	-	69	Analog core circuit power supply
GNDA	-	72	Analog core circuit ground
Others			
IC	-	70	**IC: Internal Connection** Internal Use. This pin should be left open in normal operation.
IC	-	6	**IC: Internal Connection** Internal Use. This pin should be connected to ground in normal operation.

3 FUNCTIONAL DESCRIPTION

3.1 CONTROL MODE SELECTION

The IDT82V2052E can be configured by software or by hardware. The software control mode supports Serial Control Interface, Motorola non-Multiplexed Control Interface and Intel non-Multiplexed Control Interface. The Control mode is selected by MODE1 and MODE0 pins as follows:

	Control Interface Mode
00	Hardware interface
01	Serial Microcontroller Interface.
10	Parallel -non-Multiplexed -Motorola Interface
11	Parallel -non-Multiplexed -Intel Interface

- The serial microcontroller Interface consists of $\overline{CS}$, SCLK, SCLKE, SDI, SDO and $\overline{INT}$ pins. SCLKE is used for the selection of active edge of SCLK.
- The parallel non-Multiplexed microcontroller Interface consists of $\overline{CS}$, A[5:0], D[7:0], $\overline{DS}$/$\overline{RD}$, R/$\overline{W}$/$\overline{WR}$ and $\overline{INT}$ pins.
- Hardware interface consists of PULSn, THZ, RCLKE, LPn[1:0], PATTn[1:0], JA[1:0], MONTn, TERMn, RPDn, MODE[1:0] and RXTXM[1:0] (n=1, 2). Refer to 5 HARDWARE CONTROL PIN SUMMARY for details about hardware control.

3.2 TRANSMIT PATH

The transmit path of each channel of IDT82V2052E consists of an Encoder, an optional Jitter Attenuator, a Waveform Shaper, a Line Driver and a Programmable Transmit Termination.

3.2.1 TRANSMIT PATH SYSTEM INTERFACE

The transmit path system interface consists of TCLKn pin, TDn/TDPn pin and TDNn pin. TCLKn is a 2.048 MHz clock. If TCLKn is missing for more than 70 MCLK cycles, an interrupt will be generated if it is not masked.

Transmit data is sampled on the TDn/TDPn and TDNn pins by the active edge of TCLKn. The active edge of TCLKn can be selected by the TCLK_SEL bit (**TCF0, 04H...**). And the active level of the data on TDn/TDPn and TDNn can be selected by the TD_INV bit (**TCF0, 04H...**). In hardware control mode, the falling edge of TCLKn and the active high of transmit data are always used.

The transmit data from the system side can be provided in two different ways: Single Rail and Dual Rail. In Single Rail mode, only TDn pin is used for transmitting data and the T_MD[1] bit (**TCF0, 04H...**) should be set to '0'. In Dual Rail Mode, both TDPn pin and TDNn pin are used for transmitting data, the T_MD[1] bit (**TCF0, 04H...**) should be set to '1'.

3.2.2 ENCODER

In Single Rail mode, the Encoder can be configured to be a HDB3 encoder or an AMI encoder by setting T_MD[0] bit (**TCF0, 04H...**).

In Dual Rail mode, the Encoder is by-passed. In Dual Rail mode, a logic '1' on the TDPn pin and a logic '0' on the TDNn pin results in a negative pulse on the TTIPn/TRINGn; a logic '0' on TDPn pin and a logic '1' on TDNn pin results in a positive pulse on the TTIPn/TRINGn. If both TDPn and TDNn are high or low, the TTIPn/TRINGn outputs a space (Refer to TDn/TDPn, TDNn Pin Description).

In hardware control mode, the operation mode of receive and transmit path can be selected by setting RXTXM1 and RXTXM0 pins on a global basis. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

3.2.3 PULSE SHAPER

The IDT82V2052E provides two ways of manipulating the pulse shape before sending it. One is to use preset pulse templates; the other is to use user-programmable arbitrary waveform template.

In software control mode, the pulse shape can be selected by setting the related registers.

In hardware control mode, the pulse shape can be selected by setting PULSn pins on a per channel basis. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

3.2.3.1 Preset Pulse Templates

The pulse shape is shown in Figure-3 according to the G.703 and the measuring diagram is shown in Figure-4. In internal impedance matching mode, if the cable impedance is 75 Ω, the PULS[3:0] bits (**TCF1, 05H...**) should be set to '0000'; if the cable impedance is 120 Ω, the PULS[3:0] bits (**TCF1, 05H...**) should be set to '0001'. In external impedance matching mode, for both E1/75 Ω and E1/120 Ω cable impedance, PULS[3:0] should be set to '0001'.

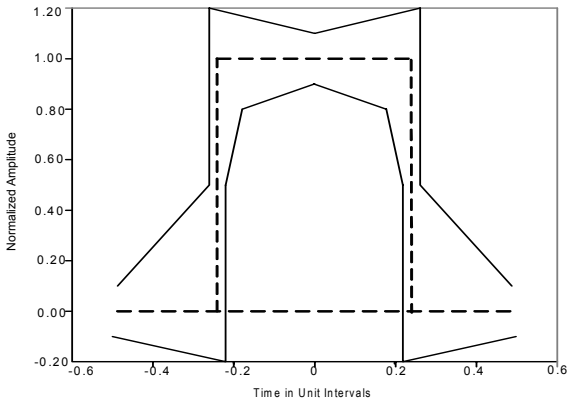
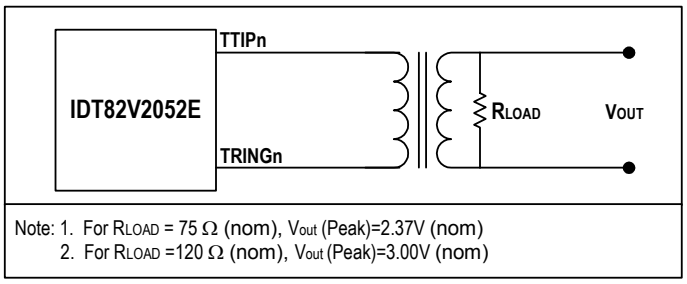


Figure-3 E1 Waveform Template Diagram



Note: 1. For R_{LOAD} = 75 Ω (nom), V_{out} (Peak)=2.37V (nom)
2. For R_{LOAD} =120 Ω (nom), V_{out} (Peak)=3.00V (nom)

Figure-4 E1 Pulse Template Test Circuit

3.2.3.2 User-Programmable Arbitrary Waveform

When the PULS[3:0] bits are set to '11xx', user-programmable arbitrary waveform generator mode can be used in the corresponding channel. This allows the transmitter performance to be tuned for a wide variety of line condition or special application.

Each pulse shape can extend up to 4 UIs (Unit Interval), addressed by UI[1:0] bits (**TCF3, 07H...**) and each UI is divided into 16 sub-phases, addressed by the SAMP[3:0] bits (**TCF3, 07H...**). The pulse amplitude of each phase is represented by a binary byte, within the range from +63 to -63, stored in WDAT[6:0] bits (**TCF4, 08H...**) in signed magnitude form. The most positive number +63 (D) represents the maximum positive amplitude of the transmit pulse while the most negative number -63 (D) represents the maximum negative amplitude of the transmit pulse. Therefore, up to 64 bytes are used. For each channel, a 64 bytes RAM is available.

There are two standard templates which are stored in an on-chip ROM. User can select one of them as reference and make some changes to get the desired waveform.

User can change the wave shape and the amplitude to get the desired pulse shape. In order to do this, firstly, users can choose a set of waveform value from the following two tables, which is the most similar to the desired pulse shape. Table-2 and Table-3 list the sample data and scaling data of each of the two templates. Then modify the corresponding sample data to get the desired transmit pulse shape.

Secondly, through the value of SCAL[5:0] bits increased or decreased by 1, the pulse amplitude can be scaled up or down at the percentage ratio against the standard pulse amplitude if needed. For different pulse shapes, the value of SCAL[5:0] bits and the scaling percentage ratio are different. The following two tables list these values.

Do the followings step by step, the desired waveform can be programmed, based on the selected waveform template:

(1).Select the UI by UI[1:0] bits (**TCF3, 07H...**)

(2).Specify the sample address in the selected UI by SAMP [3:0] bits (**TCF3, 07H...**)

(3).Write sample data to WDAT[6:0] bits (**TCF4, 08H...**). It contains the data to be stored in the RAM, addressed by the selected UI and the corresponding sample address.

(4).Set the RW bit (**TCF3, 07H...**) to '0' to implement writing data to RAM, or to '1' to implement read data from RAM

(5).Implement the Read from RAM/Write to RAM by setting the DONE bit (**TCF3, 07H...**)

Repeat the above steps until all the sample data are written to or read from the internal RAM.

(6).Write the scaling data to SCAL[5:0] bits (**TCF2, 06H...**) to scale the amplitude of the waveform based on the selected standard pulse amplitude

When more than one UI is used to compose the pulse template, the overlap of two consecutive pulses could make the pulse amplitude overflow (exceed the maximum limitation) if the pulse amplitude is not set properly. This overflow is captured by DAC_OV_IS bit (**INTS1, 19H...**), and, if enabled by the DAC_OV_IM bit (**INTM1, 14H...**), an interrupt will be generated.

The following tables give all the sample data based on the preset pulse templates in detail for reference. For preset pulse templates, scaling up/down against the pulse amplitude is not supported.

1. Table-2 Transmit Waveform Value for E1 75 Ω
2. Table-3 Transmit Waveform Value for E1 120 Ω

Table-2 Transmit Waveform Value For E1 75 Ohm

Sample	UI 1	UI 2	UI 3	UI 4
1	0000000	0000000	0000000	0000000
2	0000000	0000000	0000000	0000000
3	0000000	0000000	0000000	0000000
4	0001100	0000000	0000000	0000000
5	0110000	0000000	0000000	0000000
6	0110000	0000000	0000000	0000000
7	0110000	0000000	0000000	0000000
8	0110000	0000000	0000000	0000000
9	0110000	0000000	0000000	0000000
10	0110000	0000000	0000000	0000000
11	0110000	0000000	0000000	0000000
12	0110000	0000000	0000000	0000000
13	0000000	0000000	0000000	0000000
14	0000000	0000000	0000000	0000000
15	0000000	0000000	0000000	0000000
16	0000000	0000000	0000000	0000000
SCAL[5:0] = 100001 (default), One step change of this value of SCAL[5:0] results in 3% scaling up/down against the pulse amplitude.				

Table-3 Transmit Waveform Value For E1 120 Ohm

Sample	UI 1	UI 2	UI 3	UI 4
1	0000000	0000000	0000000	0000000
2	0000000	0000000	0000000	0000000
3	0000000	0000000	0000000	0000000
4	0001111	0000000	0000000	0000000
5	0111100	0000000	0000000	0000000
6	0111100	0000000	0000000	0000000
7	0111100	0000000	0000000	0000000
8	0111100	0000000	0000000	0000000
9	0111100	0000000	0000000	0000000
10	0111100	0000000	0000000	0000000
11	0111100	0000000	0000000	0000000
12	0111100	0000000	0000000	0000000
13	0000000	0000000	0000000	0000000
14	0000000	0000000	0000000	0000000
15	0000000	0000000	0000000	0000000
16	0000000	0000000	0000000	0000000
SCAL[5:0] = 100001 (default), One step change of this value of SCAL[5:0] results in 3% scaling up/down against the pulse amplitude.				

3.2.4 TRANSMIT PATH LINE INTERFACE

The transmit line interface consists of TTIPn and TRINGn pins. The impedance matching can be realized by the internal impedance matching circuit or the external impedance matching circuit. If T_TERM[2] is set to '0', the internal impedance matching circuit will be selected. In this case, the T_TERM[1:0] bits (**TERM, 02H...**) can be set to choose 75 Ω or 120 Ω internal impedance of TTIPn/TRINGn. If T_TERM[2] is set to '1', the internal impedance matching circuit will be disabled. In this case, the external impedance matching circuit will be used to realize the impedance matching.

Figure-6 shows the appropriate external components to connect with the cable for one channel. Table-4 is the list of the recommended impedance matching for transmitter.

In hardware control mode, TERMn pin can be used to select impedance matching for both receiver and transmitter on a per channel basis. If TERMn pin is low, internal impedance network will be used. If TERMn pin is high, external impedance network will be used. When internal impedance network is used, PULSn pins should be set to select the specific internal impedance in the corresponding channel. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

The TTIPn/TRINGn can also be turned into high impedance globally by pulling THZ pin to high or individually by setting the THZ bit (**TCF1, 05H...**) to '1'. In this state, the internal transmit circuits are still active.

In hardware control mode, TTIPn/TRINGn pins can be turned into high impedance globally by pulling THZ pin to high. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

Besides, in the following cases, TTIPn/TRINGn will also become high impedance:

- Loss of MCLK;
- Loss of TCLKn (exceptions: Remote Loopback; Transmit internal pattern by MCLK);
- Transmit path power down;
- After software reset; pin reset and power on.

Table-4 Impedance Matching for Transmitter

Cable Configuration	Internal Termination			External Termination		
	T_TERM[2:0]	PULS[3:0]	R_T	T_TERM[2:0]	PULS[3:0]	R_T
E1 / 75 Ω	000	0000	0 Ω	1XX	0001	9.4 Ω
E1 / 120 Ω	001	0001			0001	

Note: The precision of the resistors should be better than ± 1%

3.2.5 TRANSMIT PATH POWER DOWN

The transmit path can be powered down individually by setting the T_OFF bit (**TCF0, 04H...**) to '1'. In this case, the TTIPn/TRINGn pins are turned into high impedance.

In hardware control mode, the transmit path can be powered down by setting PATTn[1:0] pins to '11' on a per channel basis. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

3.3 RECEIVE PATH

The receive path consists of Receive Internal Termination, Monitor Gain, Amplitude/Wave Shape Detector, Digital Tuning Controller, Adaptive Equalizer, Data Slicer, CDR (Clock & Data Recovery), Optional Jitter Attenuator, Decoder and LOS/AIS Detector. Refer to Figure-5.

3.3.1 RECEIVE INTERNAL TERMINATION

The impedance matching can be realized by the internal impedance matching circuit or the external impedance matching circuit. If R_TERM[2] is set to '0', the internal impedance matching circuit will be selected. In this case, the R_TERM[1:0] bits (**TERM, 02H...**) can be set to choose 75 Ω or 120 Ω internal impedance of RTIPn/RRINGn. If R_TERM[2] is set to '1', the internal impedance matching circuit will be disabled. In this case, the external impedance matching circuit will be used to realize the impedance matching.

Figure-6 shows the appropriate external components to connect with the cable for one channel. Table-5 is the list of the recommended impedance matching for receiver.

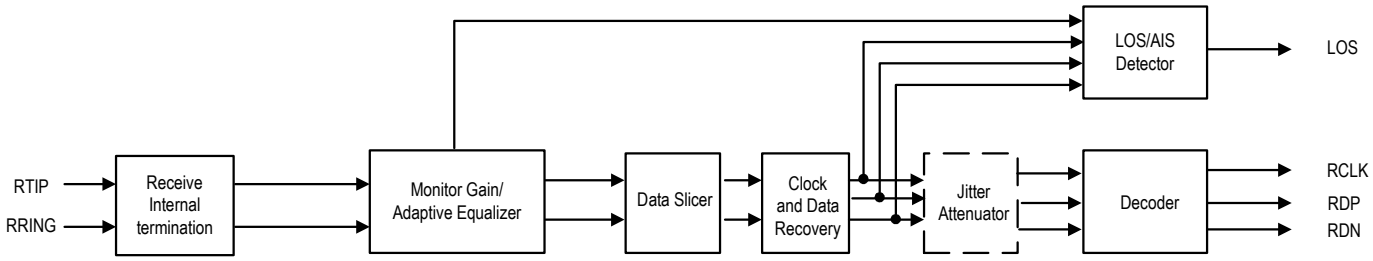
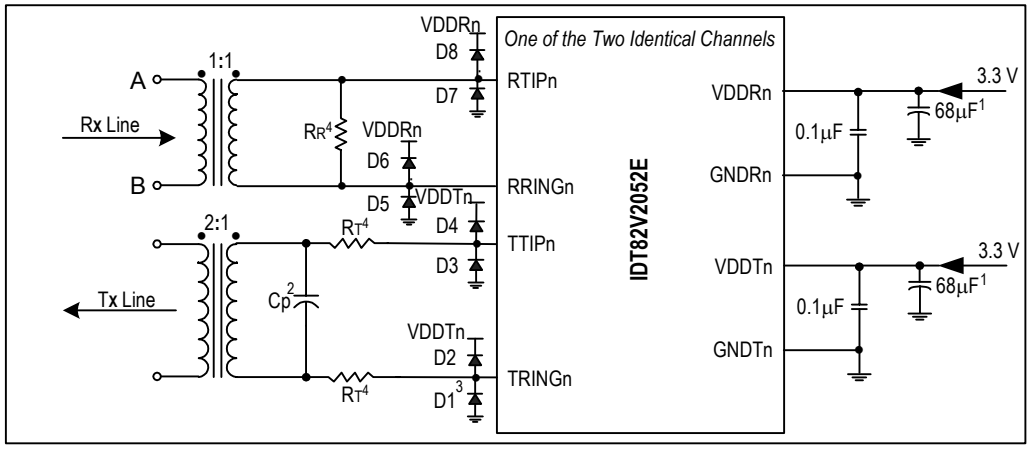


Figure-5 Receive Path Function Block Diagram

Table-5 Impedance Matching for Receiver

Cable Configuration	Internal Termination		External Termination	
	R_TERM[2:0]	R_R	R_TERM[2:0]	R_R
E1 / 75 Ω	000	120 Ω	1XX	75 Ω
E1 / 120 Ω	001			120 Ω



Note:
1. Common decoupling capacitor. One per chip
2. Cp 0-560 (pF)
3. D1 - D8, Motorola - MBR0540T1; International Rectifier - 11DQ04 or 10BQ060
4. R_T/ R_R: refer to Table-4 and Table-5 respecivley for R_T and R_R values

Figure-6 Transmit/Receive Line Circuit

In hardware control mode, TERMn, PULSn pins can be used to select impedance matching for both receiver and transmitter on a per channel basis. If TERMn pin is low, internal impedance network will be used. If TERMn pin is high, external impedance network will be used. When internal impedance network is used, PULSn pins should be set to select specific internal impedance for the corresponding channel. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

3.3.2 LINE MONITOR

The non-intrusive monitoring on channels located in other chips can be performed by tapping the monitored channel through a high impedance bridging circuit. Refer to Figure-7 and Figure-8.

After a high resistance bridging circuit, the signal arriving at the RTIPn/ RRINGn is dramatically attenuated. To compensate this attenuation, the Monitor Gain can be used to boost the signal by 22 dB, 26 dB and 32 dB, selected by MG[1:0] bits (**RCF2, 0BH...**). For normal operation, the Monitor Gain should be set to 0 dB.

In hardware control mode, MONTn pin can be used to set the Monitor Gain on a per channel basis. When MONTn pin is low, the Monitor Gain for the specific channel is 0 dB. When MONTn pin is high, the Monitor Gain for the specific channel is 26 dB. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

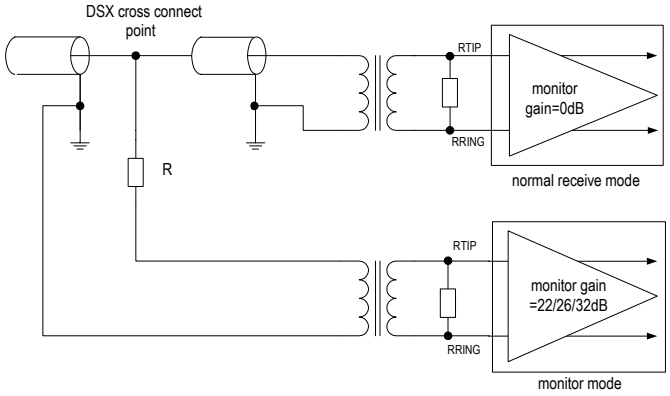


Figure-7 Monitoring Receive Line in Another Chip

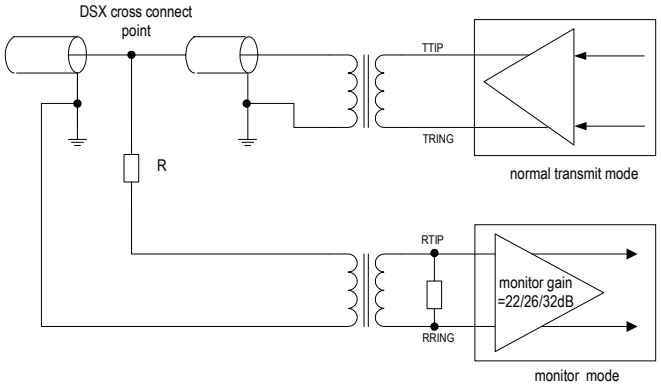


Figure-8 Monitor Transmit Line in Another Chip

3.3.3 ADAPTIVE EQUALIZER

The Adaptive Equalizer can be enabled to increase the receive sensitivity and to allow programming of the LOS level up to -24 dB. See section 3.5 LOS AND AIS DETECTION. It can be enabled or disabled by setting EQ_ON bit to '1' or '0' (**RCF1, 0AH...**).

3.3.4 RECEIVE SENSITIVITY

In Host mode, the Receive Sensitivity is -10 dB. With the Adaptive Equalizer enabled, the receive sensitivity will be -20 dB.

In Hardware mode, the Adaptive Equalizer can not be enabled and the receive sensitivity is fixed at -10 dB. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

3.3.5 DATA SLICER

The Data Slicer is used to generate a standard amplitude mark or a space according to the amplitude of the input signals. The threshold can be 40%, 50%, 60% or 70%, as selected by the SLICE[1:0] bits (**RCF2, 0BH...**). The output of the Data Slicer is forwarded to the CDR (Clock & Data Recovery) unit or to the RDPn/RDNn pins directly if the CDR is disabled.

3.3.6 CDR (Clock & Data Recovery)

The CDR is used to recover the clock and data from the received signal. The recovered clock tracks the jitter in the data output from the Data Slicer and keeps the phase relationship between data and clock during the absence of the incoming pulse. The CDR can also be by-passed in the Dual Rail mode. When CDR is by-passed, the data from the Data Slicer is output to the RDPn/RDNn pins directly.

3.3.7 DECODER

The R_MD[1:0] bits (**RCF0, 09H...**) are used to select the AMI decoder or HDB3 decoder.

When the chip is configured by hardware, the operation mode of receive and transmit path can be selected by setting RXTXM[1:0] pins on a global basis. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

3.3.8 RECEIVE PATH SYSTEM INTERFACE

The receive path system interface consists of RCLKn pin, RDn/RDPn pin and RDNn pin. The RCLKn outputs a recovered 2.048 MHz clock. The received data is updated on the RDn/RDPn and RDNn pins on the active edge of RCLKn. The active edge of RCLKn can be selected by the RCLK_SEL bit (**RCF0, 09H...**). And the active level of the data on RDn/RDPn and RDNn can be selected by the RD_INV bit (**RCF0, 09H...**).

In hardware control mode, only the active edge of RCLKn can be selected. If RCLKE is set to high, the falling edge will be chosen as the active edge of RCLKn. If RCLKE is set to low, the rising edge will be chosen as the active edge of RCLKn. The active level of the data on RDn/RDPn and RDNn is the same as that in software control mode.

The received data can be output to the system side in two different ways: Single Rail or Dual Rail, as selected by R_MD bit [1] (**RCF0, 09H...**). In Single Rail mode, only RDn pin is used to output data and the RDNn/CVn pin is used to report the received errors. In Dual Rail Mode, both RDPn pin and RDNn pin are used for outputting data.

In the receive Dual Rail mode, the CDR unit can be by-passed by setting R_MD[1:0] to '11' (binary). In this situation, the output data from the Data Slicer will be output to the RDPn/RDNn pins directly, and the RCLKn outputs the exclusive OR (XOR) of the RDPn and RDNn. This is called receiver slicer mode. In this case, the transmit path is still operating in Dual Rail mode.

3.3.9 RECEIVE PATH POWER DOWN

The receive path can be powered down individually by setting R_OFF bit (**RCF0, 09H...**) to '1'. In this case, the RCLKn, RDn/RDPn, RDNn and LOSn will be logic low.

In hardware control mode, receiver power down can be selected by pulling RPDn pin to high on a per channel basis. Refer to 5 HARDWARE CONTROL PIN SUMMARY for more details.

3.3.10 G.772 NON-INTRUSIVE MONITORING

In applications using only one channel, channel 1 can be configured to monitor the data received or transmitted in channel 2. The MONT[1:0] bits (**GCF, 20H**) determine which direction (transmit/receive) will be monitored. The monitoring is non-intrusive per ITU-T G.772. Figure-9 illustrates the concept.

The monitored line signal (transmit or receive) goes through Channel 1's Clock and Data Recovery. The signal can be observed digitally at the RCLK1, RD1/RDP1 and RDN1. If Channel 1 is configured to Remote Loopback while in the Monitoring mode, the monitored data will be output on TTIP1/TRING1.

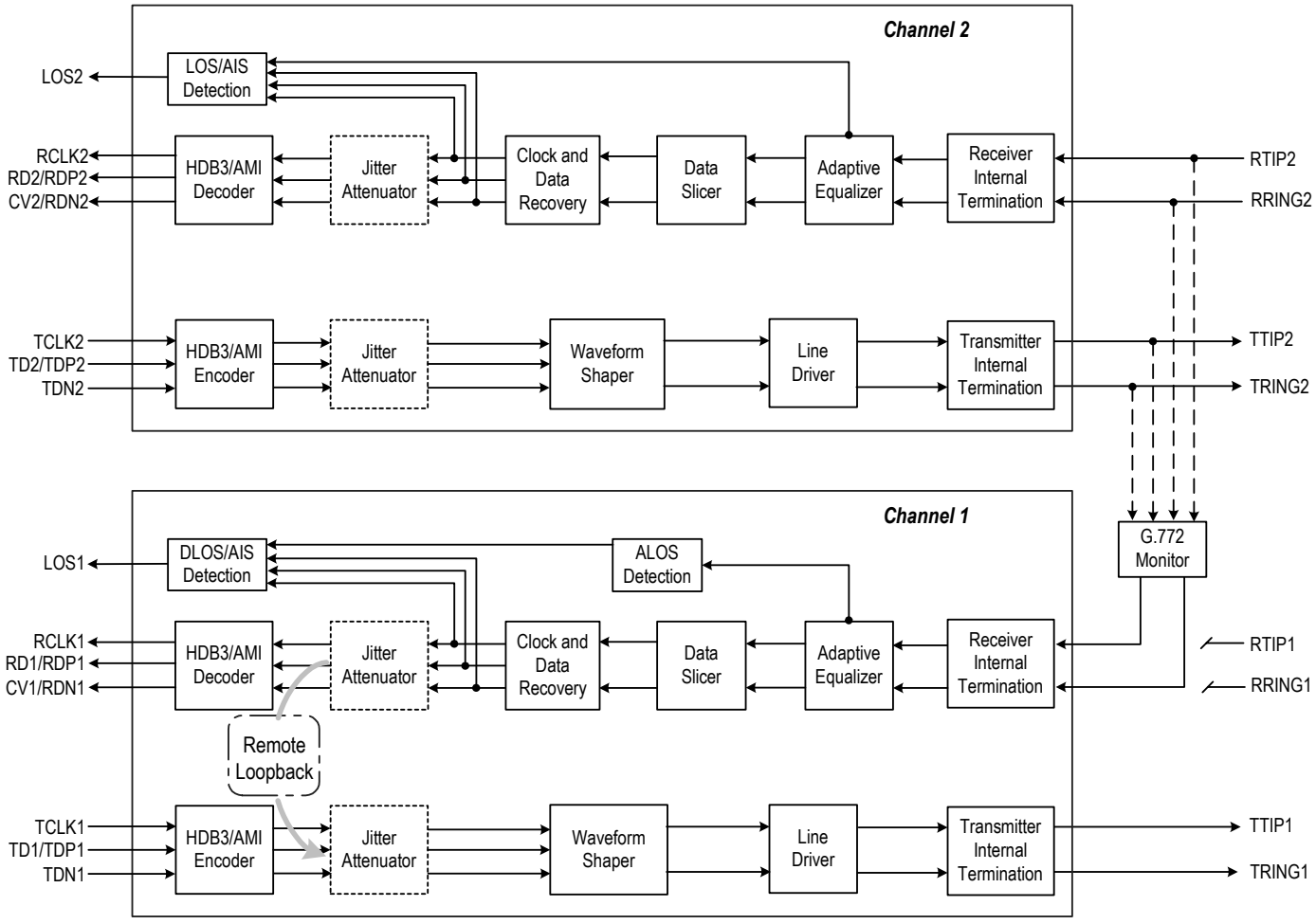


Figure-9 G.772 Monitoring Diagram

3.4 JITTER ATTENUATOR

There is one Jitter Attenuator in each channel of the LIU. The Jitter Attenuator can be deployed in the transmit path or the receive path, and can also be disabled. This is selected by the JACF[1:0] bits (**JACF, 03H...**).

In hardware control mode, Jitter Attenuator position, bandwidth and the depth of FIFO can be selected by JA[1:0] pins on a global basis. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

3.4.1 JITTER ATTENUATION FUNCTION DESCRIPTION

The Jitter Attenuator is composed of a FIFO and a DPLL, as shown in Figure-10. The FIFO is used as a pool to buffer the jittered input data, then the data is clocked out of the FIFO by a de-jittered clock. The depth of the FIFO can be 32 bits, 64 bits or 128 bits, as selected by the JADP[1:0] bits (**JACF, 03H...**). In hardware control mode, the depth of FIFO can be selected by JA[1:0] pins on a global basis. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details. Consequently, the constant delay of the Jitter Attenuator will be 16 bits, 32 bits or 64 bits. Deeper FIFO can tolerate larger jitter, but at the cost of increasing data latency time.

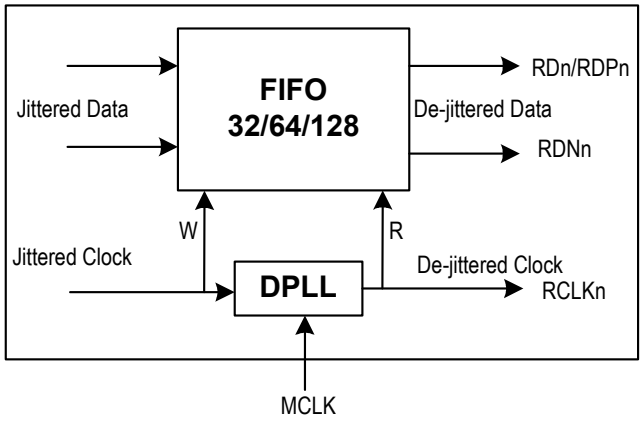


Figure-10 Jitter Attenuator

The Corner Frequency of the DPLL can be 0.9 Hz or 6.8 Hz, as selected by the JABW bit (**JACF, 03H...**). The lower the Corner Frequency is, the longer time is needed to achieve synchronization.

When the incoming data moves faster than the outgoing data, the FIFO will overflow. This overflow is captured by the JAOV_IS bit (**INTS1, 19H...**). If the incoming data moves slower than the outgoing data, the FIFO will underflow. This underflow is captured by the JAUD_IS bit (**INTS1, 19H...**). For some applications that are sensitive to data corruption, the JA limit mode can be enabled by setting JA_LIMIT bit (**JACF, 03H...**) to '1'. In the JA limit mode, the speed of the outgoing data will be adjusted automatically when the FIFO is close to its full or emptiness. The criteria of starting speed adjustment are shown in Table-6. The JA limit mode can reduce the possibility of FIFO overflow and underflow, but the quality of jitter attenuation is deteriorated.

Table-6 Criteria of Starting Speed Adjustment

FIFO Depth	Criteria for Adjusting Data Outgoing Speed
32 Bits	2 bits close to its full or emptiness
	3 bits close to its full or emptiness
	4 bits close to its full or emptiness

3.4.2 JITTER ATTENUATOR PERFORMANCE

The performance of the Jitter Attenuator in the IDT82V2052E meets the ITU-T I.431, G.703, G.736-739, G.823, G.824, ETSI 300011, ETSI TBR12/13 specifications. Details of the Jitter Attenuator performance is shown in Table-52 Jitter Tolerance and Table-53 Jitter Attenuator Characteristics.

3.5 LOS AND AIS DETECTION

3.5.1 LOS DETECTION

The Loss of Signal Detector monitors the amplitude of the incoming signal level and pulse density of the received signal on RTIPn and RRINGn.

- **LOS declare (LOS=1)**

A LOS is detected when the incoming signal has “no transitions”, i.e., when the signal level is less than Q dB below nominal for N consecutive pulse intervals. Here N is defined by LAC bit (**MAINT0, 0CH...**). LOS will be declared by pulling LOSn pin to high (LOS=1) and LOS interrupt will be generated if it is not masked.

- **LOS clear (LOS=0)**

The LOS is cleared when the incoming signal has “transitions”, i.e., when the signal level is greater than P dB below nominal and has an average pulse density of at least 12.5% for M consecutive pulse intervals, starting with the receipt of a pulse. Here M is defined by LAC bit (**MAINT0, 0CH...**). LOS status is cleared by pulling LOSn pin to low.

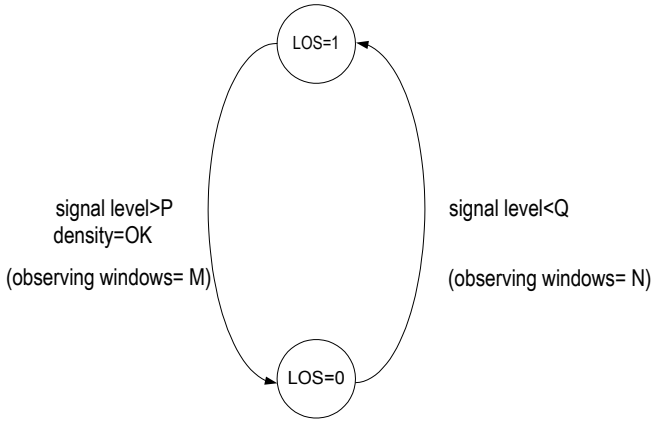


Figure-11 LOS Declare and Clear

- **LOS detect level threshold**

With the Adaptive Equalizer off, the amplitude threshold Q is fixed on 800 mVpp, while P=Q+200 mVpp (200 mVpp is the LOS level detect hysteresis).

With the Adaptive Equalizer on, the value of Q can be selected by LOS[4:0] bit (**RCF1, 0AH...**), while P=Q+4 dB (4 dB is the LOS level detect hysteresis). Refer to Table 27, “RCF1: Receiver Configuration Register 1,” on page 42 for LOS[4:0] bit values available.

When the chip is configured by hardware, the Adaptive Equalizer can not be enabled and Programmable LOS levels are not available (pin 58 & pin 60 have to be set to ‘0’).

- **Criteria for declare and clear of a LOS detect**

The detection supports G.775 and ETSI 300233/I.431. The criteria can be selected by LAC bit (**MAINT0, 0CH...**).

Table-7 and Table-8 summarize LOS declare and clear criteria for both with and without the Adaptive Equalizer enabled.

- **All Ones output during LOS**

On the system side, the RDPn/RDNn will reflect the input pulse “transition” at the RTIPn/RRINGn side and output recovered clock (but the quality of the output clock can not be guaranteed when the input level is lower than the maximum receive sensitivity) when AISE bit (**MAINT0, 0CH...**) is 0; or output All Ones as AIS when AISE bit (**MAINT0, 0CH...**) is 1. In this case RCLKn output is replaced by MCLK.

On the line side, the TTIPn/TRINGn will output All Ones as AIS when ATAO bit (**MAINT0, 0CH...**) is 1. The All Ones pattern uses MCLK as the reference clock.

LOS indicator is always active for all kinds of loopback modes.

Table-7 LOS Declare and Clear Criteria, Adaptive Equalizer Disabled

Control bit (LAC)	LOS declare threshold	LOS clear threshold
0 = G.775	Level < 800 mVpp; N=32 bits	Level > 1 Vpp; M=32 bits; 12.5% mark density; <16 consecutive zeroes
1 = I.431/ETSI	Level < 800 mVpp; N=2048 bits	Level > 1 Vpp; M=32 bits; 12.5% mark density; <16 consecutive zeroes