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OCTAL E1 SHORT HAUL LINE INTERFACE UNIT

FEATURES

- Fully integrated octal E1 short haul line interface which supports 120 Ω E1 twisted pair and 75 Ω E1 coaxial applications
- Selectable Single Rail mode or Dual Rail mode and AMI or HDB3 encoder/decoder
- Built-in transmit pre-equalization meets G.703
- Selectable transmit/receive jitter attenuator meets ETSI CTR12/13, ITU G.736, G.742 and G.823 specifications
- SONET/SDH optimized jitter attenuator meets ITU G.783 mapping jitter specification
- Digital/Analog LOS detector meets ITU G.775 and ETS 300 233
- ITU G.772 non-intrusive monitoring for in-service testing for any one of channel 1 to channel 7
- Low impedance transmit drivers with high-Z
- Selectable hardware and parallel/serial host interface
- Local and Remote Loopback test functions
- Hitless Protection Switching (HPS) for 1 to 1 protection without relays
- JTAG boundary scan for board test
- 3.3 V supply with 5 V tolerant I/O
- Low power consumption
- Operating temperature range: -40°C to +85°C
- Available in 144-pin Thin Quad Flat Pack (TQFP) and 160-pin Plastic Ball Grid Array (PBGA) packages
  Green package options available

FUNCTIONAL BLOCK DIAGRAM

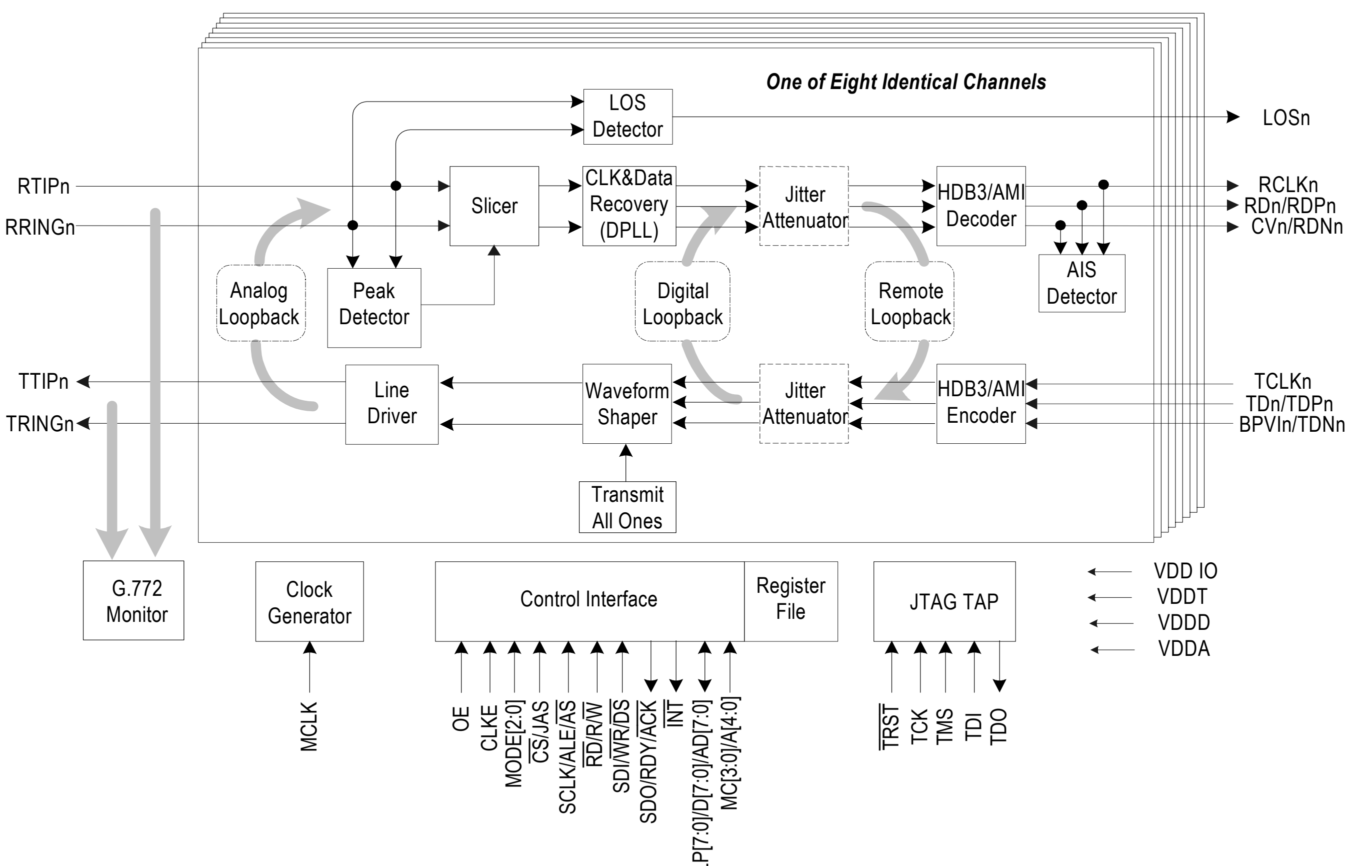


Figure-1 Block Diagram

January 21, 2010

DSC-6038/12

DESCRIPTION

The IDT82V2058 is a single chip, 8-channel E1 short haul PCM transceiver with a reference clock of 2.048 MHz. The IDT82V2058 contains 8 transmitters and 8 receivers.

All the receivers and transmitters can be programmed to work either in Single Rail mode or Dual Rail mode. HDB3 or AMI encoder/decoder is selectable in Single Rail mode. Pre-encoded transmit data in NRZ format can be accepted when the device is configured in Dual Rail mode. The receivers perform clock and data recovery by using integrated digital phase-locked loop. As an option, the raw sliced data (no retiming) can be output on the receive data pins. Transmit equalization is implemented with low-impedance output drivers that provide shaped waveforms to the transformer, guaranteeing template conformance.

A jitter attenuator is integrated in the IDT82V2058 and can be switched into either the transmit path or the receive path for all channels. The jitter attenuation performance meets ETSI CTR12/13, ITU G.736, G.742 and G.823 specifications.

The IDT82V2058 offers hardware control mode and software control mode. Software control mode works with either serial host interface or parallel host interface. The latter works via an Intel/Motorola compatible 8-bit parallel interface for both multiplexed or non-multiplexed applications. Hardware control mode uses multiplexed pins to select different operation modes when the host interface is not available to the device.

The IDT82V2058 also provides loopback and JTAG boundary scan testing functions. Using the integrated monitoring function, the IDT82V2058 can be configured as a 7-channel transceiver with non-intrusive protected monitoring points.

The IDT82V2058 can be used for SDH/SONET multiplexers, central office or PBX, digital access cross connects, digital radio base stations, remote wireless modules and microwave transmission systems.

PIN CONFIGURATIONS

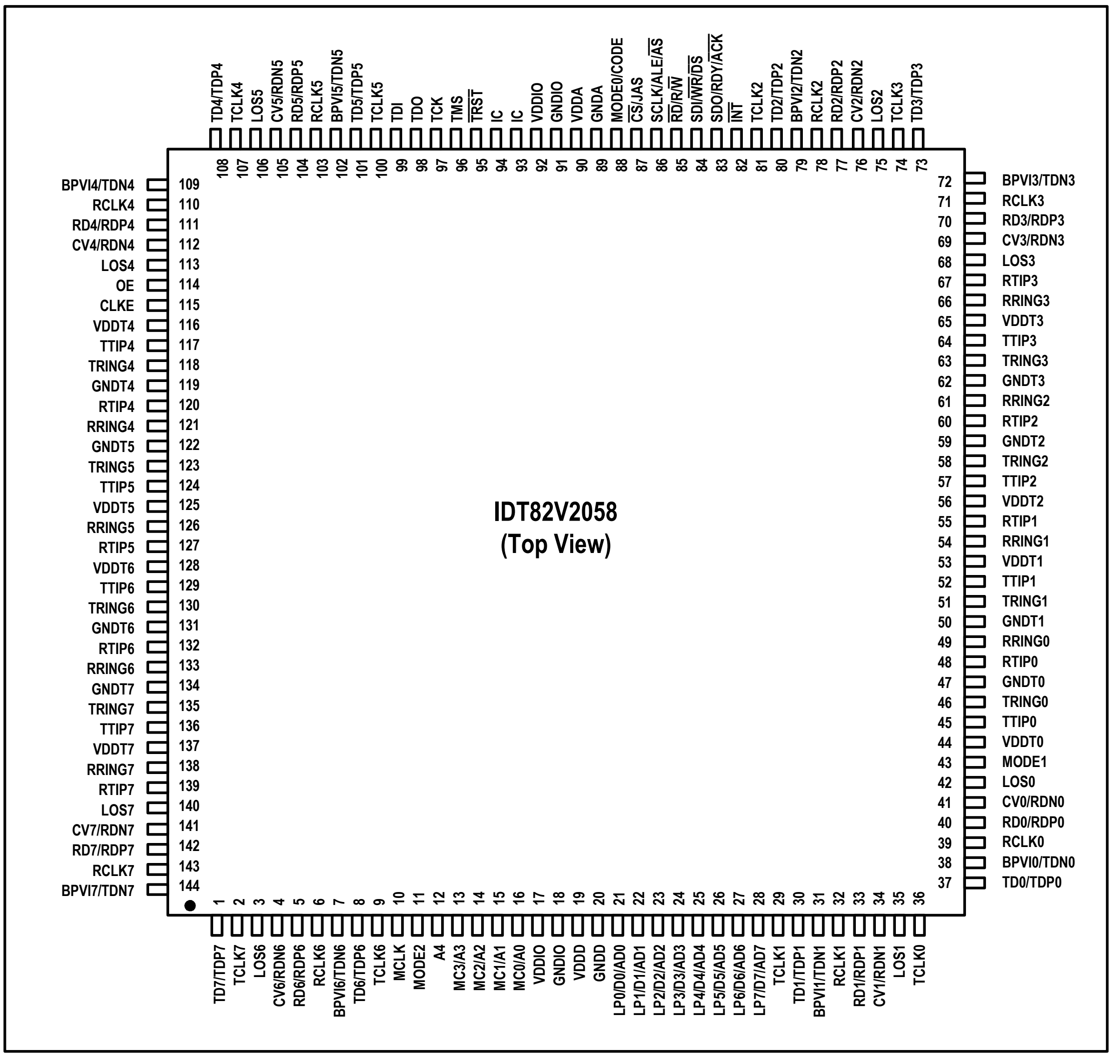


Figure-2 TQFP144 Package Pin Assignment

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	
1	RCLK 7	TCLK 7	RCLK 6	TCLK 6	MCLK	MC 1	VDDIO	VDDD	LP 6	LP 7	TCLK 1	RCLK 1	TCLK 0	RCLK 0	1
2	RDP 7	TDP 7	RDP 6	TDP 6	MODE 2	MC 2	LP 0	LP 2	LP 5	MODE 1	TDP 1	RDP 1	TDP 0	RDP 0	2
3	RDN 7	TDN 7	RDN 6	TDN 6	LOS 6	MC 3	MC 0	LP 1	LP 4	LOS 1	TDN 1	RDN 1	TDN 0	RDN 0	3
4	VDDT 7	VDDT 7	VDDT 6	VDDT 6	LOS 7	A4	GNDIO	GNDD	LP 3	LOS 0	VDDT 1	VDDT 1	VDDT 0	VDDT 0	4
5	TRING 7	TTIP 7	TRING 6	TTIP 6							TTIP 1	TRING 1	TTIP 0	TRING 0	5
6	GNDT 7	GNDT 7	GNDT 6	GNDT 6							GNDT 1	GNDT 1	GNDT 0	GNDT 0	6
7	RTIP 7	RRING 7	RTIP 6	RRING 6				IDT82V2058			RRING 1	RTIP 1	RRING 0	RTIP 0	7
8	RTIP 4	RRING 4	RTIP 5	RRING 5				(Bottom View)			RRING 2	RTIP 2	RRING 3	RTIP 3	8
9	GNDT 4	GNDT 4	GNDT 5	GNDT 5							GNDT 2	GNDT 2	GNDT 3	GNDT 3	9
10	TRING 4	TTIP 4	TRING 5	TTIP 5							TTIP 2	TRING 2	TTIP 3	TRING 3	10
11	VDDT 4	VDDT 4	VDDT 5	VDDT 5	LOS 4	TMS	GNDIO	GNDA	$\overline{CS}$	LOS 3	VDDT 2	VDDT 2	VDDT 3	VDDT 3	11
12	RDN 4	TDN 4	RDN 5	TDN 5	LOS 5	TDI	$\overline{TRST}$	MODE 0	SCLK	LOS 2	TDN 2	RDN 2	TDN 3	RDN 3	12
13	RDP 4	TDP 4	RDP 5	TDP 5	CLKE	TDO	IC	IC	$\overline{RD}$	$\overline{INT}$	TDP 2	RDP 2	TDP 3	RDP 3	13
14	RCLK 4	TCLK 4	RCLK 5	TCLK 5	OE	TCK	VDDIO	VDDA	SDI	SDO	TCLK 2	RCLK 2	TCLK 3	RCLK 3	14
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	

Figure-3 PBGA160 Package Pin Assignment

1 PIN DESCRIPTION

Table-1 Pin Description

Name	Type	Pin No.		Description
		TQFP144	PBGA160	
Transmit and Receive Line Interface				
TTIP0 TTIP1 TTIP2 TTIP3 TTIP4 TTIP5 TTIP6 TTIP7 TRING0 TRING1 TRING2 TRING3 TRING4 TRING5 TRING6 TRING7	Analog Output	45 52 57 64 117 124 129 136 46 51 58 63 118 123 130 135	N5 L5 L10 N10 B10 D10 D5 B5 P5 M5 M10 P10 A10 C10 C5 A5	**TTIPn/TRINGn: Transmit Bipolar Tip/Ring for Channel 0~7** These pins are the differential line driver outputs. They will be in high-Z if pin OE is low or the corresponding pin TCLKn is low (pin OE is global control, while pin TCLKn is per-channel control). In host mode, each pin can be in high-Z by programming a ‘1’ to the corresponding bit in register **OE**[1].
RTIP0 RTIP1 RTIP2 RTIP3 RTIP4 RTIP5 RTIP6 RTIP7 RRING0 RRING1 RRING2 RRING3 RRING4 RRING5 RRING6 RRING7	Analog Input	48 55 60 67 120 127 132 139 49 54 61 66 121 126 133 138	P7 M7 M8 P8 A8 C8 C7 A7 N7 L7 L8 N8 B8 D8 D7 B7	**RTIPn/RRINGn: Receive Bipolar Tip/Ring for Channel 0~7** These pins are the differential line receiver inputs.

1. Register name is indicated by bold capital letter. For example, **OE** indicates Output Enable Register.

Table-1 Pin Description (Continued)

<table>
<tr><th rowspan="2">Name</th><th rowspan="2">Type</th><th colspan="2">Pin No.</th><th rowspan="2">Description</th></tr>
<tr><th>TQFP144</th><th>PBGA160</th></tr>
<tr><td colspan="5">Transmit and Receive Digital Data Interface</td></tr>
<tr>
<td>TD0/TDP0
TD1/TDP1
TD2/TDP2
TD3/TDP3
TD4/TDP4
TD5/TDP5
TD6/TDP6
TD7/TDP7

BPVI0/TDN0
BPVI1/TDN1
BPVI2/TDN2
BPVI3/TDN3
BPVI4/TDN4
BPVI5/TDN5
BPVI6/TDN6
BPVI7/TDN7</td>
<td>I</td>
<td>37
30
80
73
108
101
8
1

38
31
79
72
109
102
7
144</td>
<td>N2
L2
L13
N13
B13
D13
D2
B2

N3
L3
L12
N12
B12
D12
D3
B3</td>
<td>TDn: Transmit Data for Channel 0~7
When the device is in Single Rail mode, the NRZ data to be transmitted is input on this pin. Data on TDn is sampled into the device on the falling edges of TCLKn, and encoded by AMI or HDB3 line code rules before being transmitted to the line.

BPVIn: Bipolar Violation Insertion for Channel 0~7
Bipolar violation insertion is available in Single Rail mode 2 (see Table-2 on page 13 and Table-3 on page 14) with AMI enabled. A low-to-high transition on this pin will make the next logic one to be transmitted on TDn the same polarity as the previous pulse, and violate the AMI rule. This is for testing.

TDPn/TDNn: Positive/Negative Transmit Data for Channel 0~7
When the device is in Dual Rail Mode, the NRZ data to be transmitted for positive/negative pulse is input on this pin. Data on TDPn/TDNn are sampled on the falling edges of TCLKn. The line code in dual rail mode is as the follow:
<table>
<tr><th>TDPn</th><th>TDNn</th><th>Output Pulse</th></tr>
<tr><td>0</td><td>0</td><td>Space</td></tr>
<tr><td>0</td><td>1</td><td>Negative Pulse</td></tr>
<tr><td>1</td><td>0</td><td>Positive Pulse</td></tr>
<tr><td>1</td><td>1</td><td>Space</td></tr>
</table>
Pulling pin TDNn high for more than 16 consecutive TCLK clock cycles will configure the corresponding channel into Single Rail mode 1 (see Table-2 on page 13 and Table-3 on page 14).</td>
</tr>
<tr>
<td>TCLK0
TCLK1
TCLK2
TCLK3
TCLK4
TCLK5
TCLK6
TCLK7</td>
<td>I</td>
<td>36
29
81
74
107
100
9
2</td>
<td>N1
L1
L14
N14
B14
D14
D1
B1</td>
<td>TCLKn: Transmit Clock for Channel 0~7
The clock of 2.048 MHz for transmit is input on this pin. The transmit data at TDn/TDPn or TDNn is sampled into the device on the falling edges of TCLKn.
Pulling TCLKn high for more than 16 MCLK cycles, the corresponding transmitter is set in Transmit All Ones (TAOS) state (when MCLK is clocked). In TAOS state, the TAOS generator adopts MCLK as the clock reference.
If TCLKn is low, the corresponding transmit channel is set into power down state, while driver output ports become high-Z.
Different combinations of TCLKn and MCLK result in different transmit mode. It is summarized as the follows:
<table>
<tr><th>MCLK</th><th>TCLKn</th><th colspan="2">Transmit Mode</th></tr>
<tr><td>Clocked</td><td>Clocked</td><td colspan="2">Normal operation</td></tr>
<tr><td>Clocked</td><td>High (≥ 16 MCLK)</td><td colspan="2">Transmit All Ones (TAOS) signals to the line side in the corresponding transmit channel.</td></tr>
<tr><td>Clocked</td><td>Low (≥ 64 MCLK)</td><td colspan="2">The corresponding transmit channel is set into power down state.</td></tr>
<tr><td rowspan="4">High/Low</td><td rowspan="4">TCLK1 is clocked</td><td>TCLKn is clocked</td><td>Normal operation</td></tr>
<tr><td>TCLKn is high (≥ 16 TCLK1)</td><td>Transmit All Ones (TAOS) signals to the line side in the corresponding transmit channel.</td></tr>
<tr><td>TCLKn is low (≥ 64 TCLK1)</td><td>Corresponding transmit channel is set into power down state.</td></tr>
<tr><td colspan="2">The receive path is not affected by the status of TCLK1. When MCLK is high, all receive paths just slice the incoming data stream. When MCLK is low, all the receive paths are powered down.</td></tr>
<tr><td>High/Low</td><td>TCLK1 is unavailable.</td><td colspan="2">All eight transmitters (TTIPn & TRINGn) will be in high-Z.</td></tr>
</table></td>
</tr>
</table>

Table-1 Pin Description (Continued)

Name	Type	Pin No.		Description
		TQFP144	PBGA160	
RD0/RDP0 RD1/RDP1 RD2/RDP2 RD3/RDP3 RD4/RDP4 RD5/RDP5 RD6/RDP6 RD7/RDP7 CV0/RDN0 CV1/RDN1 CV2/RDN2 CV3/RDN3 CV4/RDN4 CV5/RDN5 CV6/RDN6 CV7/RDN7	O High-Z	40 33 77 70 111 104 5 142 41 34 76 69 112 105 4 141	P2 M2 M13 P13 A13 C13 C2 A2 P3 M3 M12 P12 A12 C12 C3 A3	**RDn: Receive Data for Channel 0~7** In Single Rail mode, the received NRZ data is output on this pin. The data is decoded by AMI or HDB3 line code rule. **CVn: Code Violation for Channel 0~7** In Single Rail mode, the bipolar violation, code violation and excessive zeros will be reported by driving pin CVn high for a full clock cycle. However, only bipolar violation is indicated when AMI decoder is selected. **RDPn/RDNn: Positive/Negative Receive Data for Channel 0~7** In Dual Rail Mode with clock recovery, these pins output the NRZ data. A high signal on RDPn indicates the receipt of a positive pulse on RTIPn/RRINGn while a high signal on RDNn indicates the receipt of a negative pulse on RTIPn/RRINGn. The output data at RDn or RDPn/RDNn are clocked out on the falling edges of RCLK when the CLKE input is low, or are clocked out on the rising edges of RCLK when CLKE is high. In Dual Rail Mode without clock recovery, these pins output the raw RZ sliced data. In this data recovery mode, the active polarity of RDPn/RDNn is determined by pin CLKE. When pin CLKE is low, RDPn/RDNn is active low. When pin CLKE is high, RDPn/RDNn is active high. In hardware mode, RDn or RDPn/RDNn will remain active during LOS. In host mode, these pins will either remain active or insert alarm indication signal (AIS) into the receive path, determined by bit AISE in register **GCF**. RDn or RDPn/RDNn is set into high-Z when the corresponding receiver is powered down.
RCLK0 RCLK1 RCLK2 RCLK3 RCLK4 RCLK5 RCLK6 RCLK7	O High-Z	39 32 78 71 110 103 6 143	P1 M1 M14 P14 A14 C14 C1 A1	**RCLKn: Receive Clock for Channel 0~7** In clock recovery mode, this pin outputs the recovered clock from signal received on RTIPn/RRINGn. The received data are clocked out of the device on the rising edges of RCLKn if pin CLKE is high, or on falling edges of RCLKn if pin CLKE is low. In data recovery mode, RCLKn is the output of an internal exclusive OR (XOR) which is connected with RDPn and RDNn. The clock is recovered from the signal on RCLKn. If Receiver n is powered down, the corresponding RCLKn is in high-Z.
MCLK	I	10	E1	**MCLK: Master Clock** This is an independent, free running reference clock. A clock of 2.048 MHz is supplied to this pin as the clock reference of the device for normal operation. In receive path, when MCLK is high, the device slices the incoming bipolar line signal into RZ pulse (Data Recovery mode). When MCLK is low, all the receivers are powered down, and the output pins RCLKn, RDPn and RDNn are switched to high-Z. In transmit path, the operation mode is decided by the combination of MCLK and TCLKn (see TCLKn pin description for details). **NOTE:** Wait state generation via RDY/$\overline{ACK}$ is not available if MCLK is not provided.
LOS0 LOS1 LOS2 LOS3 LOS4 LOS5 LOS6 LOS7	O	42 35 75 68 113 106 3 140	K4 K3 K12 K11 E11 E12 E3 E4	**LOSn: Loss of Signal Output for Channel 0~7** A high level on this pin indicates the loss of signal when there is no transition over a specified period of time or no enough ones density in the received signal. The transition will return to low automatically when there is enough transitions over a specified period of time with a certain ones density in the received signal. The LOS assertion and desertion criteria are described in 2.3.4 Loss of Signal (LOS) Detection.

Table-1 Pin Description (Continued)

<table>
<tr><th rowspan="2">Name</th><th rowspan="2">Type</th><th colspan="2">Pin No.</th><th rowspan="2">Description</th></tr>
<tr><th>TQFP144</th><th>PBGA160</th></tr>
<tr><td colspan="5">Hardware/Host Control Interface</td></tr>
<tr><td>MODE2</td><td>I
(Pulled to VDDIO/2)</td><td>11</td><td>E2</td><td>MODE2: Control Mode Select 2
The signal on this pin determines which control mode is selected to control the device:
<table>
<tr><th>MODE2</th><th>Control Interface</th></tr>
<tr><td>Low</td><td>Hardware Mode</td></tr>
<tr><td>VDDIO/2</td><td>Serial Host Interface</td></tr>
<tr><td>High</td><td>Parallel Host Interface</td></tr>
</table>
Hardware control pins include MODE[2:0], LP[7:0], CODE, CLKE, JAS and OE.
Serial host Interface pins include $\overline{CS}$, SCLK, SDI, SDO and $\overline{INT}$.
Parallel host Interface pins include $\overline{CS}$, A[4:0], D[7:0], $\overline{WR}$/DS, $\overline{RD}$/R/$\overline{W}$, ALE/$\overline{AS}$, $\overline{INT}$ and RDY/$\overline{ACK}$. The device supports multiple parallel host interface as follows (refer to MODE1 and MODE0 pin descriptions below for details):
<table>
<tr><th>MODE[2:0]</th><th>Host Interface</th></tr>
<tr><td>100</td><td>Non-multiplexed Motorola Mode Interface</td></tr>
<tr><td>101</td><td>Non-multiplexed Intel Mode Interface</td></tr>
<tr><td>110</td><td>Multiplexed Motorola Mode Interface</td></tr>
<tr><td>111</td><td>Multiplexed Intel Mode Interface</td></tr>
</table></td></tr>
<tr><td>MODE1</td><td>I</td><td>43</td><td>K2</td><td>MODE1: Control Mode Select 1
In parallel host mode, the parallel interface operates with separate address bus and data bus when this pin is low, and operates with multiplexed address and data bus when this pin is high.
In serial host mode or hardware mode, this pin should be grounded.</td></tr>
<tr><td>MODE0/CODE</td><td>I</td><td>88</td><td>H12</td><td>MODE0: Control Mode Select 0
In parallel host mode, the parallel host interface is configured for Motorola compatible hosts when this pin is low, or for Intel compatible hosts when this pin is high.

CODE: Line Code Rule Select
In hardware control mode, the HDB3 encoder/decoder is enabled when this pin is low, and AMI encoder/decoder is enabled when this pin is high. The selections affect all the channels.

In serial host mode, this pin should be grounded.</td></tr>
<tr><td>$\overline{CS}$/JAS</td><td>I
(Pulled to VDDIO/2)</td><td>87</td><td>J11</td><td>$\overline{CS}$: Chip Select (Active Low)
In host mode, this pin is asserted low by the host to enable host interface. A high to low transition must occur on this pin for each read/write operation and the level must not return to high until the operation is over.

JAS: Jitter Attenuator Select
In hardware control mode, this pin globally determines the Jitter Attenuator position:
<table>
<tr><th>JAS</th><th>Jitter Attenuator (JA) Configuration</th></tr>
<tr><td>Low</td><td>JA in transmit path</td></tr>
<tr><td>VDDIO/2</td><td>JA not used</td></tr>
<tr><td>High</td><td>JA in receive path</td></tr>
</table></td></tr>
</table>

Table-1 Pin Description (Continued)

Name	Type	Pin No.		Description
		TQFP144	PBGA160	
SCLK/ALE/$\overline{AS}$	I	86	J12	**SCLK: Shift Clock** In serial host mode, the signal on this pin is the shift clock for the serial interface. Data on pin SDO is clocked out on falling edges of SCLK if pin CLKE is high, or on rising edges of SCLK if pin CLKE is low. Data on pin SDI is always sampled on rising edges of SCLK. **ALE: Address Latch Enable** In parallel Intel multiplexed host mode, the address on AD[4:0] is sampled into the device on the falling edges of ALE (signals on AD[7:5] are ignored). In non-multiplexed host mode, ALE should be pulled high. **$\overline{AS}$: Address Strobe (Active Low)** In parallel Motorola multiplexed host mode, the address on AD[4:0] is latched into the device on the falling edges of $\overline{AS}$ (signals on AD[7:5] are ignored). In non-multiplexed host mode, $\overline{AS}$ should be pulled high. **NOTE**: This pin is ignored in hardware control mode.
$\overline{RD}$/R/$\overline{W}$	I	85	J13	**$\overline{RD}$: Read Strobe (Active Low)** In parallel Intel multiplexed or non-multiplexed host mode, this pin is active low for read operation. **R/$\overline{W}$: Read/Write Select** In parallel Motorola multiplexed or non-multiplexed host mode, the pin is active low for write operation and high for read operation. **NOTE**: This pin is ignored in hardware control mode.
SDI/$\overline{WR}$/$\overline{DS}$	I	84	J14	**SDI: Serial Data Input** In serial host mode, this pin input the data to the serial interface. Data on this pin is sampled on the rising edges of SCLK. **$\overline{WR}$: Write Strobe (Active Low)** In parallel Intel host mode, this pin is active low during write operation. The data on D[7:0] (in non-multiplexed mode) or AD[7:0] (in multiplexed mode) is sampled into the device on the rising edges of $\overline{WR}$. **$\overline{DS}$: Data Strobe (Active Low)** In parallel Motorola host mode, this pin is active low. During a write operation (R/$\overline{W}$ = 0), the data on D[7:0] (in non-multiplexed mode) or AD[7:0] (in multiplexed mode) is sampled into the device on the rising edges of $\overline{DS}$. During a read operation (R/$\overline{W}$ = 1), the data is driven to D[7:0] (in non-multiplexed mode) or AD[7:0] (in multiplexed mode) by the device on the rising edges of $\overline{DS}$. In parallel Motorola non-multiplexed host mode, the address information on the 5 bits of address bus A[4:0] are latched into the device on the falling edges of $\overline{DS}$. **NOTE**: This pin is ignored in hardware control mode.
SDO/RDY/$\overline{ACK}$	O	83	K14	**SDO: Serial Data Output** In serial host mode, the data is output on this pin. In serial write operation, SDO is in high impedance for the first 8 SCLK clock cycles and driven low for the remaining 8 SCLK clock cycles. In serial read operation, SDO is in high-Z only when SDI is in address/command byte. Data on pin SDO is clocked out of the device on the falling edges of SCLK if pin CLKE is high, or on the rising edges of SCLK if pin CLKE is low. **RDY: Ready Output** In parallel Intel host mode, the high level of this pin reports to the host that bus cycle can be completed, while low reports the host must insert wait states. **$\overline{ACK}$: Acknowledge Output (Active Low)** In parallel Motorola host mode, the low level of this pin indicates that valid information on the data bus is ready for a read operation or acknowledges the acceptance of the written data during a write operation.
$\overline{INT}$	O Open Drain	82	K13	**$\overline{INT}$: Interrupt (Active Low)** This is an open drain, active low interrupt output. Three sources may cause the interrupt . Refer to 2.18 Interrupt Handling for details.

Table-1 Pin Description (Continued)

<table>
<tr><th rowspan="2">Name</th><th rowspan="2">Type</th><th colspan="2">Pin No.</th><th rowspan="2">Description</th></tr>
<tr><th>TQFP144</th><th>PBGA160</th></tr>
<tr><td>LP7/D7/AD7
LP6/D6/AD6
LP5/D5/AD5
LP4/D4/AD4
LP3/D3/AD3
LP2/D2/AD2
LP1/D1/AD1
LP0/D0/AD0</td><td>I/O

High-Z</td><td>28
27
26
25
24
23
22
21</td><td>K1
J1
J2
J3
J4
H2
H3
G2</td><td>LPn: Loopback Select 7~0
In hardware control mode, pin LPn configures the corresponding channel in different loopback mode, as follows:
<table>
<tr><th>LPn</th><th>Loopback Configuration</th></tr>
<tr><td>Low</td><td>Remote Loopback</td></tr>
<tr><td>VDDIO/2</td><td>No loopback</td></tr>
<tr><td>High</td><td>Analog Loopback</td></tr>
</table>
Refer to 2.16 Loopback Mode for details.

Dn: Data Bus 7~0
In non-multiplexed host mode, these pins are the bi-directional data bus.

ADn: Address/Data Bus 7~0
In multiplexed host mode, these pins are the multiplexed bi-directional address/data bus.

In serial host mode, these pins should be grounded.</td></tr>
<tr><td>A4
MC3/A3
MC2/A2
MC1/A1
MC0/A0</td><td>I</td><td>12
13
14
15
16</td><td>F4
F3
F2
F1
G3</td><td>MCn: Performance Monitor Configuration 3~0
In hardware control mode, A4 must be connected to GND. MC[3:0] are used to select one transmitter or receiver of channel 1 to 7 for non-intrusive monitoring. Channel 0 is used as the monitoring channel. If a transmitter is monitored, signals on the corresponding pins TTIPn and TRINGn are internally transmitted to RTIP0 and RRING0. If a receiver is monitored, signals on the corresponding pins RTIPn and RRINGn are internally transmitted to RTIP0 and RRING0. The monitored is then output to RDP0 and RDN0 pins. In host mode operation, the signals monitored by channel 0 can be routed to TTIP0/RING0 by activating the remote loopback in this channel. Refer to 2.19 G.772 Monitoring for more details.

Performance Monitor Configuration determined by MC[3:0] is shown below. Note that if MC[2:0] = 000, the device is in normal operation of all the channels.
<table>
<tr><th>MC[3:0]</th><th>Monitoring Configuration</th></tr>
<tr><td>0000</td><td>Normal operation without monitoring</td></tr>
<tr><td>0001</td><td>Monitor Receiver 1</td></tr>
<tr><td>0010</td><td>Monitor Receiver 2</td></tr>
<tr><td>0011</td><td>Monitor Receiver 3</td></tr>
<tr><td>0100</td><td>Monitor Receiver 4</td></tr>
<tr><td>0101</td><td>Monitor Receiver 5</td></tr>
<tr><td>0110</td><td>Monitor Receiver 6</td></tr>
<tr><td>0111</td><td>Monitor Receiver 7</td></tr>
<tr><td>1000</td><td>Normal operation without monitoring</td></tr>
<tr><td>1001</td><td>Monitor Transmitter 1</td></tr>
<tr><td>1010</td><td>Monitor Transmitter 2</td></tr>
<tr><td>1011</td><td>Monitor Transmitter 3</td></tr>
<tr><td>1100</td><td>Monitor Transmitter 4</td></tr>
<tr><td>1101</td><td>Monitor Transmitter 5</td></tr>
<tr><td>1110</td><td>Monitor Transmitter 6</td></tr>
<tr><td>1111</td><td>Monitor Transmitter 7</td></tr>
</table>
An: Address Bus 4~0
When pin MODE1 is low, the parallel host interface operates with separate address and data bus. In this mode, the signal on this pin is the address bus of the host interface.</td></tr>
<tr><td>OE</td><td>I</td><td>114</td><td>E14</td><td>OE: Output Driver Enable
Pulling this pin low can drive all driver output into high-Z for redundancy application without external mechanical relays. In this condition, all other internal circuits remain active.</td></tr>
</table>

Table-1 Pin Description (Continued)

Name	Type	Pin No.		Description
		TQFP144	PBGA160	
CLKE	I	115	E13	**CLKE: Clock Edge Select** The signal on this pin determines the active edge of RCLKn and SCLK in clock recovery mode, or determines the active level of RDPn and RDNn in the data recovery mode. See 2.2 Clock Edges on page 14 for details.
				JTAG Signals
$\overline{TRST}$	I Pull-up	95	G12	**$\overline{TRST}$: JTAG Test Port Reset (Active Low)** This is the active low asynchronous reset to the JTAG Test Port. This pin has an internal pull-up resistor and it can be left open.
TMS	I Pull-up	96	F11	**TMS: JTAG Test Mode Select** The signal on this pin controls the JTAG test performance and is clocked into the device on the rising edges of TCK. This pin has an internal pull-up resistor and it can be left open.
TCK	I	97	F14	**TCK: JTAG Test Clock** This pin input the clock of the JTAG Test. The data on TDI and TMS are clocked into the device on the rising edges of TCK, while the data on TDO is clocked out of the device on the falling edges of TCK. This pin should be connected to GNDIO or VDDIO pin when unused.
TDO	O High-Z	98	F13	**TDO: JTAG Test Data Output** This pin output the serial data of the JTAG Test. The data on TDO is clocked out of the device on the falling edges of TCK. TDO is a high-Z output signal. It is active only when scanning of data is out. This pin should be left float when unused.
TDI	I Pull-up	99	F12	**TDI: JTAG Test Data Input** This pin input the serial data of the JTAG Test. The data on TDI is clocked into the device on the rising edges of TCK. This pin has an internal pull-up resistor and it can be left open.
				Power Supplies and Grounds
VDDIO	-	17 92	G1 G14	**3.3 V I/O Power Supply**
GNDIO	-	18 91	G4 G11	**I/O GND**
VDDT0 VDDT1 VDDT2 VDDT3 VDDT4 VDDT5 VDDT6 VDDT7	-	44 53 56 65 116 125 128 137	N4, P4 L4, M4 L11, M11 N11, P11 A11, B11 C11, D11 C4, D4 A4, B4	**3.3 V/5 V Power Supply for Transmitter Driver** All VDDT pins must be connected to 3.3 V or all VDDT must be connected to 5 V. It is not allowed to leave any of the VDDT pins open (not-connected) even if the channel is not used.
GNDT0 GNDT1 GNDT2 GNDT3 GNDT4 GNDT5 GNDT6 GNDT7	-	47 50 59 62 119 122 131 134	N6, P6 L6, M6 L9, M9 N9, P9 A9, B9 C9, D9 C6, D6 A6, B6	**Analog GND for Transmitter Driver**
VDDD VDDA	-	19 90	H1 H14	**3.3 V Digital/Analog Core Power Supply**

Table-1 Pin Description (Continued)

Name	Type	Pin No.		Description
		TQFP144	PBGA160	
GNDD GNDA	-	20 89	H4 H11	Digital/Analog Core GND
Others				
IC	O	93 94	G13 H13	**IC: Internal Connection** Internal use. Leave it float for normal operation.

2 FUNCTIONAL DESCRIPTION

2.1 OVERVIEW

The IDT82V2058 is a fully integrated octal short-haul line interface unit, which contains eight transmit and receive channels for use in E1 applications. The receiver performs clock and data recovery. As an option, the raw sliced data (no retiming) can be output to the system. Transmit equalization is implemented with low-impedance output drivers that provide shaped waveforms to the transformer, guaranteeing template conformance. A selectable jitter attenuator may be placed in the receive path or the transmit path. Moreover, multiple testing functions, such as error detection, loopback and JTAG boundary scan are also provided. The device is optimized for flexible software control through a serial or parallel host mode interface. Hardware control is also available. Figure-1 on page 1 shows one of the eight identical channels operation.

2.1.1 SYSTEM INTERFACE

The system interface of each channel can be configured to operate in different modes:

1. *Single rail interface with clock recovery.*
2. *Dual rail interface with clock recovery.*
3. *Dual rail interface with data recovery (that is, with raw data slicing only and without clock recovery).*

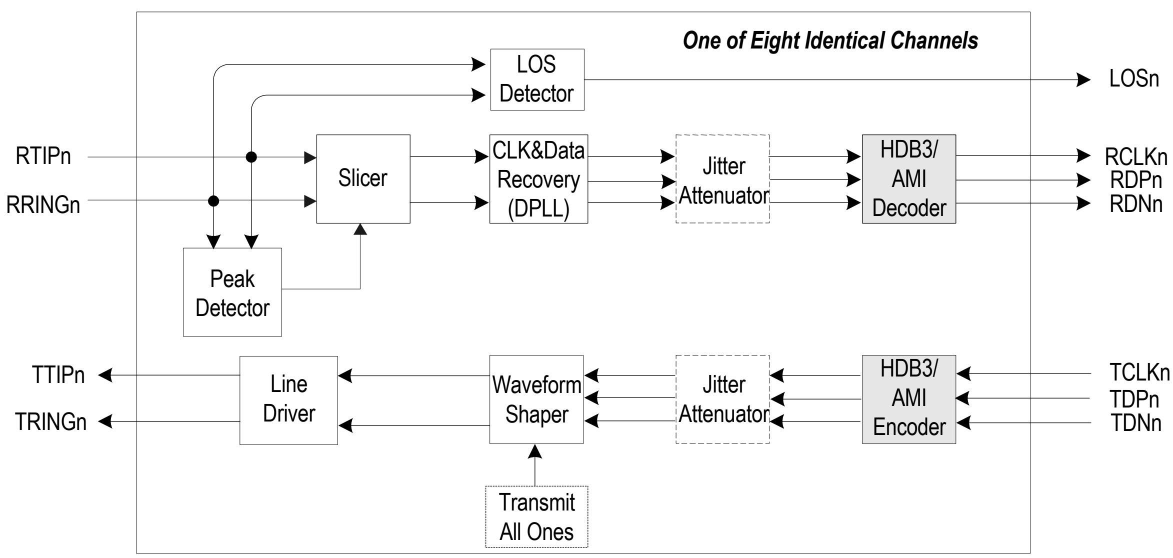
Each signal pin on system side has multiple functions depending on which operation mode the device is in.

The Dual Rail interface consists of TDPn[1], TDNn, TCLKn, RDPn, RDNn and RCLKn. Data transmitted from TDPn and TDNn appears on TTIPn and TRINGn at the line interface; data received from the RTIPn and RRINGn at the line interface are transferred to RDPn and RDNn while the recovered clock extracting from the received data stream outputs on RCLKn. In Dual Rail operation, the clock/data recovery mode is selectable. Dual Rail interface with clock recovery shown in Figure-4 is a default configuration mode. Dual Rail interface with data recovery is shown in Figure-5. Pin RDPn and RDNn, are raw RZ slice outputs and internally connected to an EXOR which is fed to the RCLKn output for external clock recovery applications.

In Single Rail mode, data transmitted from TDn appears on TTIPn and TRINGn at the line interface. Data received from the RTIPn and RRINGn at the line interface appears on RDn while the recovered clock extracting from the received data stream outputs on RCLKn. When the device is in single rail interface, the selectable AMI or HDB3 line encoder/decoder is available and any code violation in the received data will be indicated at the CVn pin. The Single Rail mode has 2 sub-modes: Single Rail Mode 1 and Single Rail Mode 2. Single Rail Mode 1, whose interface is composed of TDn, TCLKn, RDn, CVn and RCLKn, is realized by pulling pin TDNn high for more than 16 consecutive TCLK cycles. Single Rail Mode 2, whose interface is composed of TDn, TCLKn, RDn, CVn, RCLKn and BPVIn, is realized by setting bit CRS in register **e-CRS**[2] and bit SING in register **e-SING**. The difference between them is that, in the latter mode bipolar violation can be inserted via pin BPVIn if AMI line code is selected.

The configuration of the Hardware Mode System Interface is summarized in Table-2. The configuration of the Host Mode System Interface is summarized in Table-3.

1. The footprint 'n' (n = 0 - 7) indicates one of the eight channels.
2. The first letter 'e-' indicates expanded register.



Note: The grey blocks are bypassed and the dotted blocks are selectable.

Figure-4 Dual Rail Interface with Clock Recovery

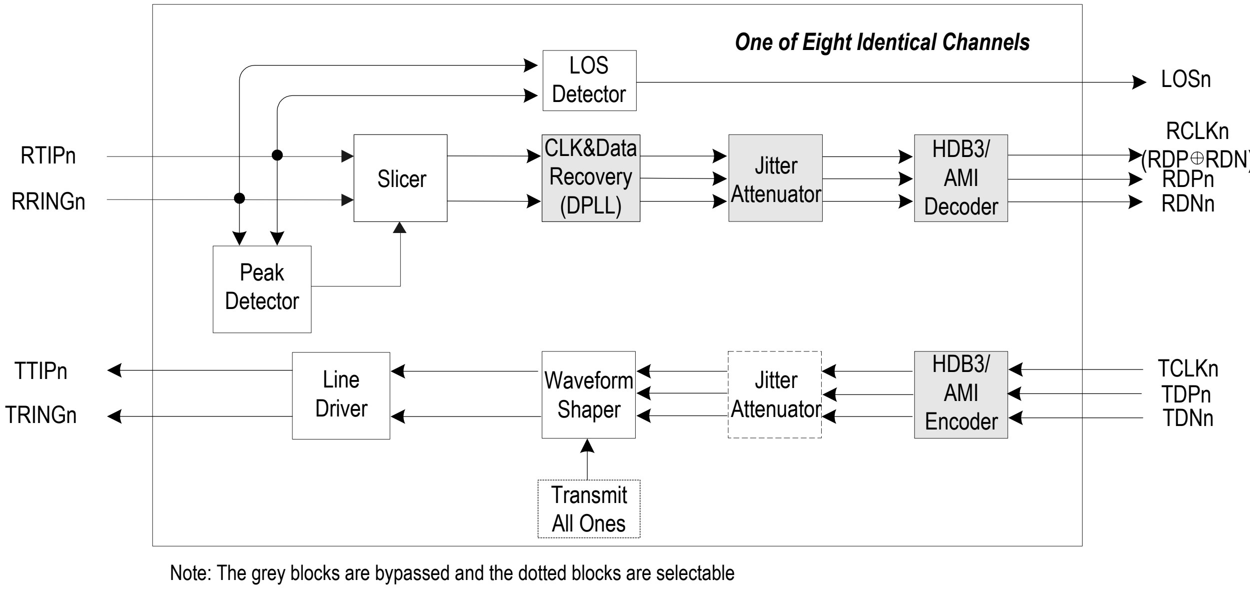


Figure-5 Dual Rail Interface with Data Recovery

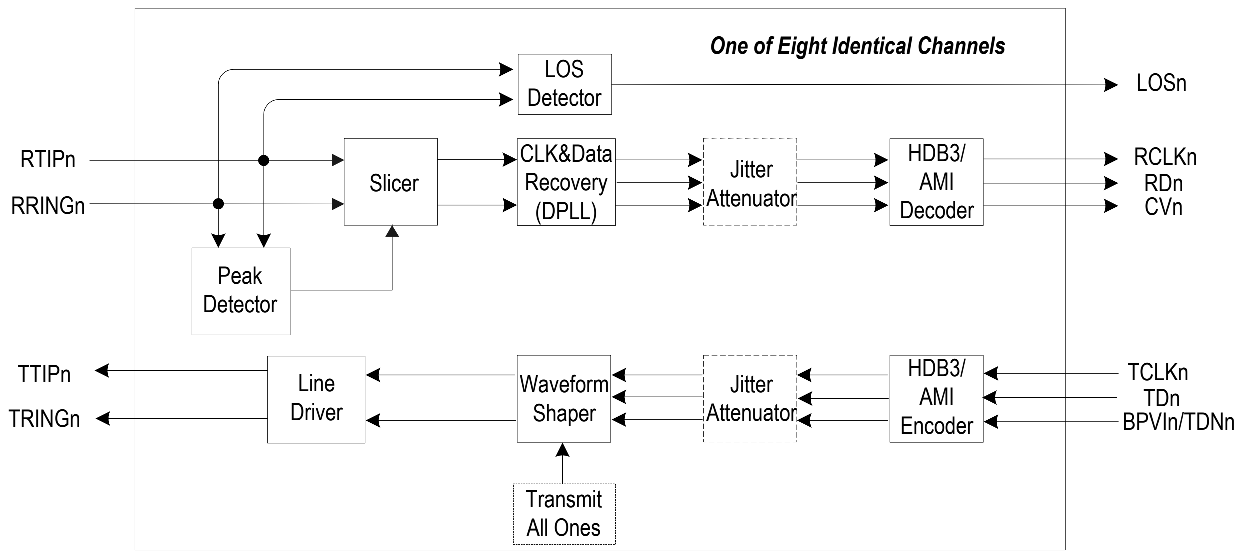


Figure-6 Single Rail Mode

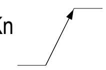
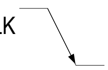
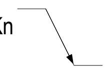
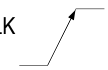
Table-2 System Interface Configuration (In Hardware Mode)

Pin MCLK	Pin TDNn	Interface
Clocked	High (≥ 16 MCLK)	Single Rail Mode 1
Clocked	Pulse	Dual Rail mode with Clock Recovery
High	Pulse	Dual Rail mode with Data Recovery. Receive just slices the incoming data. Transmit is determined by the status of TCLKn.
Low	Pulse	Receiver is powered down. Transmit is determined by the status of TCLKn.

Table-3 System Interface Configuration (In Host Mode)

Pin MCLK	Pin TDNn	CRSn in e-CRS	SINGn in e-SING	Interface
Clocked	High	0	0	Single Rail Mode 1
Clocked	Pulse	0	1	Single Rail Mode 2
Clocked	Pulse	0	0	Dual Rail mode with Clock Recovery
Clocked	Pulse	1	0	Dual Rail mode with Data Recovery. Receive just slices the incoming data. Transmit is determined by the status of TCLKn.
High	Pulse	-	-	Dual Rail mode with Data Recovery. Receive just slices the incoming data. Transmit is determined by the status of TCLKn.
Low	Pulse	-	-	Receiver is powered down. Transmit is determined by the status of TCLKn.

Table-4 Active Clock Edge and Active Level

Pin CLKE	Pin RDn/RDPn and CVn/RDNn			Pin SDO	
	Clock Recovery		Slicer Output		
High	RCLKn 	Active High	Active High	SCLK 	Active High
Low	RCLKn 	Active High	Active Low	SCLK 	Active High

2.2 CLOCK EDGES

The active edge of RCLKn and SCLK are selectable. If pin CLKE is high, the active edge of RCLKn is the rising edge, as for SCLK, that is falling edge. On the contrary, if CLKE is low, the active edge of RCLK is the falling edge and that of SCLK is rising edge. Pins RDn/RDPn, CVn/RDNn and SDO are always active high, and those output signals are clocked out on the active edge of RCLKn and SCLK respectively. See Table-4 Active Clock Edge and Active Level on page 14 for details. However, in dual rail mode without clock recovery, pin CLKE is used to set the active level for RDPn/RDNn raw slicing output: High for active high polarity and low for active low. It should be noted that data on pin SDI are always active high and are sampled on the rising edges of SCLK. The data on pin TDn/TDPn or BPVIn/TDNn are also always active high but are sampled on the falling edges of TCLKn, despite the level on CLKE.

2.3 RECEIVER

In receive path, the line signals couple into RRINGn and RTIPn via a transformer and are converted into RZ digital pulses by a data slicer. Adaptation for attenuation is achieved using an integral peak detector that sets the slicing levels. Clock and data are recovered from the received RZ digital pulses by a digital phase-locked loop that provides jitter accommodation. After passing through the selectable jitter attenuator, the recovered data are decoded using HDB3 or AMI line code rules and clocked out of pin RDn in single rail mode, or presented on RDPn/RDNn in an undecoded dual rail NRZ format. Loss of signal, alarm indication signal, line code violation and excessive zeros are detected. These various changes in status may be enabled to generate interrupts.

2.3.1 PEAK DETECTOR AND SLICER

The slicer determines the presence and polarity of the received pulses. In data recovery mode, the raw positive slicer output appears on RDPn while the negative slicer output appears on RDNn. In clock and data recovery mode, the slicer output is sent to Clock and Data Recovery circuit for abstracting retimed data and optional decoding. The slicer circuit has a built-in peak detector from which the slicing threshold is derived. The slicing threshold is default to 50% (typical) of the peak value.

Signals with an attenuation of up to 12 dB (from 2.4 V) can be recovered by the receiver. To provide immunity from impulsive noise, the peak detectors are held above a minimum level of 0.150 V typically, despite the received signal level.

2.3.2 CLOCK AND DATA RECOVERY

The Clock and Data Recovery is accomplished by Digital Phase Locked Loop (DPLL). The DPLL is clocked 16 times of the received clock rate, i.e. 32.768 MHz in E1 mode. The recovered data and clock from DPLL is then sent to the selectable Jitter Attenuator or decoder for further processing.

The clock recovery and data recovery mode can be selected on a per channel basis by setting bit CRSn in register **e-CRS**. When bit CRSn is defaulted to '0', the corresponding channel operates in data and clock recovery mode. The recovered clock is output on pin RCLKn and re-timed NRZ data are output on pin RDPn/RDNn in dual rail mode or on RDn in single rail mode. When bit CRSn is set to '1', dual rail mode with data recovery is enabled in the corresponding channel and the clock recovery is bypassed. In this condition, the analog line signals are converted to RZ digital bit streams on the RDPn/RDNn pins and internally connected to an EXOR which is fed to the RCLKn output for external clock recovery applications.

If MCLK is pulled high, all the receivers will enter the dual rail mode with data recovery. In this case, register **e-CRS** is ignored.

2.3.3 HDB3/AMI LINE CODE RULE

Selectable HDB3 and AMI line coding/decoding is provided when the device is configured in single rail mode. HDB3 rules is enabled by setting bit CODE in register **GCF** to ‘0’ or pulling pin CODE low. AMI rule is enabled by setting bit CODE in register **GCF** to ‘1’ or pulling pin CODE high. The settings affect all eight channels.

Individual line code rule selection for each channel, if needed, is available by setting bit SINGn in register **e-SING** to ‘1’ (to activate bit CODEn in register **e-CODE**) and programming bit CODEn to select line code rules in the corresponding channel: ‘0’ for HDB3, while ‘1’ for AMI. In this case, the value in bit CODE in register **GCF** or pin CODE for global control is unaffected in the corresponding channel and only affect in other channels.

In dual rail mode, the decoder/encoder are bypassed. Bit CODE in register **GCF**, bit CODEn in register **e-CODE** and pin CODE are ignored.

The configuration of the line code rule is summarized in Table-5.

2.3.4 LOSS OF SIGNAL (LOS) DETECTION

The Loss of Signal Detector monitors the amplitude and density of the received signal on receiver line before the transformer (measured on port A, B shown in Figure-10). The loss condition is reported by pulling pin LOSn high. At the same time, LOS alarm registers track LOS condition. When LOS is detected or cleared, an interrupt will generate if not masked. In host mode, the detection supports ITU G.775 and ETSI 300 233. In hardware mode, it supports the ITU G.775.

Table-6 summarizes the conditions of LOS in clock recovery mode.

During LOS, the RDPn/RDNn continue to output the sliced data when bit AISE in register **GCF** is set to ‘0’ or output all ones as AIS (alarm indication signal) when bit AISE is set to ‘1’. The RCLKn is replaced by MCLK only if the bit AISE is set.

Table-5 Configuration of the Line Code Rule

Hardware Mode	
CODE	**Line Code Rule**
Low	All channels in HDB3
High	All channels in AMI

Host Mode			
CODE in GCF	**CODEn in e-CODE**	**SINGn in e-SING**	**Line Code Rule**
0	0/1	0	All channels in HDB3
0	0	1	
1	0/1	0	All channels in AMI
1	1	1	
0	1	1	CHn in AMI
1	0	1	CHn in HDB3

Table-6 LOS Condition in Clock Recovery Mode

		Standard		Signal on LOSn
		G.775	**ETSI 300 233**	
LOS Detected	**Continuous Intervals**	32	2048 (1 ms)	High
	Amplitude[1]	below typical 200 mVp	below typical 200 mVp	
LOS Cleared	**Density**	12.5% (4 marks in a sliding 32-bit period) with no more than 15 continuous zeros	12.5% (4 marks in a sliding 32-bit period) with no more than 15 continuous zeros	Low
	Amplitude[1]	exceed typical 250 mVp	exceed typical 250 mVp	

1. LOS levels at device (RTIPn, RRINGn) with all ones signal. For more detail regarding the LOS parameters, please refer to Receiver Characteristics on page 42.

2.3.5 ALARM INDICATION SIGNAL (AIS) DETECTION

Alarm Indication Signal is available only in host mode with clock recovery, as shown in Table-7.

2.3.6 ERROR DETECTION

The device can detect excessive zeros, bipolar violation and HDB3 code violation, as shown in Figure-7 and Figure-8. All the three kinds of errors are reported in both host mode and hardware mode with HDB3 line code rule used. In host mode, the **e-CZER** and **e-CODV** are used to determine whether excessive zeros and code violation are reported respectively. When the device is configured in AMI decoding mode, only bipolar violation can be reported.

The error detection is available only in single rail mode in which the pin CVn/RDNn is used as error report output (CVn pin).

The configuration and report status of error detection are summarized in Table-8.

Table-7 AIS Condition

	ITU G.775 (Register LAC defaulted to ‘0’)	**ETSI 300 233 (Register LAC set to ‘1’)**
AIS Detected	Less than 3 zeros contained in each of two consecutive 512-bit stream are received	Less than 3 zeros contained in a 512-bit stream are received
AIS Cleared	3 or more zeros contained in each of two consecutive 512-bit stream are received	3 or more zeros contained in a 512-bit stream are received

Table-8 Error Detection

Hardware Mode	
Line Code	**Pin CVn Reports**
AMI	Bipolar Violation
HDB3	Bipolar Violation + Code Violation + Excessive Zeros

Host Mode			
Line Code	**CODVn in e-CODV**	**CZERn in e-CZER**	**Pin CVn Reports**
AMI	-	-	Bipolar Violation
HDB3	0	0	Bipolar Violation + Code Violation
	0	1	Bipolar Violation + Code Violation + Excessive Zeros
	1	0	Bipolar Violation
	1	1	Bipolar Violation + Excessive Zeros

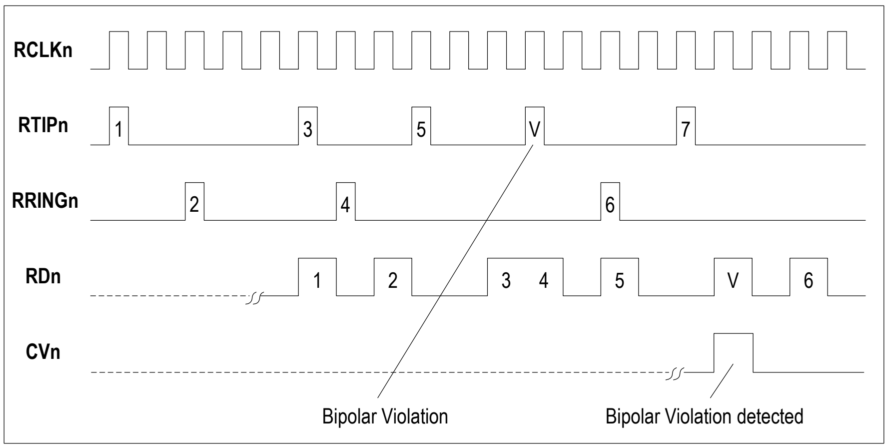


Figure-7 AMI Bipolar Violation

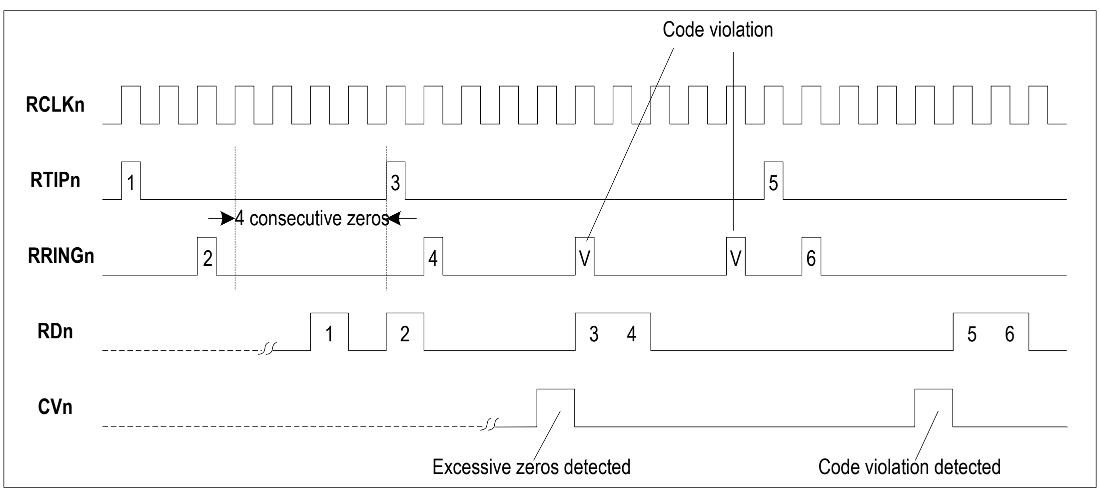


Figure-8 HDB3 Code Violation & Excessive Zeros

2.4 TRANSMITTER

In transmit path, data in NRZ format are clocked into the device on TDn and encoded by AMI or HDB3 line code rules when single rail mode is configured or pre-encoded data in NRZ format are input on TDPn and TDNn when dual rail mode is configured. The data are sampled into the device on falling edges of TCLKn. Jitter attenuator, if enabled, is provided with a FIFO through which the data to be transmitted are passing. A low jitter clock is generated by an integral digital phase-locked loop and is used to read data from the FIFO. The shape of the pulses should meet the E1 pulse template after the signal passes through different cable lengths or types. Bipolar violation, for diagnosis, can be inserted on pin BPVIn if AMI line code rule is enabled.

2.4.1 WAVEFORM SHAPER

E1 pulse template, specified in ITU-T G.703, is shown in Figure-9. The device has built-in transmit waveform templates for cable of 75 Ω or 120 Ω.

The built-in waveform shaper uses an internal high frequency clock which is 16XMCLK as the clock reference. This function will be bypassed when MCLK is unavailable.

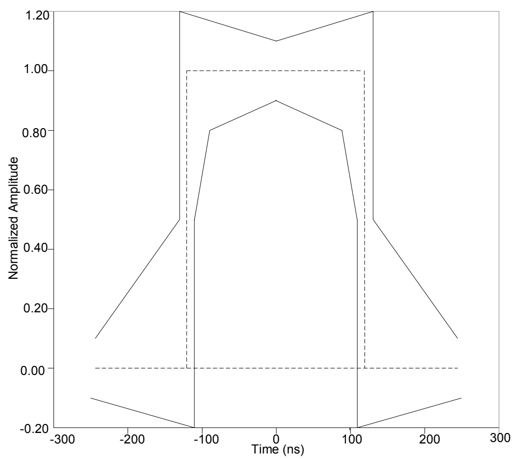


Figure-9 CEPT Waveform Template

2.4.2 BIPOLAR VIOLATION INSERTION

When configured in Single Rail Mode 2 with AMI line code enabled, pin TDNn/BPVIn is used as BPVI input. A low-to-high transition on this pin inserts a bipolar violation on the next available mark in the transmit data stream. Sampling occurs on the falling edges of TCLK. But in TAOS (Transmit All Ones) with Analog Loopback and Remote Loopback, the BPVI is disabled. In TAOS with Digital Loopback, the BPVI is looped back to the system side, so the data to be transmitted on TTIPn and TRINGn are all ones with no bipolar violation.

2.5 JITTER ATTENUATOR

The jitter attenuator can be selected to work either in transmit path or in receive path or not used. The selection is accomplished by setting pin JAS in hardware mode or configuring bits JACF[1:0] in register **GCF** in host mode, which affects all eight channels.

For applications which require line synchronization, the line clock needed to be extracted for the internal synchronization, the jitter attenuator is set in the receive path. Another use of the jitter attenuator is to provide clock smoothing in the transmit path for applications such as synchronous/asynchronous demultiplexing applications. In these applications, TCLK will have an instantaneous frequency that is higher than the nominal E1 data rate and in order to set the average long-term TCLK frequency within the transmit line rate specifications, periods of TCLK are suppressed (gapped).

The jitter attenuator integrates a FIFO which can accommodate a gapped TCLK. In host mode, the FIFO length can be 32 X 2 or 64 X 2 bits by programming bit JADP in **GCF**. In hardware mode, it is fixed to 64 X 2 bits. The FIFO length determines the maximum permissible gap width (see Table-9 Gap Width Limitation). Exceeding these values will cause FIFO overflow or underflow. The data is 16 or 32 bits' delay through the jitter attenuator in the corresponding transmit or receive path. The constant delay feature is crucial for the applications requiring "hitless" switching.

Table-9 Gap Width Limitation

FIFO Length	Max. Gap Width
64 bit	56 UI
32 bit	28 UI

In host mode, bit JABW in GCF determines the jitter attenuator 3 dB corner frequency (fc). In hardware mode, the fc is fixed to 1.7 Hz. Generally, the lower the fc is, the higher the attenuation. However, lower fc comes at the expense of increased acquisition time. Therefore, the optimum fc is to optimize both the attenuation and the acquisition time. In addition, the longer FIFO length results in an increased throughput delay and also influences the 3 dB corner frequency. Generally, it's recommended to use the lower corner frequency and the shortest FIFO length that can still meet jitter attenuation requirements.

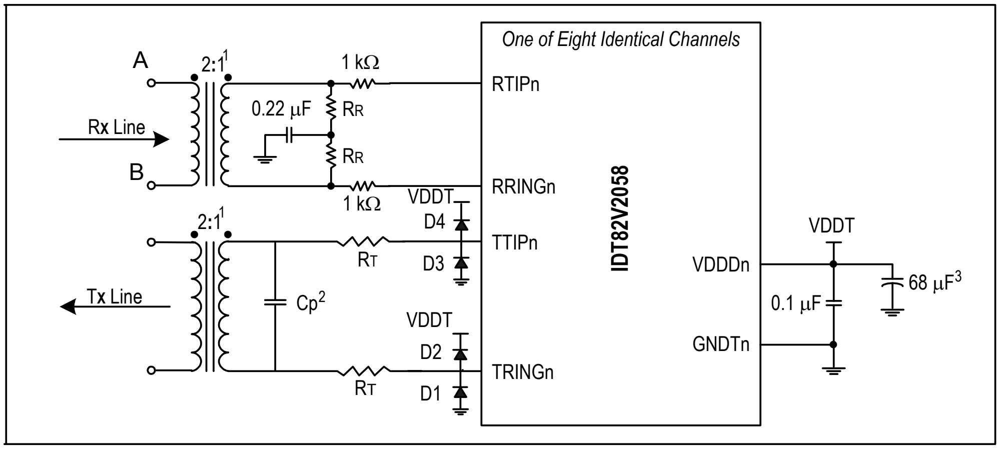
The output jitter meets ITU-T G.736, ITU-T G.742, ITU-T G.783 and ETSI CTR 12/13.

2.6 LINE INTERFACE CIRCUITRY

The transmit and receive interface RTIPn/RRINGn and TTIPn/TRINGn connections provide a matched interface to the cable. Figure-10 shows the appropriate external components to connect with the cable for one transmit/receive channel. Table-10 summarizes the component values based on the specific application.

Table-10 External Components Values

Component	75 Ω Coax	120 Ω Twisted Pair
R_T	9.5 Ω ± 1%	9.5 Ω ± 1%
R_R	9.31 Ω ± 1%	15 Ω ± 1%
Cp	2200 pF	
D1 - D4	Nihon Inter Electronics - EP05Q03L, 11EQS03L, EC10QS04, EC10QS03L; Motorola - MBR0540T1	



NOTE:
1. Pulse T1124 transformer is recommended to be used in Standard (STD) operating temperature range (0°C to 70°C), while Pulse T1114 transformer is recommended to be used in Extended (EXT) operating temperature range is -40°C to +85°C. See Transformer Specifications Table for details.
2. Typical value. Adjust for actual board parasitics to obtain optimum return loss.
3. Common decoupling capacitor for all VDDT and GNDT pins. One per chip.

Figure-10 External Transmit/Receive Line Circuitry

2.7 TRANSMIT DRIVER POWER SUPPLY

All transmit driver power supplies must be 5.0 V or 3.3 V.

Despite the power supply voltage, the 75 Ω/120 Ω lines are driven through a pair of 9.5 Ω series resistors and a 1:2 transformer.

Table-11 Transformer Specifications(1)

Electrical Specification @ 25°C										
Part No.		Turns Ratio (Pri: sec ± 2%)		OCL @ 25°C (mH MIN)		L_L (µH MAX)		$C_{W/W}$ (pF MAX)		Package/Schematic
STD Temp.	EXT Temp.	Transmit	Receive	Transmit	Receive	Transmit	Receive	Transmit	Receive	
T1124	T1114	1:2CT	1CT:2	1.2	1.2	.6	.6	35	35	TOU/3

1. Pulse T1124 transformer is recommended to be used in Standard (STD) operating temperature range (0°C to 70°C), while Pulse T1114 transformer is recommended to be used in Extended (EXT) operating temperature range is -40°C to +85°C.

2.8 POWER DRIVER FAILURE MONITOR

An internal power Driver Failure Monitor (DFMON), parallel connected with TTIPn and TRINGn, can detect short circuit failure between TTIPn and TRINGn pins. Bit SCPB in register **GCF** decides whether the output driver short circuit protection is enabled. When the short circuit protection is enabled, the driver output current is limited to a typical value: 180 mAp. Also, register **DF**, **DFI** and **DFM** will be available. When DFMON will detect a short circuit, register **DF** will be set. With a short circuit failure detected and short circuit protection enabled, register **DFI** will be set and an interrupt will be generated on pin $\overline{INT}$.

2.9 TRANSMIT LINE SIDE SHORT CIRCUIT FAILURE DETECTION

A pair of 9.5 Ω serial resistors connect with TTIPn and TRINGn pins and limit the output current. In this case, the output current is a limited value which is always lower than the typical line short circuit current 180 mAp, even if the transmit line side is shorted.

Refer to Table-10 External Components Values for details.

2.10 LINE PROTECTION

In transmit side, the Schottky diodes D1~D4 are required to protect the line driver and improve the design robustness. In receive side, the series resistors of 1 kΩ are used to protect the receiver against current surges coupled in the device. The series resistors do not affect the receiver sensitivity, since the receiver impedance is as high as 120 kΩ typically.

2.11 HITLESS PROTECTION SWITCHING (HPS)

The IDT82V2058 transceivers include an output driver with high-Z feature for E1 redundancy applications. This feature reduces the cost of redundancy protection by eliminating external relays. Details of HPS are described in relative Application Note.

2.12 SOFTWARE RESET

Writing register **RS** will cause software reset by initiating about 1 µs reset cycle. This operation set all the registers to their default value.

2.13 POWER ON RESET

During power up, an internal reset signal sets all the registers to default values. The power-on reset takes at least 10 µs, starting from when the power supply exceeds 2/3 VDDA.

2.14 POWER DOWN

Each transmit channel will be powered down by pulling pin TCLKn low for more than 64 MCLK cycles (if MCLK is available) or about 30 µs (if MCLK is not available). In host mode, each transmit channel will also be powered down by setting bit TPDNn in register **e-TPDN** to ‘1’.

All the receivers will be powered down when MCLK is low. When MCLK is clocked or high, setting bit RPDNn in register **e-RPDN** to ‘1’ will configure the corresponding receiver to be powered down.

2.15 INTERFACE WITH 5 V LOGIC

The IDT82V2058 can interface directly with 5 V TTL family devices. The internal input pads are tolerant to 5 V output from TTL and CMOS family devices.

2.16 LOOPBACK MODE

The device provides four different diagnostic loopback configurations: Digital Loopback, Analog Loopback, Remote Loopback and Dual Loopback. In host mode, these functions are implemented by programming the registers **DLB**, **ALB** and **RLB** respectively. In hardware mode, only Analog Loopback and Remote Loopback can be selected by pin LPn.

2.16.1 DIGITAL LOOPBACK

By programming the bits of register **DLB**, each channel of the device can be configured in Local Digital Loopback. In this configuration, the data and clock to be transmitted, after passing the encoder, are looped back to Jitter Attenuator (if enabled) and decoder in the receive path, then output on RCLKn, RDn/RDPn and CVn/RDNn. The data to be transmitted are still output on TTIPn and TRINGn while the data received on RTIPn and RRINGn are ignored. The Loss Detector is still in use. Figure-11 shows the process.

During Digital Loopback, the received signal on the receive line is still monitored by the LOS Detector (See 2.3.4 Loss of Signal (LOS) Detection for details). In case of a LOS condition and AIS insertion enabled, all ones signal will be output on RDPn/RDNn. With ATAO enabled, all ones signal will be also output on TTIPn/TRINGn. AIS insertion can be enabled by setting AISE bit in register **GCF** and ATAO can be enabled by setting register **ATAO** (default disabled).

2.16.2 ANALOG LOOPBACK

By programming the bits of register **ALB** or pulling pin LPn high, each channel of the device can be configured in Analog Loopback. In this configuration, the data to be transmitted output from the line driver are internally looped back to the slicer and peak detector in the receive path and output on RCLKn, RDn/RDPn and CVn/RDNn. The data to be transmitted are still output on TTIPn and TRINGn while the data received on RTIPn and RRINGn are ignored. The LOS Detector (See 2.3.4 Loss of Signal (LOS) Detection for details) is still in use and monitors the internal looped back data. If a LOS condition on TDPn/TDNn is expected during Analog Loopback, ATAO should be disabled (default). Figure-12 shows the process.

The TTIPn and RTIPn, TRINGn and RRINGn cannot be connected directly to do the external analog loopback test. Line impedance loading is required to conduct the external analog loopback test.

2.16.3 REMOTE LOOPBACK

By programming the bits of register **RLB** or pulling pin LPn low, each channel of the device can be set in Remote Loopback. In this configuration, the data and clock recovered by the clock and data recovery circuits are looped to waveform shaper and output on TTIPn and TRINGn. The jitter attenuator is also included in loopback when enabled in the transmit or receive path. The received data and clock are still output on RCLKn, RDn/RDPn and CVn/RDNn while the data to be transmitted on TCLKn, TDn/TDPn and BPVIn/TDNn are ignored. The LOs Detector is still in use. Figure-13 shows the process.

2.16.4 DUAL LOOPBACK

Dual Loopback mode is set by setting bit DLBn in register **DLB** and bit RLBn in register **RLB** to ‘1’. In this configuration, after passing the encoder, the data and clock to be transmitted are looped back to decoder directly and output on RCLKn, RDn/RDPn and CVn/RDNn. The recovered data from RTIPn and RRINGn are looped back to waveform shaper through JA (if selected) and output on TTIPn and TRINGn. The LOS Detector is still in use. Figure-14 shows the process.

2.16.5 TRANSMIT ALL ONES (TAOS)

In hardware mode, the TAOS mode is set by pulling pin TCLKn high for more than 16 MCLK cycles. In host mode, TAOS mode is set by programming register **TAO**. In addition, automatic TAOS signals are inserted by setting register **ATAO** when Loss of Signal occurs. Note that the TAOS generator adopts MCLK as a timing reference. In order to assure that the output frequency is within specified limits, MCLK must have the applicable stability.

The TAOS mode, the TAOS mode with Digital Loopback and the TAOS mode with Analog Loopback are shown in Figure-15, Figure-16 and Figure-17.

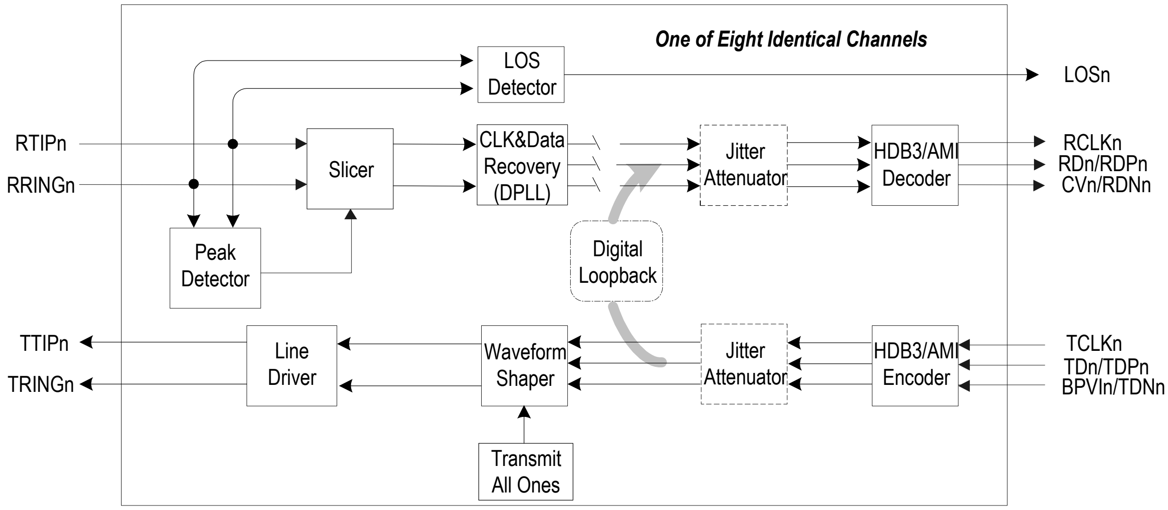


Figure-11 Digital Loopback

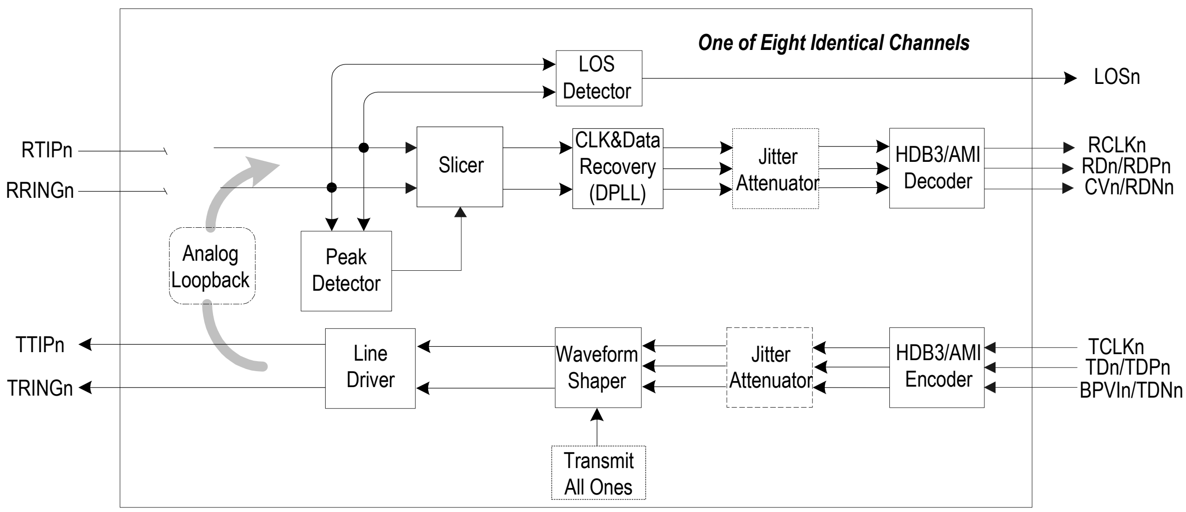


Figure-12 Analog Loopback

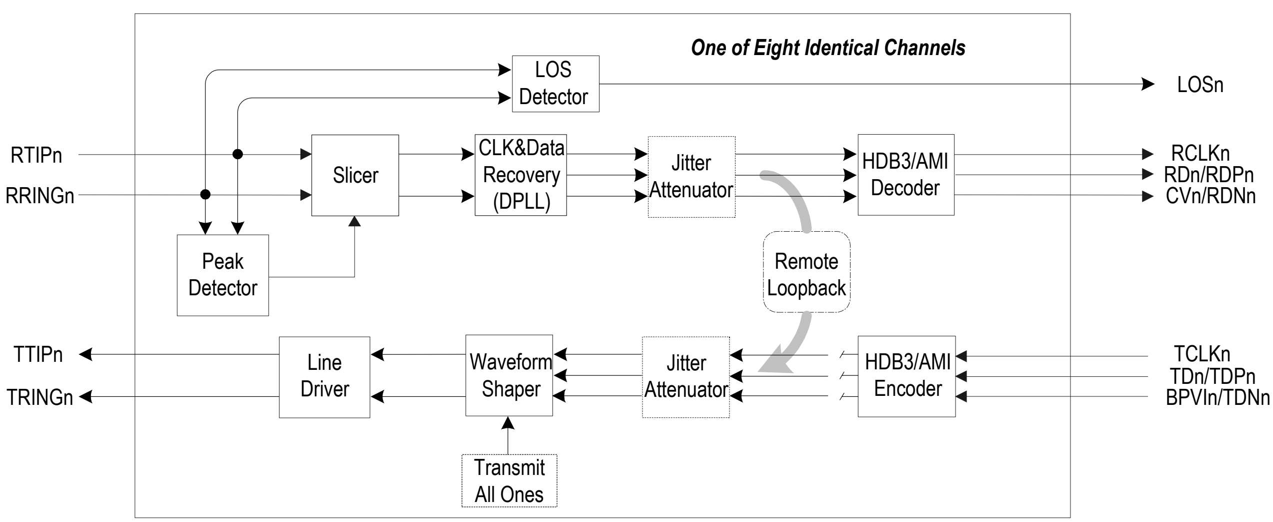


Figure-13 Remote Loopback

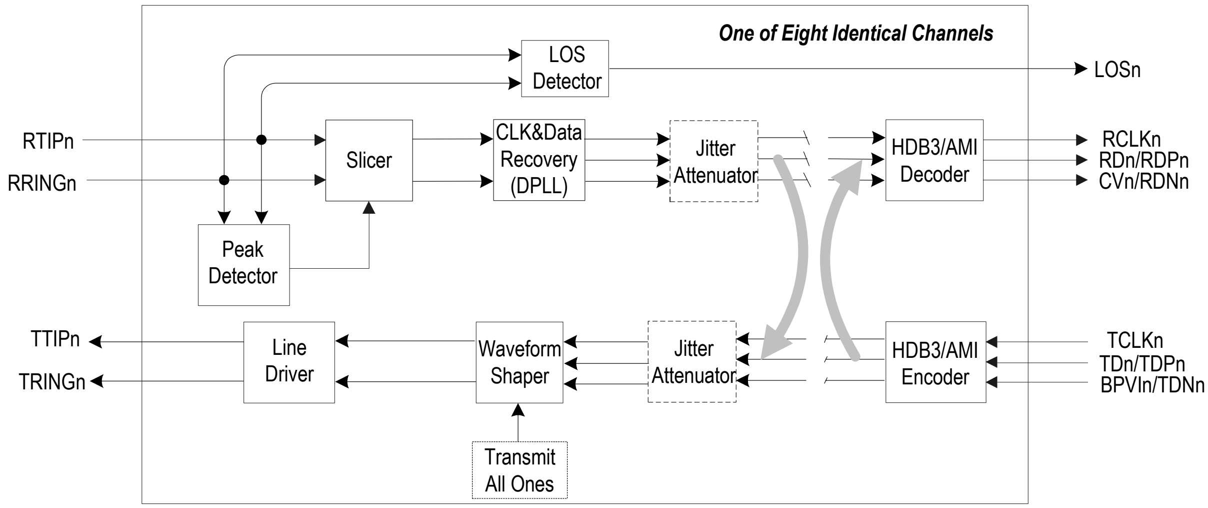


Figure-14 Dual Loopback

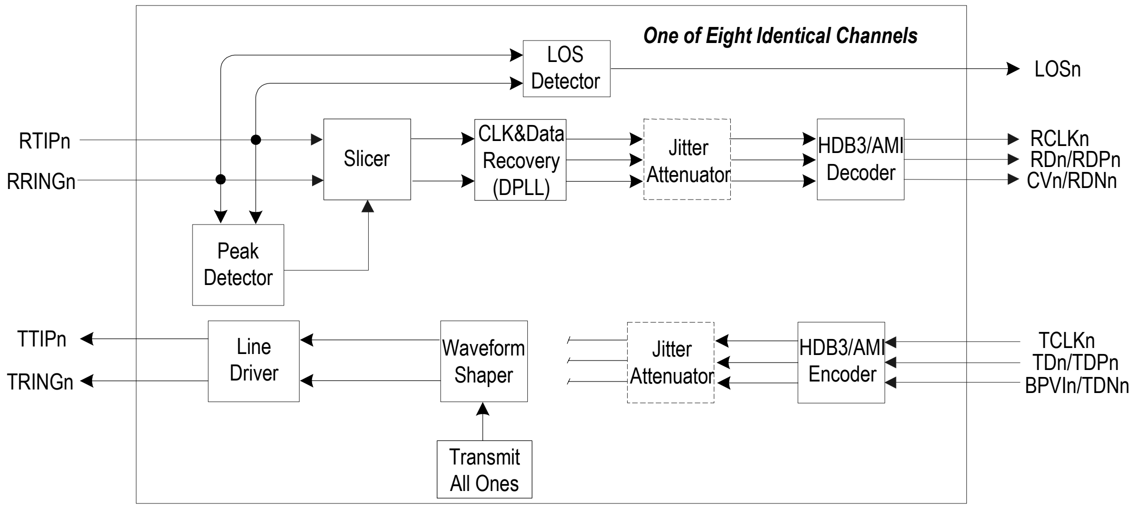


Figure-15 TAOS Data Path

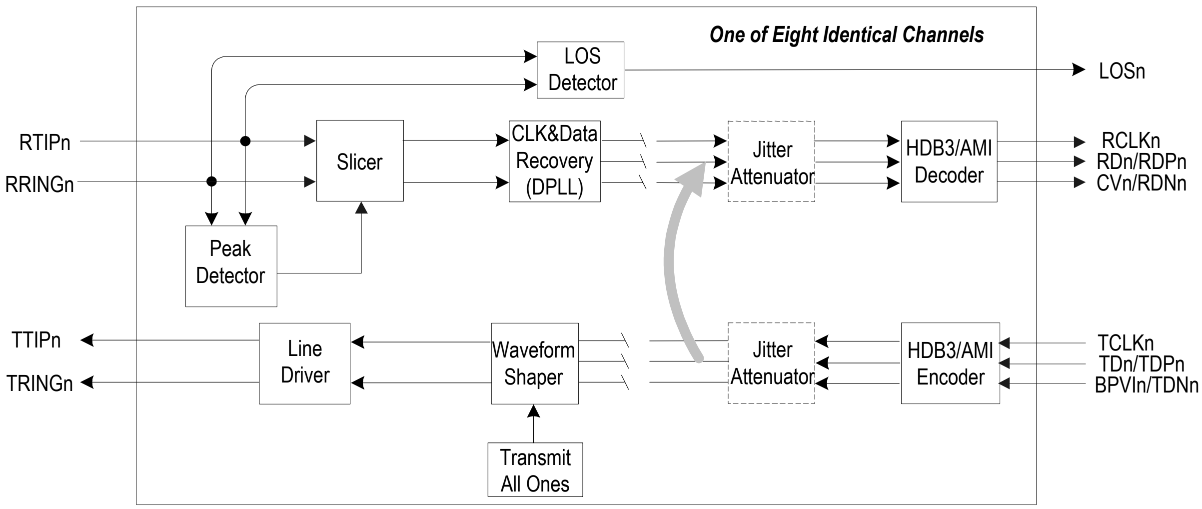


Figure-16 TAOS with Digital Loopback

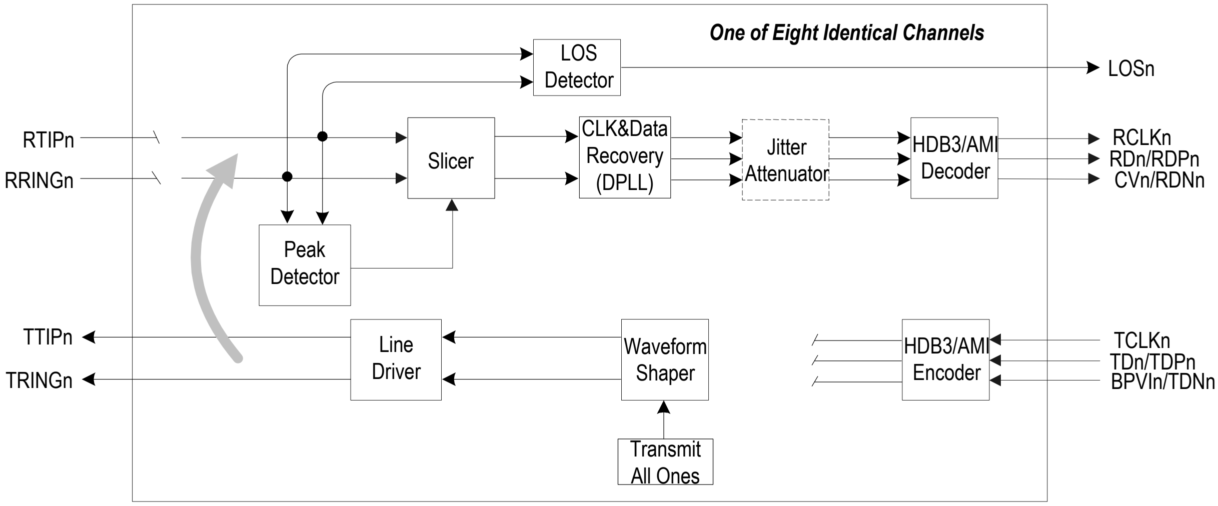


Figure-17 TAOS with Analog Loopback

2.17 HOST INTERFACE

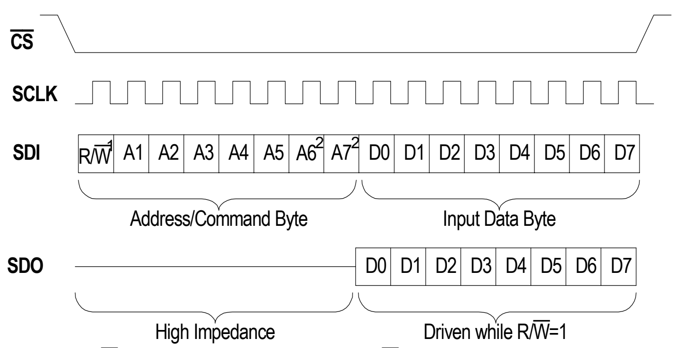
The host interface provides access to read and write the registers in the device. The interface consists of serial host interface and parallel host interface. By pulling pin MODE2 to VDDIO/2 or high, the device can be set to work in serial mode and in parallel mode respectively.

2.17.1 PARALLEL HOST INTERFACE

The interface is compatible with Motorola and Intel host. Pins MODE1 and MODE0 are used to select the operating mode of the parallel host interface. When pin MODE1 is pulled low, the host uses separate address bus and data bus. When high, multiplexed address/data bus is used. When pin MODE0 is pulled low, the parallel host interface is configured for Motorola compatible hosts. When pin MODE0 is pulled high, the parallel host interface is configured for Intel compatible hosts. See Table-1 Pin Description for more details. The host interface pins in each operation mode is tabulated in Table-12:

Table-12 Parallel Host Interface Pins

MODE[2:0]	Host Interface	Generic Control, Data and Output Pin
100	Non-multiplexed Motorola interface	CS, ACK, DS, R/W, AS, A[4:0], D[7:0], INT
101	Non-multiplexed Intel interface	CS, RDY, WR, RD, ALE, A[4:0], D[7:0], INT
110	Multiplexed Motorola interface	CS, ACK, DS, R/W, AS, AD[7:0], INT
111	Multiplexed Intel interface	CS, RDY, WR, RD, ALE, AD[7:0], INT



1. While R/W=1, read from IDT82V2058; While R/W=0, write to IDT82V2058.
2. Ignored.

Figure-18 Serial Host Mode Timing

2.17.2 SERIAL HOST INTERFACE

By pulling pin MODE2 to VDDIO/2, the device operates in the serial host Mode. In this mode, the registers are accessible through a 16-bit word which contains an 8-bit command/address byte (bit R/W and 5-address-bit A1~A5, A6 and A7 bits are ignored) and a subsequent 8-bit data byte (D7~D0), as shown in Figure-18. When bit R/W is set to '1', data is read out from pin SDO. When bit R/W is set to '0', data on pin SDI is written into the register whose address is indicated by address bits A5~A1. See Figure-18 Serial Host Mode Timing.

2.18 INTERRUPT HANDLING

2.18.1 INTERRUPT SOURCES

There are three kinds of interrupt sources:

1. *Status change in register **LOS**. The analog/digital loss of signal detector continuously monitors the received signal to update the specific bit in register **LOS** which indicates presence or absence of a LOS condition.*
2. *Status change in register **DF**. The automatic power driver circuit continuously monitors the output drivers signal to update the specific bit in register **DFM** which indicates presence or absence of an output driver short circuit condition.*
3. *Status change in register **AIS**. The AIS detector monitors the received signal to update the specific bit in register **AIS** which indicates presence or absence of a AIS condition.*

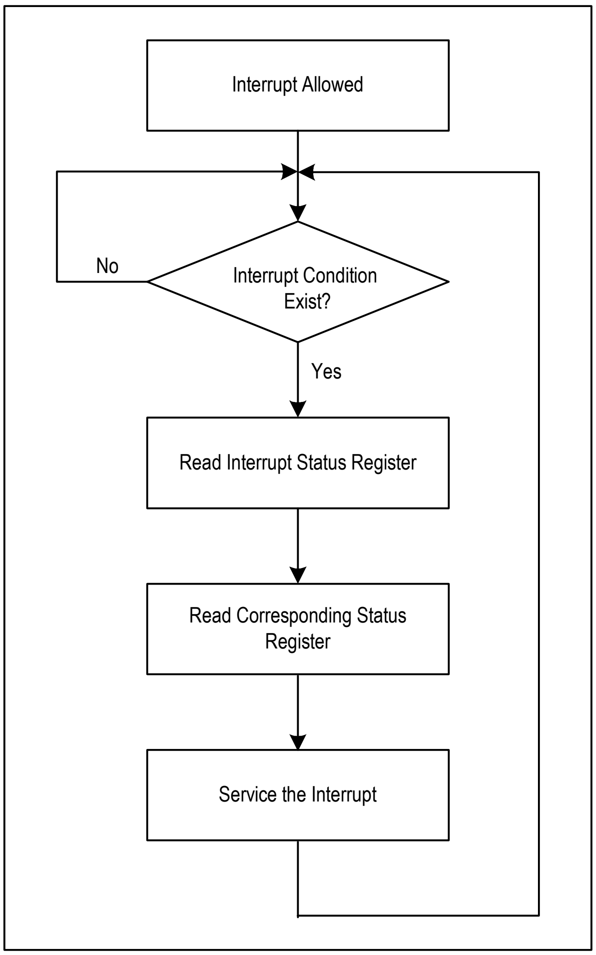


Figure-19 Interrupt Service Routine

2.18.2 INTERRUPT ENABLE

The IDT82V2058 provides a latched interrupt output ($\overline{INT}$) and the four kinds of interrupts are all reported by this pin. When the Interrupt Mask register (**LOSM**, **DFM** and **AISM**) is set to '1', the Interrupt Status register (**LOSI**, **DFI** and **AISI**) is enabled respectively. Whenever there is a transition ('0' to '1' or '1' to '0') in the corresponding status register, the Interrupt Status register will change into '1', which means an interrupt occurs, and there will be a high to low transition on $\overline{INT}$ pin. An external pull-up resistor of approximately 10 kΩ is required to support the wire-OR operation of $\overline{INT}$. When any of the three Interrupt Mask registers is set to '0' (the power-on default value is '0'), the corresponding Interrupt Status register is disabled and the transition on status register is ignored.

2.18.3 INTERRUPT CLEARING

When an interrupt occurs, the Interrupt Status registers: **LOSI**, **DFI** and **AISI**, are read to identify the interrupt source. These registers will be cleared to '0' after the corresponding status registers: **LOS**, **DF** and **AIS** are read. The Status registers will be cleared once the corresponding conditions are met.

Pin $\overline{INT}$ is pulled high when there is no pending interrupt left. The interrupt handling in the interrupt service routine is showed in Figure-19.

2.19 G.772 MONITORING

The eight channels of IDT82V2058 can all be configured to work as regular transceivers. In applications using only seven channels (channels 1 to 7), channel 0 is configured to non-intrusively monitor any of the other channels' inputs or outputs on the line side. The monitoring is non-intrusive per ITU-T G.772. Figure-20 shows the Monitoring Principle. The receiver path or transmitter path to be monitored is configured by pins MC[3:0] in hardware mode or by register **PMON** in host mode.

The monitored signal goes through the clock and data recovery circuit of channel 0. The monitored clock can output on RCLK0 which can be used as a timing interfaces derived from E1 signal. The monitored data can be observed digitally at the output pins RCLK0, RD0/RDP0 and RDN0. LOS detector is still in use in channel 0 for the monitored signal.

In monitoring mode, channel 0 can be configured in Remote Loopback. The signal which is being monitored will output on TTIP0 and TRING0. The output signal can then be connected to a standard test equipment with an E1 electrical interface for non-intrusive monitoring.

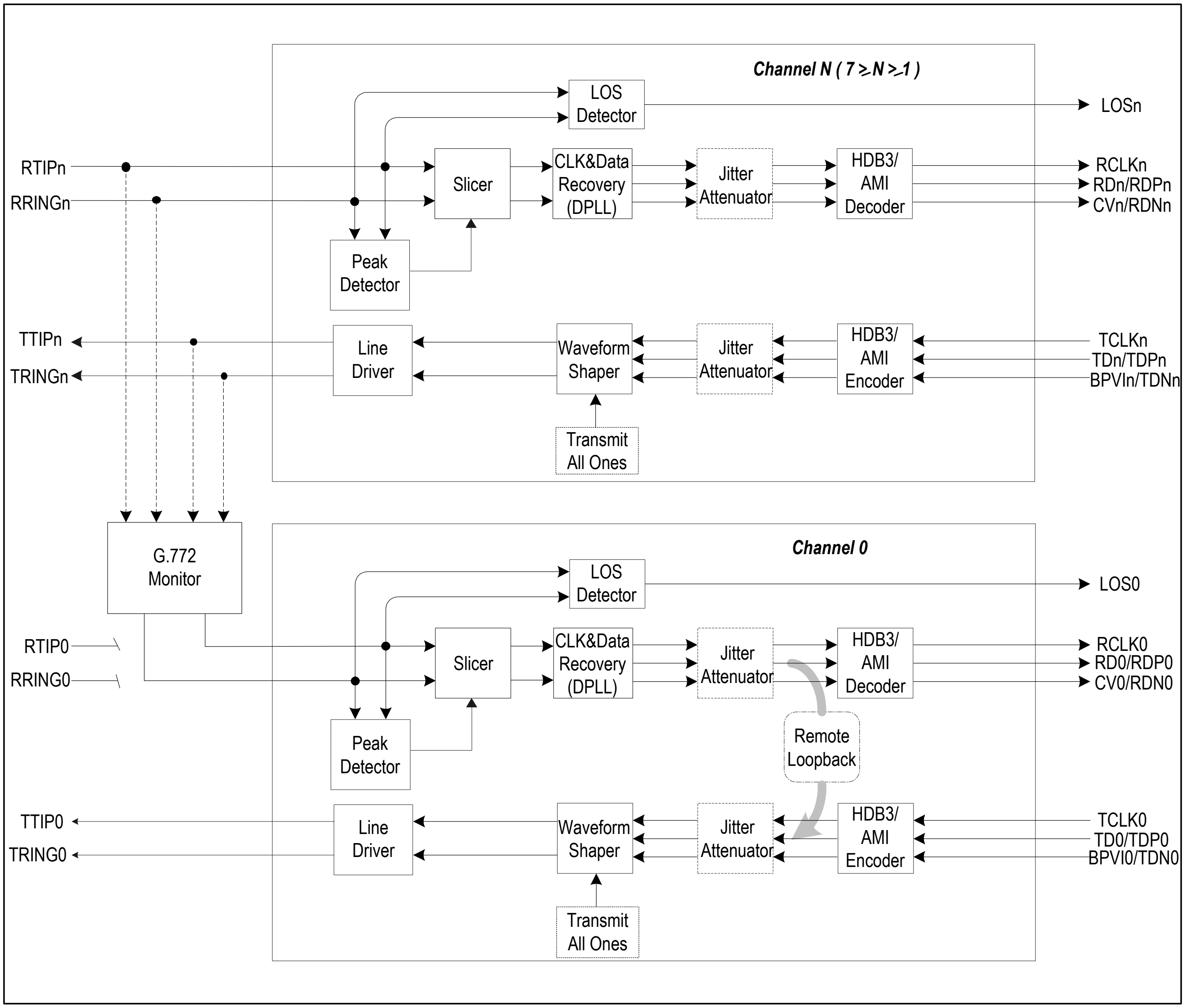


Figure-20 Monitoring Principle

3 PROGRAMMING INFORMATION

3.1 REGISTER LIST AND MAP

There are 21 primary registers (including an Address Pointer Control Register and 8 expanded registers in the device).

Whatever the control interface is, 5 address bits are used to set the registers. In non-multiplexed parallel interface mode, the five dedicated address bits are A[4:0]. In multiplexed parallel interface mode, AD[4:0] carries the address information. In serial interface mode, A[5:1] are used to address the register.

The Register **ADDP**, addressed as 11111 or 1F Hex, switches between primary registers bank and expanded registers bank.

By setting the register **ADDP** to 'AAH', the 5 address bits point to the expanded register bank, that is, the expanded registers are available. By clearing register **ADDP**, the primary registers are available.

Primary Registers, whose addresses are 10H, 11H, 16H to 1EH, are reserved. Expanded registers, whose addresses are 08H to 1EH, are used for test and must be set to '0' (default).

Table-13 Primary Register List

Address			Register	R/W	Explanation
Hex	Serial Interface A7-A1	Parallel Interface A7-A0			
00	XX00000	XXX00000	ID	R	Device ID Register
01	XX00001	XXX00001	ALB	R/W	Analog Loopback Configuration Register
02	XX00010	XXX00010	RLB	R/W	Remote Loopback Configuration Register
03	XX00011	XXX00011	TAO	R/W	Transmit All Ones Configuration Register
04	XX00100	XXX00100	LOS	R	Loss of Signal Status Register
05	XX00101	XXX00101	DF	R	Driver Fault Status Register
06	XX00110	XXX00110	LOSM	R/W	LOS Interrupt Mask Register
07	XX00111	XXX00111	DFM	R/W	Driver Fault Interrupt Mask Register
08	XX01000	XXX01000	LOSI	R	LOS Interrupt Status Register
09	XX01001	XXX01001	DFI	R	Driver Fault Interrupt Status Register
0A	XX01010	XXX01010	RS	W	Software Reset Register
0B	XX01011	XXX01011	PMON	R/W	Performance Monitor Configuration Register
0C	XX01100	XXX01100	DLB	R/W	Digital Loopback Configuration Register
0D	XX01101	XXX01101	LAC	R/W	LOS/AIS Criteria Configuration Register
0E	XX01110	XXX01110	ATAO	R/W	Automatic TAOS Configuration Register
0F	XX01111	XXX01111	GCF	R/W	Global Configuration Register
10	XX10000	XXX10000	Reserved		
11	XX10001	XXX10001			
12	XX10010	XXX10010	OE	R/W	Output Enable Configuration Register
13	XX10011	XXX10011	AIS	R	AIS Status Register
14	XX10100	XXX10100	AISM	R/W	AIS Interrupt Mask Register
15	XX10101	XXX10101	AISI	R	AIS Interrupt Status Register
16	XX10110	XXX10110	Reserved		
17	XX10111	XXX10111			
18	XX11000	XXX11000			
19	XX11001	XXX11001			
1A	XX11010	XXX11010			
1B	XX11011	XXX11011			
1C	XX11100	XXX11100			
1D	XX11101	XXX11101			
1E	XX11110	XXX11110			
1F	XX11111	XXX11111	ADDP	R/W	Address pointer control Register for switching between primary register bank and expanded register bank