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SINGLE CHANNEL T1/E1/J1 LONG HAUL/SHORT HAUL LINE INTERFACE UNIT

IDT82V2081

FEATURES

- **Single channel T1/E1/J1 long haul/short haul line interface**
- **Supports HPS (hitless protection Switching) for 1+1 protection without external relays**
- **Receiver sensitivity exceeds -36 dB@772KHz and -43 dB@1024 KHz**
- **Programmable T1/E1/J1 switchability allowing one bill of material for any line condition**
- **Single 3.3 V power supply with 5 V tolerance on digital interfaces**
- **Meets or exceeds specifications in**
 - ANSI T1.102, T1.403 and T1.408
 - ITU I.431, G.703, G.736, G.775 and G.823
 - ETSI 300-166, 300-233 and TBR12/13
 - AT&T Pub 62411
- **Software programmable or hardware selectable on:**
 - Wave-shaping templates for short haul and long haul LBO (Line Build Out)
 - Line terminating impedance (T1:100 Ω , J1:110 Ω , E1:75 Ω /120 Ω)
 - Adjustment of arbitrary pulse shape
 - JA (Jitter Attenuator) position (receive path or transmit path)
 - Single rail/dual rail system interfaces
 - B8ZS/HDB3/AMI line encoding/decoding
 - Active edge of transmit clock (TCLK) and receive clock (RCLK)
 - Active level of transmit data (TDATA) and receive data (RDATA)
- Receiver or transmitter power down
- High impedance setting for line drivers
- PRBS (pseudo random bit sequence) generation and detection with $2^{15}-1$ PRBS polynomials for E1
- QRSS (quasi random signal source) generation and detection with $2^{20}-1$ QRSS polynomials for T1/J1
- 16-bit BPV (bipolar pulse violation) /excess zero/PRBS or QRSS error counter
- Analog loopback, digital loopback, remote loopback and inband loopback
- **Cable attenuation indication**
- **Adaptive receive sensitivity**
- **Short circuit protection and internal protection diode for line drivers**
- **AIS (alarm indication signal) detection**
- **Supports serial control interface, Motorola and Intel multiplexed interfaces and hardware control mode**
- **Pin compatible 82V2041E T1/E1/J1 short haul LIU and 82V2051E E1 short haul LIU**
- **Package:**
Available in 44-pin TQFP and 48-pin QFN packages

DESCRIPTION

The IDT82V2081 can be configured as a single channel T1, E1 or J1 line interface unit. In the receive path, an adaptive equalizer is integrated to remove the distortion introduced by cable attenuation. The IDT82V2081 also performs clock/data recovery, AMI/B8ZS/HDB3 line decoding and detects and reports LOS conditions. In the transmit path, there is an AMI/B8ZS/HDB3 encoder, waveform shaper and LBOs. There is one jitter attenuator, which can be placed in either the receive path or the transmit path. The jitter attenuator can also be disabled. The IDT82V2081 supports both single rail and dual rail system interfaces. To facilitate the network maintenance, a PRBS/QRSS generation/detection circuit is integrated in the chip,

and different types of loopbacks can be set according to the applications. Four different kinds of line terminating impedance, 75 Ω , 100 Ω , 110 Ω and 120 Ω are selectable. The IDT82V2081 also provides driver short-circuit protection and internal protection diodes. The IDT82V2081 can be controlled by either software or hardware.

The IDT82V2081 can be used in LAN, WAN, routers, wireless base stations, IADs, IMAs, IMAPs, gateways, frame relay access devices, CSU/DSU equipment, etc.

FUNCTIONAL BLOCK DIAGRAM

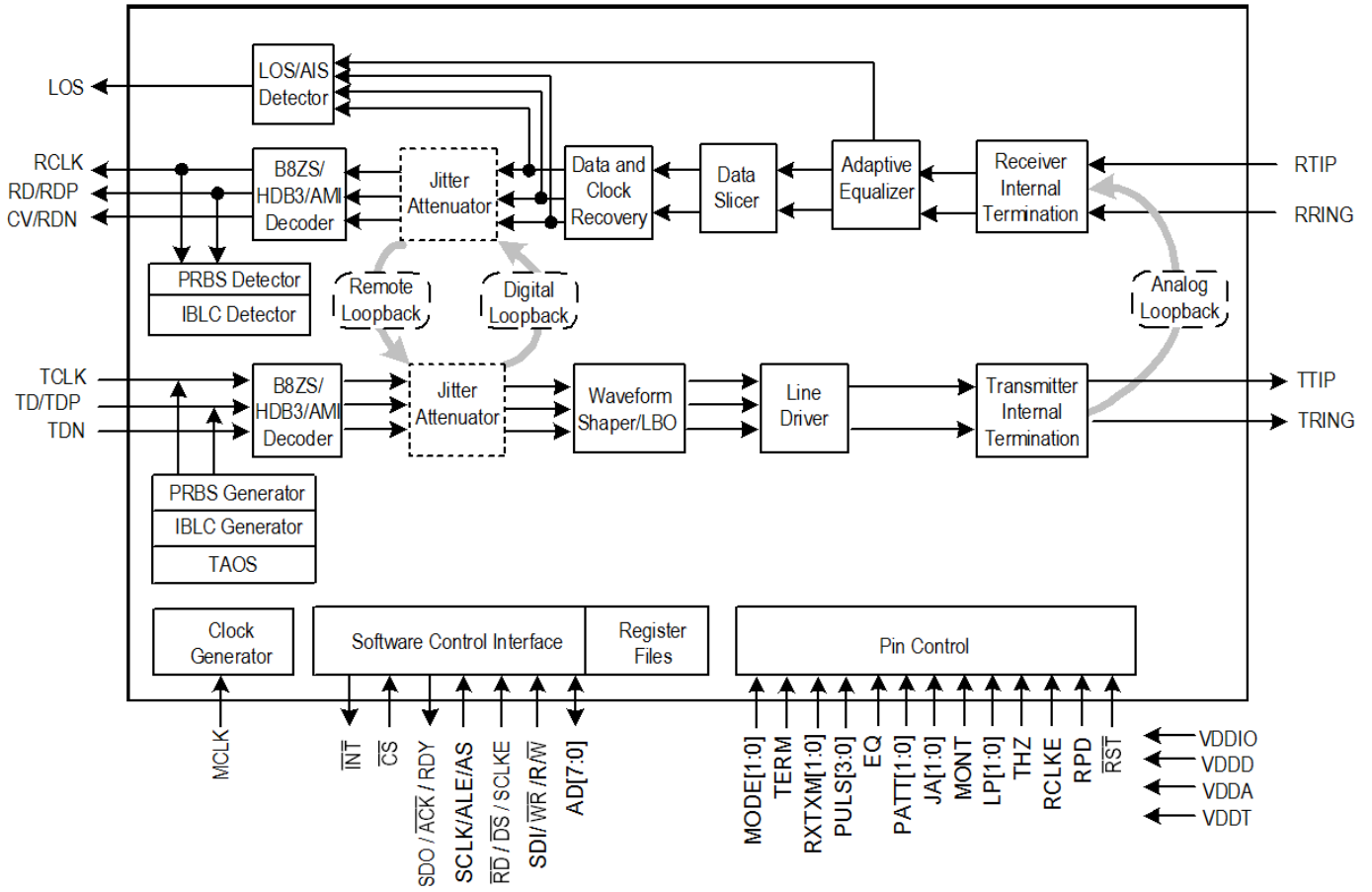


Figure-1 Block Diagram



- 1 IDT82V2081 Pin Configurations 8**
- 2 Pin Description 10**
- 3 Functional Description 16**
 - 3.1 Control Mode Selection 16
 - 3.2 T1/E1/J1 Mode Selection 16
 - 3.3 Transmit Path 16
 - 3.3.1 Transmit Path System Interface..... 16
 - 3.3.2 Encoder..... 16
 - 3.3.3 Pulse Shaper 16
 - 3.3.3.1 Preset Pulse Templates 16
 - 3.3.3.2 LBO (Line Build Out) 17
 - 3.3.3.3 User-Programmable Arbitrary Waveform 18
 - 3.3.4 Transmit Path Line Interface..... 22
 - 3.3.5 Transmit Path Power Down 22
 - 3.4 Receive Path 23
 - 3.4.1 Receive Internal Termination 23
 - 3.4.2 Line Monitor 24
 - 3.4.3 Adaptive Equalizer 25
 - 3.4.4 Receive Sensitivity 25
 - 3.4.5 Data Slicer 25
 - 3.4.6 CDR (Clock & Data Recovery)..... 25
 - 3.4.7 Decoder 25
 - 3.4.8 Receive Path System Interface..... 26
 - 3.4.9 Receive Path Power Down 26
 - 3.5 Jitter Attenuator 26
 - 3.5.1 Jitter Attenuation Function Description 26
 - 3.5.2 Jitter Attenuator Performance 27
 - 3.6 Los And AIS Detection 27
 - 3.6.1 LOS Detection..... 27
 - 3.6.2 AIS Detection 29
 - 3.7 Transmit And Detect Internal Patterns 31
 - 3.7.1 Transmit All Ones 31
 - 3.7.2 Transmit All Zeros..... 31
 - 3.7.3 PRBS/QRSS Generation And Detection..... 31
 - 3.8 Loopback 31
 - 3.8.1 Analog Loopback 31
 - 3.8.2 Digital Loopback 31

3.8.3	Remote Loopback.....	31
3.8.4	Inband Loopback	33
3.8.4.1	Transmit Activate/Deactivate Loopback Code.....	33
3.8.4.2	Receive Activate/Deactivate Loopback Code.....	33
3.8.4.3	Automatic Remote Loopback	33
3.9	Error Detection/Counting And Insertion	35
3.9.1	Definition Of Line Coding Error	35
3.9.2	Error Detection And Counting	35
3.9.3	Bipolar Violation And PRBS Error Insertion	36
3.10	Line Driver Failure Monitoring	36
3.11	MCLK And TCLK	37
3.11.1	Master Clock (MCLK).....	37
3.11.2	Transmit Clock (TCLK)	37
3.12	Microcontroller Interfaces	38
3.12.1	Parallel Microcontroller Interface	38
3.12.2	Serial Microcontroller Interface	38
3.13	Interrupt Handling	38
3.14	5V Tolerant I/O Pins	39
3.15	Reset Operation	39
3.16	Power Supply	39
4	Programming Information	40
4.1	Register List And Map	40
4.2	Reserved Registers	40
4.3	Register Description	41
4.3.1	Control Registers	41
4.3.2	Transmit Path Control Registers.....	43
4.3.3	Receive Path Control Registers.....	45
4.3.4	Network Diagnostics Control Registers	48
4.3.5	Interrupt Control Registers.....	51
4.3.6	Line Status Registers.....	54
4.3.7	Interrupt Status Registers	57
4.3.8	Counter Registers	59
5	Hardware Control Pin Summary	60
6	Test Specifications	62
7	Microcontroller Interface Timing Characteristics	75
7.1	Serial Interface Timing	75
7.2	Parallel Interface Timing	76



Figure-1	Block Diagram	2
Figure-2	IDT82V2081 TQFP Package Pin Assignment	8
Figure-3	IDT82V2081 NLG Package Pin Assignment	9
Figure-4	E1 Waveform Template Diagram	17
Figure-5	E1 Pulse Template Test Circuit	17
Figure-6	DSX-1 Waveform Template	17
Figure-7	Receive Monitor Gain Adaptive Equalizer	23
Figure-8	Transmit/Receive Line Circuit	24
Figure-9	Monitoring Receive Line in Another Chip	24
Figure-10	Monitor Transmit Line in Another Chip	24
Figure-11	Jitter Attenuator	26
Figure-12	LOS Declare and Clear	27
Figure-13	Analog Loopback	32
Figure-14	Digital Loopback	32
Figure-15	Remote Loopback	33
Figure-16	Auto Report Mode	35
Figure-17	Manual Report Mode	36
Figure-18	TCLK Operation Flowchart	37
Figure-19	Serial Microcontroller Interface Function Timing	38
Figure-20	Transmit System Interface Timing	69
Figure-21	Receive System Interface Timing	69
Figure-22	E1 Jitter Tolerance Performance	70
Figure-23	/J1 Jitter Tolerance Performance	71
Figure-24	E1 Jitter Transfer Performance	73
Figure-25	Serial Interface Write Timing	75
Figure-26	Serial Interface Read Timing with SCLKE=1	75
Figure-27	Serial Interface Read Timing with SCLKE=0	75
Figure-28	Multiplexed Motorola Read Timing	76
Figure-29	Multiplexed Motorola Write Timing	77
Figure-30	Multiplexed Intel Read Timing	78
Figure-31	Multiplexed Intel Write Timing	79



Table-1	Pin Description	10
Table-2	Transmit Waveform Value For E1 75 ohm.....	18
Table-3	Transmit Waveform Value For E1 120 ohm.....	19
Table-4	Transmit Waveform Value For T1 0~133 ft.....	19
Table-5	Transmit Waveform Value For T1 133~266 ft.....	19
Table-6	Transmit Waveform Value For T1 266~399 ft.....	19
Table-7	Transmit Waveform Value For T1 399~533 ft.....	20
Table-8	Transmit Waveform Value For T1 533~655 ft.....	20
Table-9	Transmit Waveform Value For J1 0~655 ft.....	20
Table-10	Transmit Waveform Value For DS1 0 dB LBO.....	20
Table-11	Transmit Waveform Value For DS1 -7.5 dB LBO	21
Table-12	Transmit Waveform Value For DS1 -15.0 dB LBO	21
Table-13	Transmit Waveform Value For DS1 -22.5 dB LBO	21
Table-14	Impedance Matching for Transmitter	22
Table-15	Impedance Matching for Receiver	23
Table-16	Criteria of Starting Speed Adjustment.....	27
Table-17	LOS Declare and Clear Criteria for Short Haul Mode	28
Table-18	LOS Declare and Clear Criteria for Long Haul Mode.....	29
Table-19	AIS Condition	30
Table-20	Criteria for Setting/Clearing the PRBS_S Bit	31
Table-21	EXZ Definition	35
Table-22	Interrupt Event.....	39
Table-23	Register List and Map	40
Table-24	ID: Device Revision Register	41
Table-25	RST: Reset Register	41
Table-26	GCF: Global Configuration Register	41
Table-27	TERM: Transmit and Receive Termination Configuration Register	41
Table-28	JACF: Jitter Attenuation Configuration Register	42
Table-29	TCF0: Transmitter Configuration Register 0	43
Table-30	TCF1: Transmitter Configuration Register 1	43
Table-31	TCF2: Transmitter Configuration Register 2	44
Table-32	TCF3: Transmitter Configuration Register 3	44
Table-33	TCF4: Transmitter Configuration Register 4	44
Table-34	RCF0: Receiver Configuration Register 0.....	45
Table-35	RCF1: Receiver Configuration Register 1	46
Table-36	RCF2: Receiver Configuration Register 2.....	47
Table-37	MAINT0: Maintenance Function Control Register 0.....	48
Table-38	MAINT1: Maintenance Function Control Register 1	48
Table-39	MAINT2: Maintenance Function Control Register 2.....	49
Table-40	MAINT3: Maintenance Function Control Register 3.....	49
Table-41	MAINT4: Maintenance Function Control Register 4.....	49

Table-42	MAINT5: Maintenance Function Control Register 5.....	49
Table-43	MAINT6: Maintenance Function Control Register 6.....	50
Table-44	INTM0: Interrupt Mask Register 0.....	51
Table-45	INTM1: Interrupt Masked Register 1.....	52
Table-46	INTES: Interrupt Trigger Edge Select Register.....	53
Table-47	STAT0: Line Status Register 0 (real time status monitor).....	54
Table-48	STAT1: Line Status Register 1 (real time status monitor).....	56
Table-49	INTS0: Interrupt Status Register 0.....	57
Table-50	INTS1: Interrupt Status Register 1.....	58
Table-51	CNT0: Error Counter L-byte Register 0.....	59
Table-52	CNT1: Error Counter H-byte Register 1.....	59
Table-53	Hardware Control Pin Summary.....	60
Table-54	Absolute Maximum Rating.....	62
Table-55	Recommended Operation Conditions.....	62
Table-56	Power Consumption.....	63
Table-57	DC Characteristics.....	63
Table-58	E1 Receiver Electrical Characteristics.....	64
Table-59	T1/J1 Receiver Electrical Characteristics.....	65
Table-60	E1 Transmitter Electrical Characteristics.....	66
Table-61	T1/J1 Transmitter Electrical Characteristics.....	67
Table-62	Transmitter and Receiver Timing Characteristics.....	68
Table-63	Jitter Tolerance.....	69
Table-64	Jitter Attenuator Characteristics.....	72
Table-65	Serial Interface Timing Characteristics.....	75
Table-66	Multiplexed Motorola Read Timing Characteristics.....	76
Table-67	Multiplexed Motorola Write Timing Characteristics.....	77
Table-68	Multiplexed Intel Read Timing Characteristics.....	78
Table-69	Multiplexed Intel Write Timing Characteristics.....	79

1 IDT82V2081 PIN CONFIGURATIONS

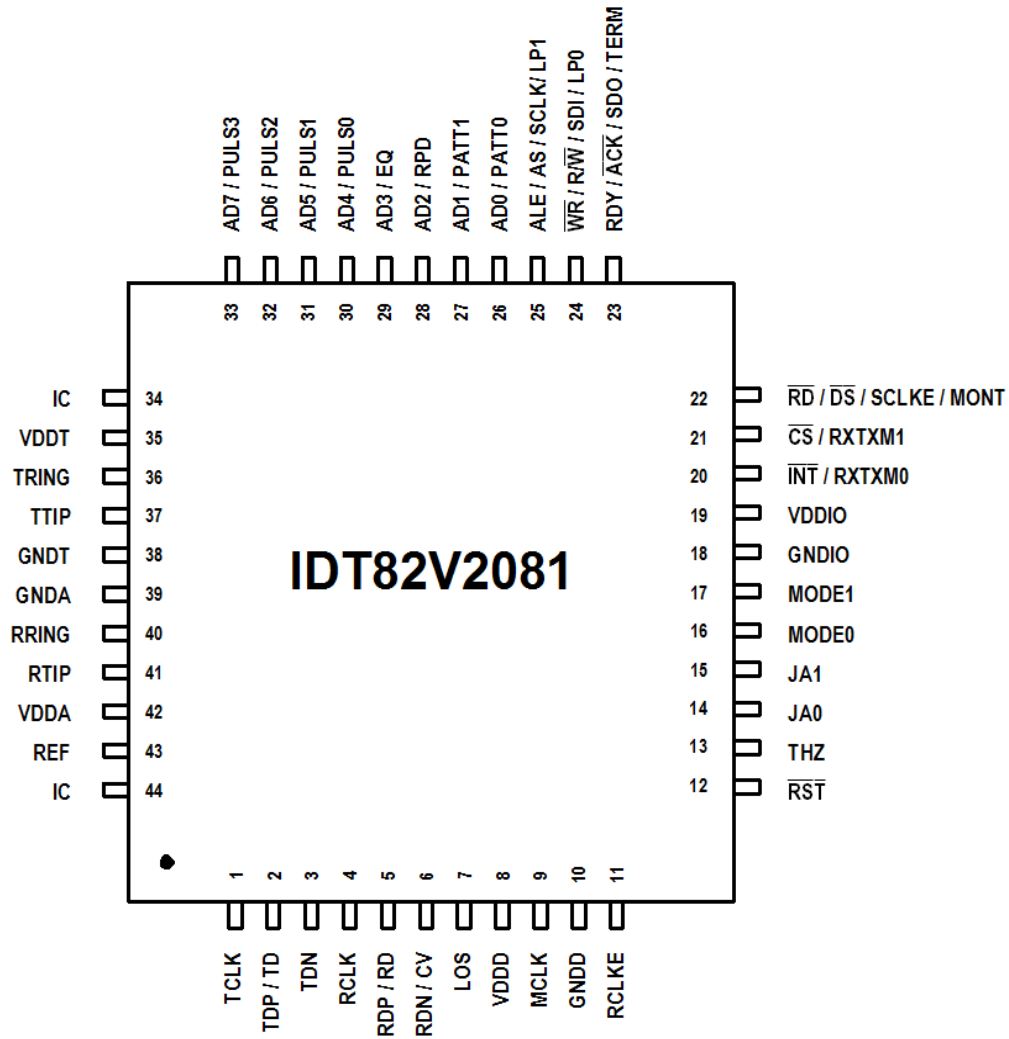


Figure-2 IDT82V2081 TQFP Package Pin Assignment



Figure-3 IDT82V2081 NLG Package Pin Assignment

2 PIN DESCRIPTION

Table-1 Pin Description

Name	Type	TQFP 44 Pin No.	QFN 48 Pin No.	Description															
TTIP TRING	Analog output	37 36	40 39	<p>TTIP/TRING: Transmit Bipolar Tip/Ring These pins are the differential line driver outputs. They will be in high impedance state under the following conditions:</p> <ul style="list-style-type: none"> • THZ pin is high; • THZ bit is set to 1; • Loss of MCLK; • Loss of TCLK (exceptions: Remote Loopback; transmit internal pattern by MCLK); • Transmit path power down; • After software reset; pin reset and power on. 															
RTIP RRING	Analog input	41 40	44 43	<p>RTIP/RRING: Receive Bipolar Tip/Ring These signals are the differential receiver inputs.</p>															
TD/TDP TDN	I	2 3	2 3	<p>TD: Transmit Data When the device is in single rail mode, the NRZ data to be transmitted is input on this pin. Data on TD pin is sampled into the device on the active edge of TCLK and is encoded by AMI, HDB3 or B8ZS line code rules before being transmitted. In this mode, TDN should be connected to ground.</p> <p>TDP/TDN: Positive/Negative Transmit Data When the device is in dual rail mode, the NRZ data to be transmitted for positive/negative pulse is input on these pins. Data on TDP/TDN pin is sampled into the device on the active edge of TCLK. The line code in dual rail mode is as follows:</p> <table border="1"> <thead> <tr> <th>TDP</th> <th>TDN</th> <th>Output Pulse</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Space</td> </tr> <tr> <td>0</td> <td>1</td> <td>Positive Pulse</td> </tr> <tr> <td>1</td> <td>0</td> <td>Negative Pulse</td> </tr> <tr> <td>1</td> <td>1</td> <td>Space</td> </tr> </tbody> </table>	TDP	TDN	Output Pulse	0	0	Space	0	1	Positive Pulse	1	0	Negative Pulse	1	1	Space
TDP	TDN	Output Pulse																	
0	0	Space																	
0	1	Positive Pulse																	
1	0	Negative Pulse																	
1	1	Space																	
TCLK	I	1	1	<p>TCLK: Transmit Clock input This pin inputs 1.544 MHz for T1/J1 mode or 2.048 MHz for E1 mode transmit clock. The transmit data at TD/TDP or TDN is sampled into the device on the active edge of TCLK. If TCLK is missing¹ and the TCLK missing interrupt is not masked, an interrupt will be generated.</p>															
RD/RDP CV/RDN	O	5 6	5 6	<p>RD: Receive Data output In single rail mode, this pin outputs NRZ data. The data is decoded according to AMI, HDB3 or B8ZS line code rules.</p> <p>CV: Code Violation indication In single rail mode, the BPV/CV code violation will be reported by driving the CV pin to high level for a full clock cycle. B8ZS/HDB3 line code violation can be indicated if the B8ZS/HDB3 decoder is enabled. When AMI decoder is selected, bipolar violation will be indicated. In hardware control mode, the EXZ, BPV/CV errors in received data stream are always monitored by the CV pin if single rail mode is chosen.</p> <p>RDP/RDN: Positive/Negative Receive Data output In dual rail mode, this pin outputs the re-timed NRZ data when CDR is enabled, or directly outputs the raw RZ slicer data if CDR is bypassed.</p> <p>Active edge and level select: Data on RDP/RDN or RD is clocked with either the rising or the falling edge of RCLK. The active polarity is also selectable.</p>															

Notes:

1. TCLK missing: the state of TCLK continues to be high level or low level over 70 MCLK cycles.

Table-1 Pin Description (Continued)

Name	Type	TQFP 44 Pin No.	QFN 48 Pin No.	Description										
RCLK	O	4	4	RCLK: Receive Clock output This pin outputs 1.544 MHz for T1/J1 mode or 2.048 MHz for E1 mode receive clock. Under LOS condition with AIS enabled (bit AISE=1), RCLK is derived from MCLK. In clock recovery mode, this signal provides the clock recovered from the RTIP/RRING signal. The receive data (RD in single rail mode or RDP and RDN in dual rail mode) is clocked out of the device on the active edge of RCLK. If clock recovery is bypassed, RCLK is the exclusive OR (XOR) output of the dual rail slicer data RDP and RDN. This signal can be used in applications with external clock recovery circuitry.										
MCLK	I	9	9	MCLK: Master Clock input A built-in clock system that accepts selectable 2.048MHz reference for E1 operating mode and 1.544MHz reference for T1/J1 operating mode. This reference clock is used to generate several internal reference signals: <ul style="list-style-type: none"> • Timing reference for the integrated clock recovery unit. • Timing reference for the integrated digital jitter attenuator. • Timing reference for microcontroller interface. • Generation of RCLK signal during a loss of signal condition. • Reference clock to transmit All Ones, all zeros, PRBS/QRSS pattern as well as activate or deactivate Inband Loopback code if MCLK is selected as the reference clock. Note that for ATA0 and AIS, MCLK is always used as the reference clock. • Reference clock during the Transmit All Ones (TAO) condition or sending PRBS/QRSS in hardware control mode. The loss of MCLK will turn TTIP/TRING into high impedance status.										
LOS	O	7	7	LOS: Loss of Signal Output This is an active high signal used to indicate the loss of received signal. When LOS pin becomes high, it indicates the loss of received signal. The LOS pin will become low automatically when valid received signal is detected again. The criteria of loss of signal are described in 3.6 Los And AIS Detection .										
REF	I	43	46	REF: reference resistor An external resistor (3 K Ω , 1%) is used to connect this pin to ground to provide a standard reference current for internal circuit.										
MODE1 MODE0	I	17 16	19 18	MODE[1:0]: operation mode of Control interface select The level on this pin determines which control mode is used to control the device as follows: <table border="1" style="margin: 10px auto;"> <thead> <tr> <th>MODE[1:0]</th> <th>Control Interface mode</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>Hardware interface</td> </tr> <tr> <td>01</td> <td>Serial Microcontroller Interface</td> </tr> <tr> <td>10</td> <td>Parallel –Multiplexed –Motorola Interface</td> </tr> <tr> <td>11</td> <td>Parallel –Multiplexed –Intel Interface</td> </tr> </tbody> </table> <ul style="list-style-type: none"> • The serial microcontroller Interface consists of \overline{CS}, SCLK, SCLKE, SDI, SDO and \overline{INT} pins. SCLKE is used for the selection of the active edge of SCLK. • The parallel multiplexed microcontroller interface consists of \overline{CS}, AD[7:0], $\overline{DS/RD}$, $\overline{R\overline{W}/WR}$, ALE/AS, $\overline{ACK/RDY}$ and \overline{INT} pins. (refer to 3.12 Microcontroller Interfaces for details) • Hardware interface consists of PULS[3:0], THZ, RCLKE, LP[1:0], PATT[1:0], JA[1:0], MONT, TERM, EQ, RPD, MODE[1:0] and RXTXM[1:0] 	MODE[1:0]	Control Interface mode	00	Hardware interface	01	Serial Microcontroller Interface	10	Parallel –Multiplexed –Motorola Interface	11	Parallel –Multiplexed –Intel Interface
MODE[1:0]	Control Interface mode													
00	Hardware interface													
01	Serial Microcontroller Interface													
10	Parallel –Multiplexed –Motorola Interface													
11	Parallel –Multiplexed –Intel Interface													
RCLKE	I	11	11	RCLKE: the active edge of RCLK select In hardware control mode, this pin selects the active edge of RCLK <ul style="list-style-type: none"> • L= select the rising edge as the active edge of RCLK • H= select the falling edge as the active edge of RCLK In software control mode, this pin should be connected to GNDIO.										

Table-1 Pin Description (Continued)

Name	Type	TQFP 44 Pin No.	QFN 48 Pin No.	Description
$\overline{\text{CS}}$ RXTXM1	I	21	23	<p>CS: Chip Select In serial or parallel microcontroller interface mode, this is the active low enable signal. A low level on this pin enables serial or parallel microcontroller interface.</p> <p>RXTXM[1:0]: Receive and transmit path operation mode select In hardware control mode, these pins are used to select the single rail or dual rail operation modes as well as AMI or HDB3/B8ZS line coding:</p> <ul style="list-style-type: none"> • 00= single rail with HDB3/B8ZS coding • 01= single rail with AMI coding • 10= dual rail interface with CDR enabled • 11= slicer mode (dual rail interface with CDR disabled)
$\overline{\text{INT}}$ RXTXM0	O I	20	22	<p>INT: Interrupt Request In software control mode, this pin outputs the general interrupt request for all interrupt sources. These interrupt sources can be masked individually via registers (INTM0, 14H) and (INTM1, 15H). The interrupt status is reported via the registers (INTS0, 19H) and (INTS1, 1AH). Output characteristics of this pin can be defined to be push-pull (active high or active low) or open-drain (active low) by setting INT_PIN[1:0] (GCF, 02H).</p> <p>RXTXM0 See RXTXM1 above.</p>
SCLK ALE AS LP1	I	25	27	<p>SCLK: Shift Clock In serial microcontroller interface mode, this signal is the shift clock for the serial interface. Configuration data on SDI pin is sampled on the rising edge of SCLK. Configuration and status data on SDO pin is clocked out of the device on the falling edge of SCLK if SCLKE pin is high, or on the rising edge of SCLK if SCLKE pin is low.</p> <p>ALE: Address Latch Enable In parallel microcontroller interface mode with multiplexed Intel interface, the address on AD[7:0] is sampled into the device on the falling edge of ALE.</p> <p>AS: Address Strobe In parallel microcontroller interface mode with multiplexed Motorola interface, the address on AD[7:0] is latched into the device on the falling edge of AS.</p> <p>LP[1:0]: Loopback mode select When the chip is configured by hardware, this pin is used to select loopback operation modes (Inband Loopback is not provided in hardware control mode):</p> <ul style="list-style-type: none"> • 00= no loopback • 01= analog loopback • 10= digital loopback • 11= remote loopback
SDI $\overline{\text{WR}}$ R $\overline{\text{W}}$ LP0	I	24	26	<p>SDI: Serial Data Input In serial microcontroller interface mode, this signal is the input data to the serial interface. Configuration data at SDI pin is sampled by the device on the rising edge of SCLK.</p> <p>$\overline{\text{WR}}$: Write Strobe In Intel parallel multiplexed interface mode, this pin is asserted low by the microcontroller to initiate a write cycle. The data on AD[7:0] is sampled into the device in a write operation.</p> <p>R$\overline{\text{W}}$: Read/Write Select In Motorola parallel multiplexed interface mode, this pin is low for write operation and high for read operation.</p> <p>LP0 See LP1 above.</p>

Table-1 Pin Description (Continued)

Name	Type	TQFP 44 Pin No.	QFN 48 Pin No.	Description						
SDO	O	23	25	<p>SDO: Serial Data Output In serial microcontroller interface mode, this signal is the output data of the serial interface. Configuration or Status data at SDO pin is clocked out of the device on the falling edge of SCLK if SCLKE pin is high, or on the rising edge of SCLK if SCLKE pin is low.</p> <p>$\overline{\text{ACK}}$: Acknowledge Output In Motorola parallel mode interface, the low level on this pin means:</p> <ul style="list-style-type: none"> The valid information is on the data bus during a read operation. The write data has been accepted during a write cycle. <p>RDY: Ready signal output In Intel parallel mode interface, the low level on this pin means a read or write operation is in progress; a high acknowledges a read or write operation has been completed.</p> <p>TERM: Internal or external termination select in hardware mode This pin selects internal or external impedance matching for both receiver and transmitter.</p> <ul style="list-style-type: none"> 0 = ternary interface with external impedance matching network 1 = ternary interface with internal impedance matching network 						
SCLKE	I	22	24	<p>SCLKE: Serial Clock Edge Select In serial microcontroller interface mode, this signal selects the active edge of SCLK for outputting SDO. The output data is valid after some delay from the active clock edge. It can be sampled on the opposite edge of the clock. The active clock edge which clocks the data out of the device is selected as shown below:</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>SCLKE</th> <th>SCLK</th> </tr> </thead> <tbody> <tr> <td>Low</td> <td>Rising edge is the active edge.</td> </tr> <tr> <td>High</td> <td>Falling edge is the active edge.</td> </tr> </tbody> </table> <p>$\overline{\text{RD}}$: Read Strobe In Intel parallel multiplexed interface mode, the data is driven to AD[7:0] by the device during low level of $\overline{\text{RD}}$ in a read operation.</p> <p>$\overline{\text{DS}}$: Data Strobe In Motorola parallel multiplexed interface mode, this signal is the data strobe of the parallel interface. In a write operation ($R/\overline{W} = 0$), the data on AD[7:0] is sampled into the device. In a read operation ($R/\overline{W} = 1$), the data is driven to AD[7:0] by the device.</p> <p>MONT: Receive Monitor gain select In hardware control mode with ternary interface, this pin selects the receive monitor gain of receiver: 0= 0 dB 1= 26 dB</p>	SCLKE	SCLK	Low	Rising edge is the active edge.	High	Falling edge is the active edge.
SCLKE	SCLK									
Low	Rising edge is the active edge.									
High	Falling edge is the active edge.									
AD7	I/O	33	35	<p>AD7: Address/Data Bus bit7 In Intel/Motorola multiplexed interface mode, this signal is the multiplexed bi-directional address/data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor.</p>						
PULS3	I			<p>PULS[3:0]: these pins are used to select the following functions in hardware control mode:</p> <ul style="list-style-type: none"> T1/J1/E1 mode Transmit pulse template Internal termination impedance (75Ω/120Ω/100Ω/110Ω) 						

Table-1 Pin Description (Continued)

Name	Type	TQFP 44 Pin No.	QFN 48 Pin No.	Description
AD6	I/O	32	34	AD6: Address/Data Bus bit6 In Intel/Motorola multiplexed interface mode, this signal is the multiplexed bi-directional address/data bus of the micro-controller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 k Ω resistor.
PULS2	I			See above.
AD5	I/O	31	33	AD5: Address/Data Bus bit5 In Intel/Motorola multiplexed interface mode, this signal is the multiplexed bi-directional address/data bus of the micro-controller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 k Ω resistor.
PULS1	I			See above.
AD4	I/O	30	32	AD4: Address/Data Bus bit4 In Intel/Motorola multiplexed interface mode, this signal is the multiplexed bi-directional address/data bus of the micro-controller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 k Ω resistor.
PULS0	I			See above.
AD3	I/O	29	31	AD3: Address/Data Bus bit3 In Intel/Motorola multiplexed interface mode, this signal is the multiplexed bi-directional address/data bus of the micro-controller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 k Ω resistor.
EQ	I			EQ: Receive Equalizer on/off control in hardware control mode <ul style="list-style-type: none"> • 0= short haul (10 dB) • 1= long haul (36 dB for T1/J1, 43 dB for E1)
AD2	I/O	28	30	AD2: Address/Data Bus bit2 In Intel/Motorola multiplexed interface mode, this signal is the multiplexed bi-directional address/data bus of the micro-controller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 k Ω resistor.
RPD	I			RPD: Receiver power down control in hardware control mode <ul style="list-style-type: none"> • 0= normal operation • 1= receiver power down
AD1	I/O	27	29	AD1: Address/Data Bus bit1 In Intel/Motorola multiplexed interface mode, this signal is the multiplexed bi-directional address/data bus of the micro-controller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 k Ω resistor.
PATT1	I			PATT[1:0]: Transmit pattern select In hardware control mode, this pin selects the transmit pattern <ul style="list-style-type: none"> • 00 = normal • 01= All Ones • 10= PRBS • 11= transmitter power down
AD0	I/O	26	28	AD0: Address/Data Bus bit0 In Intel/Motorola multiplexed interface mode, this signal is the multiplexed bi-directional address/data bus of the micro-controller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 k Ω resistor.
PATT0	I			See above.

Table-1 Pin Description (Continued)

Name	Type	TQFP 44 Pin No.	QFN 48 Pin No.	Description
JA1	I	15	17	JA[1:0]: Jitter attenuation position, bandwidth and the depth of FIFO select (only used for hardware control mode) <ul style="list-style-type: none"> • 00 = JA is disabled • 01 = JA in receiver, broad bandwidth, FIFO=64 bits • 10 = JA in receiver, narrow bandwidth, FIFO=128 bits • 11 = JA in transmitter, narrow bandwidth, FIFO=128 bits In software control mode, this pin should be connected to ground.
JA0	I	14	16	See above.
$\overline{\text{RST}}$	I	12	14	$\overline{\text{RST}}$: Hardware reset The chip is forced to reset state if a low signal is input on this pin for more than 100 ns. MCLK must be active during reset.
THZ	I	13	15	THZ: Transmitter Driver High Impedance Enable This signal enables or disables transmitter driver. A low level on this pin enables the driver while a high level on this pin places driver in high impedance state. Note that the functionality of the internal circuits is not affected by this signal.
Power Supplies and Grounds				
VDDIO	-	19	21	3.3 V I/O power supply
GNDIO	-	18	20	I/O ground
VDDT	-	35	38	3.3 V power supply for transmitter driver
GNDT	-	38	41	Analog ground for transmitter driver
VDDA	-	42	45	3.3 V analog core power supply
GND A	-	39	42	Analog core ground
VDDD	-	8	8	Digital core power supply
GNDD	-	10	10	Digital core ground
Others				
IC1	-	34	37	IC: Internal connection Internal Use. This pin should be left open when in normal operation.
IC2	-	44	47	IC: Internal connection Internal Use. This pin should be connected to ground when in normal operation.
nc	-	-	12, 13, 36, 48	NC: Not connected These pins should be left open.

3 FUNCTIONAL DESCRIPTION

3.1 CONTROL MODE SELECTION

The IDT82V2081 can be configured by software or by hardware. The software control mode supports Serial Control Interface, Motorola Multiplexed Control Interface and Intel Multiplexed Control Interface. The Control mode is selected by MODE1 and MODE0 pins as follows:

	Control Interface mode
00	Hardware interface
01	Serial Microcontroller Interface.
10	Parallel –Multiplexed -Motorola Interface
11	Parallel –Multiplexed -Intel Interface

- The serial microcontroller Interface consists of \overline{CS} , SCLK, SCLKE, SDI, SDO and \overline{INT} pins. SCLKE is used for the selection of active edge of SCLK.
- The parallel Multiplexed microcontroller Interface consists of \overline{CS} , AD[7:0], $\overline{DS/RD}$, R/W/ \overline{WR} , ALE/AS, $\overline{ACK/RDY}$ and \overline{INT} pins.
- Hardware interface consists of PULS[3:0], THZ, RCLKE, LP[1:0], PATT[1:0], JA[1:0], MONT, TERM, EQ, RPD, MODE[1:0] and RXTXM[1:0]. Refer to chapter 5 Hardware Control Pin Summary for details about hardware control.

3.2 T1/E1/J1 MODE SELECTION

When the chip is configured by software, T1/E1/J1 mode is selected by the T1E1 bit (**GCF, 02H**). In E1 application, the T1E1 bit (**GCF, 02H**) should be set to '0'. In T1/J1 application, the T1E1 bit should be set to '1'.

When the chip is configured by hardware, T1/E1/J1 mode is selected by PULS[3:0] pins. These pins also determine transmit pulse template and internal termination impedance. Refer to [5 Hardware Control Pin Summary](#) for details.

3.3 TRANSMIT PATH

The transmit path of IDT82V2081 consists of an Encoder, an optional Jitter Attenuator, a Waveform Shaper, a set of LBOs, a Line Driver and a Programmable Transmit Termination.

3.3.1 TRANSMIT PATH SYSTEM INTERFACE

The transmit path system interface consists of TCLK pin, TD/TDP pin and TDN pin. In E1 mode, TCLK is a 2.048 MHz clock. In T1/J1 mode, TCLK is a 1.544 MHz clock. If TCLK is missing for more than 70 MCLK cycles, an interrupt will be generated if it is not masked.

Transmit data is sampled on the TD/TDP and TDN pins by the active edge of TCLK. The active edge of TCLK can be selected by the TCLK_SEL

bit (**TCF0, 05H**). And the active level of the data on TD/TDP and TDN can be selected by the TD_INV bit (**TCF0, 05H**). In hardware control mode, the falling edge of TCLK and the active high of transmit data are always used.

The transmit data from the system side can be provided in two different ways: Single Rail and Dual Rail. In Single Rail mode, only TD pin is used for transmitting data and the T_MD[1] bit (**TCF0, 05H**) should be set to '0'. In Dual Rail Mode, both TDP pin and TDN pin are used for transmitting data, the T_MD[1] bit (**TCF0, 05H**) should be set to '1'.

3.3.2 ENCODER

In Single Rail mode, when T1/J1 mode is selected, the Encoder can be selected to be a B8ZS encoder or an AMI encoder by setting T_MD[0] bit (**TCF0, 05H**).

In Single Rail mode, when E1 mode is selected, the Encoder can be configured to be a HDB3 encoder or an AMI encoder by setting T_MD[0] bit (**TCF0, 05H**).

In both T1/J1 mode and E1 mode, when Dual Rail mode is selected (bit T_MD[1] is '1'), the Encoder is by-passed. In Dual Rail mode, a logic '1' on the TDP pin and a logic '0' on the TDN pin results in a negative pulse on the TTIP/TRING; a logic '0' on TDP pin and a logic '1' on TDN pin results in a positive pulse on the TTIP/TRING. If both TDP and TDN are high or low, the TTIP/TRING outputs a space (Refer to [TD/TDP, TDN Pin Description](#)).

In hardware control mode, the operation mode of receive and transmit path can be selected by setting RXTXM1 and RXTXM0 pins. Refer to [5 Hardware Control Pin Summary](#) for details.

3.3.3 PULSE SHAPER

The IDT82V2081 provides three ways of manipulating the pulse shape before sending it. The first is to use preset pulse templates for short haul application, the second is to use LBO (Line Build Out) for long haul application and the other way is to use user-programmable arbitrary waveform template.

In software control mode, the pulse shape can be selected by setting the related registers.

In hardware control mode, the pulse shape can be selected by setting PULS[3:0] pins. Refer to [5 Hardware Control Pin Summary](#) for details.

3.3.3.1 PRESET PULSE TEMPLATES

For E1 applications, the pulse shape is shown in [Figure-4](#) according to the G.703 and the measuring diagram is shown in [Figure-5](#). In internal impedance matching mode, if the cable impedance is 75 Ω , the PULS[3:0] bits (**TCF1, 06H**) should be set to '0000'; if the cable impedance is 120 Ω , the PULS[3:0] bits (**TCF1, 06H**) should be set to '0001'. In external impedance matching mode, for both E1/75 Ω and E1/120 Ω cable impedance, PULS[3:0] should be set to '0001'.

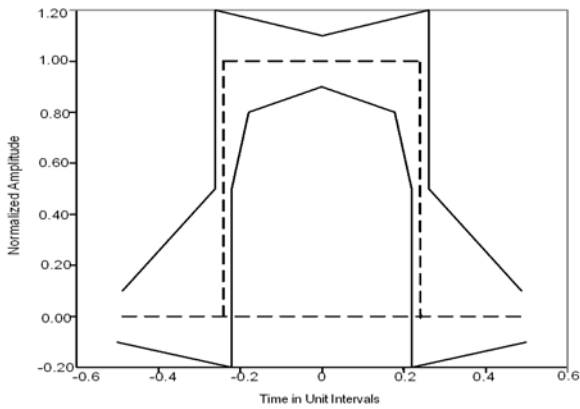


Figure-4 E1 Waveform Template Diagram

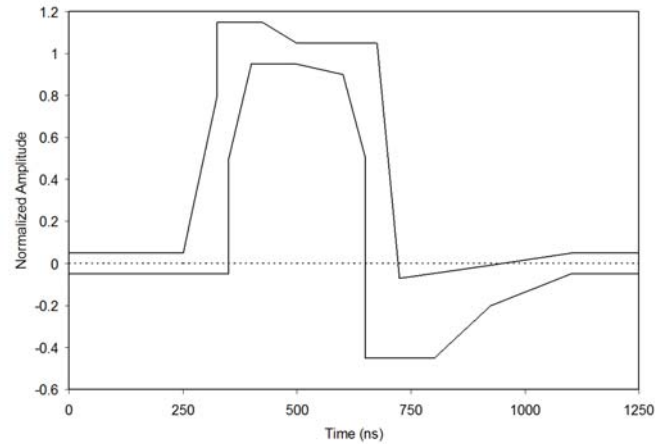


Figure-6 DSX-1 Waveform Template

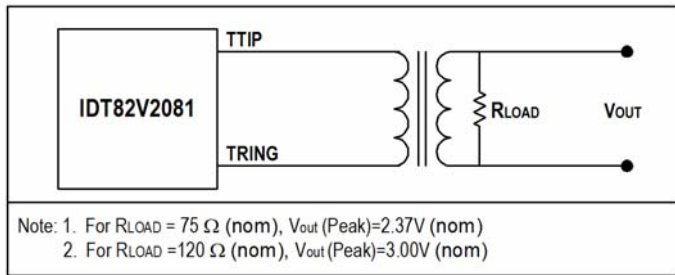
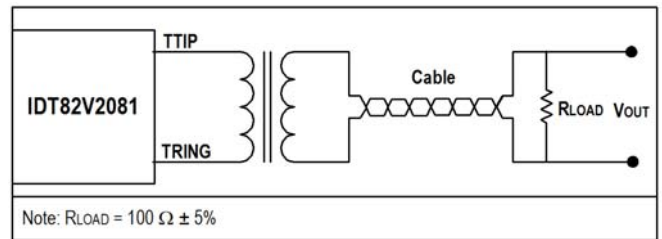


Figure-5 E1 Pulse Template Test Circuit



TCF1, 06H) should be set to '0111'. Table-14 lists these values.

3.3.3.2 LBO (LINE BUILD OUT)

To prevent the cross-talk at the far end, the output of TTIP/TRING could be attenuated before transmission for long haul applications. The FCC Part 68 Regulations specifies four grades of attenuation with a step of 7.5 dB. Three LBOs are used to implement the pulse attenuation. The PULS[3:0] bits (TCF1, 06H) are used to select the attenuation grade. Both Table-14 and Table-15 list these values.

3.3.3.3 USER-PROGRAMMABLE ARBITRARY WAVEFORM

When the PULS[3:0] bits are set to '11xx', user-programmable arbitrary waveform generator mode can be used. This allows the transmitter performance to be tuned for a wide variety of line condition or special application.

Each pulse shape can extend up to 4 UIs (Unit Interval), addressed by UI[1:0] bits (**TCF3, 08H**) and each UI is divided into 16 sub-phases, addressed by the SAMP[3:0] bits (**TCF3, 08H**). The pulse amplitude of each phase is represented by a binary byte, within the range from +63 to -63, stored in WDAT[6:0] bits (**TCF4, 09H**) in signed magnitude form. The most positive number +63 (D) represents the positive maximum amplitude of the transmit pulse while the most negative number -63 (D) represents the maximum negative amplitude of the transmit pulse. Therefore, up to 64 bytes are used.

There are twelve standard templates which are stored in an on-chip ROM. User can select one of them as reference and make some changes to get the desired waveform.

User can change the wave shape and the amplitude to get the desired pulse shape. In order to do this, firstly, users can choose a set of waveform value from the following twelve tables, which is the most similar to the desired pulse shape. [Table-2](#), [Table-3](#), [Table-4](#), [Table-5](#), [Table-6](#), [Table-7](#), [Table-8](#), [Table-9](#), [Table-10](#), [Table-11](#), [Table-12](#) and [Table-13](#) list the sample data and scaling data of each of the twelve templates. Then modify the corresponding sample data to get the desired transmit pulse shape.

Secondly, through the value of SCAL[5:0] bits increased or decreased by 1, the pulse amplitude can be scaled up or down at the percentage ratio against the standard pulse amplitude if needed. For different pulse shapes, the value of SCAL[5:0] bits and the scaling percentage ratio are different. The following twelve tables list these values.

Do the followings step by step, the desired waveform can be programmed, based on the selected waveform template:

- (1). Select the UI by UI[1:0] bits (**TCF3, 08H**)
- (2). Specify the sample address in the selected UI by SAMP [3:0] bits (**TCF3, 08H**)
- (3). Write sample data to WDAT[6:0] bits (**TCF4, 09H**). It contains the data to be stored in the RAM, addressed by the selected UI and the corresponding sample address.
- (4). Set the RW bit (**TCF3, 08H**) to '0' to implement writing data to RAM, or to '1' to implement read data from RAM
- (5). Implement the Read from RAM/Write to RAM by setting the DONE bit (**TCF3, 08H**)

Repeat the above steps until all the sample data are written to or read from the internal RAM.

- (6). Write the scaling data to SCAL[5:0] bits (**TCF2, 07H**) to scale the amplitude of the waveform based on the selected standard pulse amplitude

When more than one UI is used to compose the pulse template, the overlap of two consecutive pulses could make the pulse amplitude overflow (exceed the maximum limitation) if the pulse amplitude is not set properly. This overflow is captured by DAC_OV_IS bit (**INTS1, 1AH**), and, if enabled by the DAC_OV_IM bit (**INTM1, 15H**), an interrupt will be generated.

The following tables give all the sample data based on the preset pulse templates and LBOs in detail for reference. For preset pulse templates and LBOs, scaling up/down against the pulse amplitude is not supported.

1. [Table-2](#) Transmit Waveform Value For E1 75 Ω
2. [Table-3](#) Transmit Waveform Value For E1 120 Ω
3. [Table-4](#) Transmit Waveform Value For T1 0~133 ft
4. [Table-5](#) Transmit Waveform Value For T1 133~266 ft
5. [Table-6](#) Transmit Waveform Value For T1 266~399 ft
6. [Table-7](#) Transmit Waveform Value For T1 399~533 ft
7. [Table-8](#) Transmit Waveform Value For T1 533~655 ft
8. [Table-9](#) Transmit Waveform Value For J1 0~655 ft
9. [Table-10](#) Transmit Waveform Value For DS1 0 dB LBO
10. [Table-11](#) Transmit Waveform Value For DS1 -7.5 dB LBO
11. [Table-12](#) Transmit Waveform Value For DS1 -15.0 dB LBO
12. [Table-13](#) Transmit Waveform Value For DS1 -22.5 dB LBO

Table-2 Transmit Waveform Value For E1 75 ohm

Sample	UI 1	UI 2	UI 3	UI 4
1	0000000	0000000	0000000	0000000
2	0000000	0000000	0000000	0000000
3	0000000	0000000	0000000	0000000
4	0001100	0000000	0000000	0000000
5	0110000	0000000	0000000	0000000
6	0110000	0000000	0000000	0000000
7	0110000	0000000	0000000	0000000
8	0110000	0000000	0000000	0000000
9	0110000	0000000	0000000	0000000
10	0110000	0000000	0000000	0000000
11	0110000	0000000	0000000	0000000
12	0110000	0000000	0000000	0000000
13	0000000	0000000	0000000	0000000
14	0000000	0000000	0000000	0000000
15	0000000	0000000	0000000	0000000
16	0000000	0000000	0000000	0000000

SCAL[5:0] = 100001 (default), One step change of this value of SCAL[5:0] results in 3% scaling up/down against the pulse amplitude.

Table-3 Transmit Waveform Value For E1 120 ohm

Sample	UI 1	UI 2	UI 3	UI 4
1	0000000	0000000	0000000	0000000
2	0000000	0000000	0000000	0000000
3	0000000	0000000	0000000	0000000
4	0001111	0000000	0000000	0000000
5	0111100	0000000	0000000	0000000
6	0111100	0000000	0000000	0000000
7	0111100	0000000	0000000	0000000
8	0111100	0000000	0000000	0000000
9	0111100	0000000	0000000	0000000
10	0111100	0000000	0000000	0000000
11	0111100	0000000	0000000	0000000
12	0111100	0000000	0000000	0000000
13	0000000	0000000	0000000	0000000
14	0000000	0000000	0000000	0000000
15	0000000	0000000	0000000	0000000
16	0000000	0000000	0000000	0000000

SCAL[5:0] = 100001 (default), One step change of this value of SCAL[5:0] results in 3% scaling up/down against the pulse amplitude.

Table-4 Transmit Waveform Value For T1 0~133 ft

Sample	UI 1	UI 2	UI 3	UI 4
1	0010111	1000010	0000000	0000000
2	0100111	1000001	0000000	0000000
3	0100111	0000000	0000000	0000000
4	0100110	0000000	0000000	0000000
5	0100101	0000000	0000000	0000000
6	0100101	0000000	0000000	0000000
7	0100101	0000000	0000000	0000000
8	0100100	0000000	0000000	0000000
9	0100011	0000000	0000000	0000000
10	1001010	0000000	0000000	0000000
11	1001010	0000000	0000000	0000000
12	1001001	0000000	0000000	0000000
13	1000111	0000000	0000000	0000000
14	1000101	0000000	0000000	0000000
15	1000100	0000000	0000000	0000000
16	1000011	0000000	0000000	0000000

SCAL[5:0] = 110110¹ (default), One step change of this value of SCAL[5:0] results in 2% scaling up/down against the pulse amplitude.

1. In T1 mode, when arbitrary pulse for short haul application is configured, users should write '110110' to SCAL[5:0] bits if no scaling is required.

Table-5 Transmit Waveform Value For T1 133~266 ft

Sample	UI 1	UI 2	UI 3	UI 4
1	0011011	1000011	0000000	0000000
2	0101110	1000010	0000000	0000000
3	0101100	1000001	0000000	0000000
4	0101010	0000000	0000000	0000000
5	0101001	0000000	0000000	0000000
6	0101000	0000000	0000000	0000000
7	0100111	0000000	0000000	0000000
8	0100110	0000000	0000000	0000000
9	0100101	0000000	0000000	0000000
10	1010000	0000000	0000000	0000000
11	1001111	0000000	0000000	0000000
12	1001101	0000000	0000000	0000000
13	1001010	0000000	0000000	0000000
14	1001000	0000000	0000000	0000000
15	1000110	0000000	0000000	0000000
16	1000100	0000000	0000000	0000000

See Table-4

Table-6 Transmit Waveform Value For T1 266~399 ft

Sample	UI 1	UI 2	UI 3	UI 4
1	0011111	1000011	0000000	0000000
2	0110100	1000010	0000000	0000000
3	0101111	1000001	0000000	0000000
4	0101100	0000000	0000000	0000000
5	0101011	0000000	0000000	0000000
6	0101010	0000000	0000000	0000000
7	0101001	0000000	0000000	0000000
8	0101000	0000000	0000000	0000000
9	0100101	0000000	0000000	0000000
10	1010111	0000000	0000000	0000000
11	1010011	0000000	0000000	0000000
12	1010000	0000000	0000000	0000000
13	1001011	0000000	0000000	0000000
14	1001000	0000000	0000000	0000000
15	1000110	0000000	0000000	0000000
16	1000100	0000000	0000000	0000000

See Table-4

Table-7 Transmit Waveform Value For T1 399-533 ft

Sample	UI 1	UI 2	UI 3	UI 4
1	0100000	1000011	0000000	0000000
2	0111011	1000010	0000000	0000000
3	0110101	1000001	0000000	0000000
4	0101111	0000000	0000000	0000000
5	0101110	0000000	0000000	0000000
6	0101101	0000000	0000000	0000000
7	0101100	0000000	0000000	0000000
8	0101010	0000000	0000000	0000000
9	0101000	0000000	0000000	0000000
10	1011000	0000000	0000000	0000000
11	1011000	0000000	0000000	0000000
12	1010011	0000000	0000000	0000000
13	1001100	0000000	0000000	0000000
14	1001000	0000000	0000000	0000000
15	1000110	0000000	0000000	0000000
16	1000100	0000000	0000000	0000000

See Table-4

Table-8 Transmit Waveform Value For T1 533-655 ft

Sample	UI 1	UI 2	UI 3	UI 4
1	0100000	1000011	0000000	0000000
2	0111111	1000010	0000000	0000000
3	0111000	1000001	0000000	0000000
4	0110011	0000000	0000000	0000000
5	0101111	0000000	0000000	0000000
6	0101110	0000000	0000000	0000000
7	0101101	0000000	0000000	0000000
8	0101100	0000000	0000000	0000000
9	0101001	0000000	0000000	0000000
10	1011111	0000000	0000000	0000000
11	1011110	0000000	0000000	0000000
12	1010111	0000000	0000000	0000000
13	1001111	0000000	0000000	0000000
14	1001001	0000000	0000000	0000000
15	1000111	0000000	0000000	0000000
16	1000100	0000000	0000000	0000000

See Table-4

Table-9 Transmit Waveform Value For J1 0-655 ft

Sample	UI 1	UI 2	UI 3	UI 4
1	0010111	1000010	0000000	0000000
2	0100111	1000001	0000000	0000000
3	0100111	0000000	0000000	0000000
4	0100110	0000000	0000000	0000000
5	0100101	0000000	0000000	0000000
6	0100101	0000000	0000000	0000000
7	0100101	0000000	0000000	0000000
8	0100100	0000000	0000000	0000000
9	0100011	0000000	0000000	0000000
10	1001010	0000000	0000000	0000000
11	1001010	0000000	0000000	0000000
12	1001001	0000000	0000000	0000000
13	1000111	0000000	0000000	0000000
14	1000101	0000000	0000000	0000000
15	1000100	0000000	0000000	0000000
16	1000011	0000000	0000000	0000000

SCAL[5:0] = 110110 (default), One step change of this value of SCAL[5:0] results in 2% scaling up/down against the pulse amplitude.

Table-10 Transmit Waveform Value For DS1 0 dB LBO

Sample	UI 1	UI 2	UI 3	UI 4
1	0010111	1000010	0000000	0000000
2	0100111	1000001	0000000	0000000
3	0100111	0000000	0000000	0000000
4	0100110	0000000	0000000	0000000
5	0100101	0000000	0000000	0000000
6	0100101	0000000	0000000	0000000
7	0100101	0000000	0000000	0000000
8	0100100	0000000	0000000	0000000
9	0100011	0000000	0000000	0000000
10	1001010	0000000	0000000	0000000
11	1001010	0000000	0000000	0000000
12	1001001	0000000	0000000	0000000
13	1000111	0000000	0000000	0000000
14	1000101	0000000	0000000	0000000
15	1000100	0000000	0000000	0000000
16	1000011	0000000	0000000	0000000

SCAL[5:0] = 110110 (default), One step change of this Value results in 2% scaling up/down against the pulse amplitude.

Table-11 Transmit Waveform Value For DS1 -7.5 dB LBO

Sample	UI 1	UI 2	UI 3	UI 4
1	0000000	0010100	0000010	0000000
2	0000010	0010010	0000010	0000000
3	0001001	0010000	0000010	0000000
4	0010011	0001110	0000010	0000000
5	0011101	0001100	0000010	0000000
6	0100101	0001011	0000001	0000000
7	0101011	0001010	0000001	0000000
8	0110001	0001001	0000001	0000000
9	0110110	0001000	0000001	0000000
10	0111010	0000111	0000001	0000000
11	0111001	0000110	0000001	0000000
12	0110000	0000101	0000001	0000000
13	0101000	0000100	0000000	0000000
14	0100000	0000100	0000000	0000000
15	0011010	0000011	0000000	0000000
16	0010111	0000011	0000000	0000000

SCAL[5:0] = 010001 (default), One step change of this value of SCAL[5:0] results in 6.25% scaling up/down against the pulse amplitude.

Table-13 Transmit Waveform Value For DS1 -22.5 dB LBO

Sample	UI 1	UI 2	UI 3	UI 4
1	0000000	0101100	0011110	0001000
2	0000000	0101110	0011100	0000111
3	0000000	0110000	0011010	0000110
4	0000000	0110001	0011000	0000101
5	0000001	0110010	0010111	0000101
6	0000011	0110010	0010101	0000100
7	0000111	0110010	0010100	0000100
8	0001011	0110001	0010011	0000011
9	0001111	0110000	0010001	0000011
10	0010101	0101110	0010000	0000010
11	0011001	0101100	0001111	0000010
12	0011100	0101001	0001110	0000010
13	0100000	0100111	0001101	0000001
14	0100011	0100100	0001100	0000001
15	0100111	0100010	0001010	0000001
16	0101010	0100000	0001001	0000001

SCAL[5:0] = 000100 (default), One step change of this value of SCAL[5:0] results in 25% scaling up/down against the pulse amplitude.

Table-12 Transmit Waveform Value For DS1 -15.0 dB LBO

Sample	UI 1	UI 2	UI 3	UI 4
1	0000000	0110101	0001111	0000011
2	0000000	0110011	0001101	0000010
3	0000000	0110000	0001100	0000010
4	0000001	0101101	0001011	0000010
5	0000100	0101010	0001010	0000010
6	0001000	0100111	0001001	0000001
7	0001110	0100100	0001000	0000001
8	0010100	0100001	0000111	0000001
9	0011011	0011110	0000110	0000001
10	0100010	0011100	0000110	0000001
11	0101010	0011010	0000101	0000001
12	0110000	0010111	0000101	0000001
13	0110101	0010101	0000100	0000001
14	0110111	0010100	0000100	0000000
15	0111000	0010010	0000011	0000000
16	0110111	0010000	0000011	0000000

SCAL[5:0] = 001000 (default), One step change of the value of SCAL[5:0] results in 12.5% scaling up/down against the pulse amplitude.

3.3.4 TRANSMIT PATH LINE INTERFACE

The transmit line interface consists of TTIP pin and TRING pin. The impedance matching can be realized by the internal impedance matching circuit or the external impedance matching circuit. If T_TERM[2] is set to '0', the internal impedance matching circuit will be selected. In this case, the T_TERM[1:0] bits (**TERM, 03H**) can be set to choose 75 Ω , 100 Ω , 110 Ω or 120 Ω internal impedance of TTIP/TRING. If T_TERM[2] is set to '1', the internal impedance matching circuit will be disabled. In this case, the external impedance matching circuit will be used to realize the impedance matching. For T1/J1 mode, the external impedance matching circuit for the transmitter is not supported. [Figure-8](#) shows the appropriate external components to connect with the cable. [Table-14](#) is the list of the recommended impedance matching for transmitter.

In hardware control mode, TERM pin can be used to select impedance matching for both receiver and transmitter. If TERM pin is low, external impedance network will be used for impedance matching. If TERM pin is high, internal impedance will be used for impedance matching and

PULS[3:0] pins will be set to select the specific internal impedance. Refer to [5 Hardware Control Pin Summary](#) for details.

The TTIP/TRING pins can also be turned into high impedance by setting the THZ bit (**TCF1, 06H**) to '1'. In this state, the internal transmit circuits are still active.

In hardware control mode, TTIP/TRING can be turned into high impedance by pulling THZ pin to high. Refer to [5 Hardware Control Pin Summary](#) for details.

Besides, in the following cases, both TTIP/TRING pins will also become high impedance:

- Loss of MCLK;
- Loss of TCLK (exceptions: Remote Loopback; Transmit internal pattern by MCLK);
- Transmit path power down;
- After software reset; pin reset and power on.

Table-14 Impedance Matching for Transmitter

Cable Configuration	Internal Termination			External Termination		
	T_TERM[2:0]	PULS[3:0]	R _T	T_TERM[2:0]	PULS[3:0]	R _T
E1/75 Ω	000	0000	0 Ω	1XX	0001	9.4 Ω
E1/120 Ω	001	0001			0001	
T1/0~133 ft	010	0010		-	-	-
T1/133~266 ft		0011				
T1/266~399 ft		0100				
T1/399~533 ft		0101				
T1/533~655 ft		0110				
J1/0~655 ft		011				
0 dB LBO	010	1000		-	-	-
-7.5 dB LBO		1001				
-15.0 dB LBO		1010				
-22.5 dB LBO		1011				

Note: The precision of the resistors should be better than $\pm 1\%$

3.3.5 TRANSMIT PATH POWER DOWN

The transmit path can be powered down by setting the T_OFF bit (**TCF0, 05H**) to '1'. In this case, the TTIP/TRING pins are turned into high impedance.

In hardware control mode, the transmit path can be powered down by pulling both PATT1 and PATT0 pins to high. Refer to [5 Hardware Control Pin Summary](#) for details.

3.4 RECEIVE PATH

The receive path consists of Receive Internal Termination, Monitor Gain, Amplitude/Wave Shape Detector, Digital Tuning Controller, Adaptive Equalizer, Data Slicer, CDR (Clock & Data Recovery), Optional Jitter Attenuator, Decoder and LOS/AIS Detector. Refer to Figure-7.

3.4.1 RECEIVE INTERNAL TERMINATION

The impedance matching can be realized by the internal impedance matching circuit or the external impedance matching circuit. If R_TERM[2]

is set to '0', the internal impedance matching circuit will be selected. In this case, the R_TERM[1:0] bits (TERM, 03H) can be set to choose 75 Ω, 100 Ω, 110 Ω or 120 Ω internal impedance of RTIP/RRING. If R_TERM[2] is set to '1', the internal impedance matching circuit will be disabled. In this case, the external impedance matching circuit will be used to realize the impedance matching. Figure-8 shows the appropriate external components to connect with the cable. Table-15 is the list of the recommended impedance matching for receiver.

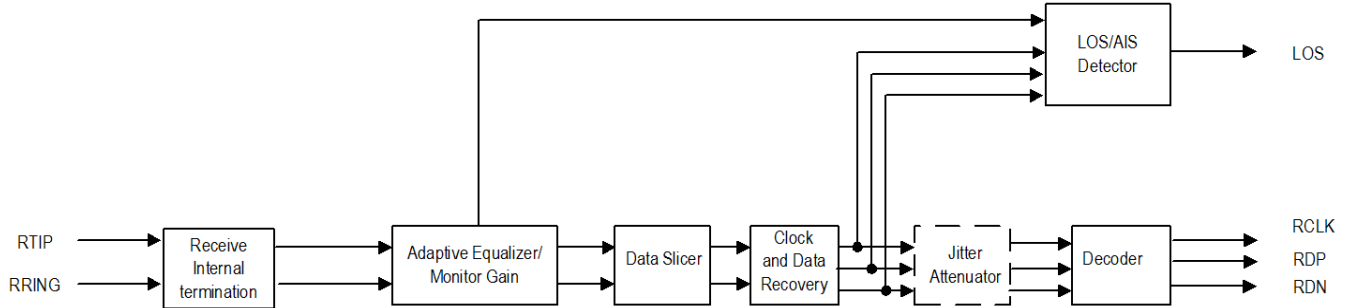
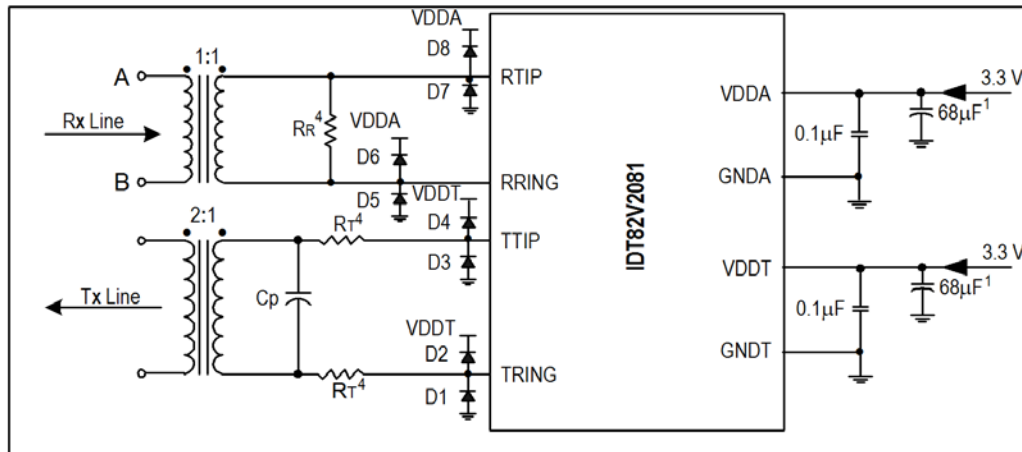


Figure-7 Receive Monitor Gain Adaptive Equalizer

Table-15 Impedance Matching for Receiver

Cable Configuration	Internal Termination		External Termination	
	R_TERM[2:0]	R _R	R_TERM[2:0]	R _R
E1/75 Ω	000	120 Ω	1XX	75 Ω
E1/120 Ω	001			120 Ω
T1	010			100 Ω
J1	011			110 Ω



- Note: 1. Common decoupling capacitor, one per chip
 2. Cp 0-560 (pF)
 3. D1 - D8, Motorola - MBR0540T1; International Rectifier - 11DQ04 or 10BQ060
 4. R_T/R_R : refer to Table-14 and Table-15 respectively for R_T and R_R values

Figure-8 Transmit/Receive Line Circuit

In hardware control mode, TERM and PULS[3:0] pins can be used to select impedance matching for both receiver and transmitter. If TERM pin is low, external impedance network will be used for impedance matching. If TERM pin is high, internal impedance will be used for impedance matching and PULS[3:0] pins can be set to select the specific internal impedance. Refer to [5 Hardware Control Pin Summary](#) for details.

3.4.2 LINE MONITOR

In both T1/J1 and E1 short haul applications, the non-intrusive monitoring on channels located in other chips can be performed by tapping the monitored channel through a high impedance bridging circuit. Refer to [Figure-9](#) and [Figure-11](#).

After a high resistance bridging circuit, the signal arriving at the RTIP/RRING is dramatically attenuated. To compensate this attenuation, the Monitor Gain can be used to boost the signal by 22 dB, 26 dB and 32 dB, selected by MG[1:0] bits (**RCF2, OCH**). For normal operation, the Monitor Gain should be set to 0 dB.

In hardware control mode, MONT pin can be used to set the Monitor Gain. When MONT pin is low, the Monitor Gain is 0 dB. When MONT pin is high, the Monitor Gain is 26 dB. Refer to [5 Hardware Control Pin Summary](#) for details.

Note that LOS indication is not supported if the device is operated in Line Monitor Mode

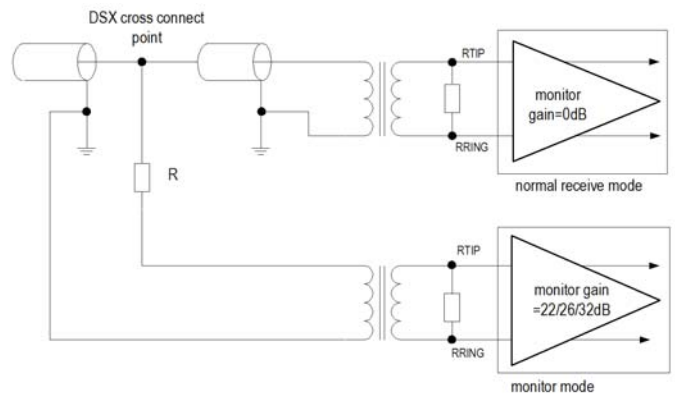


Figure-9 Monitoring Receive Line in Another Chip

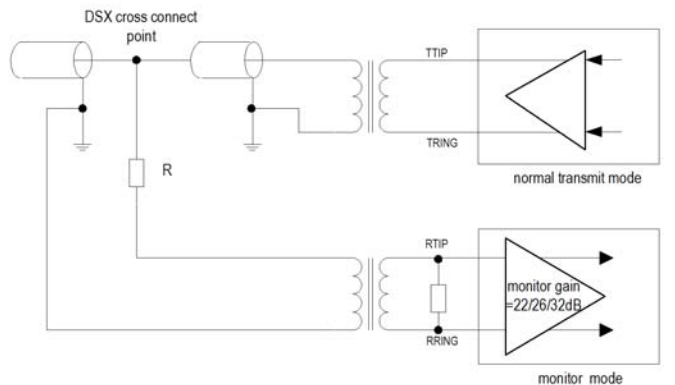


Figure-10 Monitor Transmit Line in Another Chip

3.4.3 ADAPTIVE EQUALIZER

The Adaptive Equalizer can remove most of the signal distortion due to intersymbol interference caused by cable attenuation. It can be enabled or disabled by setting EQ_ON bit to '1' or '0' (**RCF1, 0BH**).

When the adaptive equalizer is out of range, EQ_S bit (**STAT0, 17H**) will be set to '1' to indicate the status of equalizer. If EQ_IES bit (**INTES, 16H**) is set to '1', any changes of EQ_S bit will generate an interrupt and EQ_IS bit (**INTS0, 19H**) will be set to '1' if it is not masked. If EQ_IES is set to '0', only the '0' to '1' transition of the EQ_S bit will generate an interrupt and EQ_IS bit will be set to '1' if it is not masked. The EQ_IS bit will be reset after being read.

The Amplitude/wave shape detector keeps on measuring the amplitude/wave shape of the incoming signals during an observation period. This observation period can be 32, 64, 128 or 256 symbol periods, as selected by UPDW[1:0] bits (**RCF2, 0CH**). A shorter observation period allows quicker responses to pulse amplitude variation while a longer observation period can minimize the possible overshoots. The default observation period is 128 symbol periods.

Based on the observed peak value for a period, the equalizer will be adjusted to achieve a normalized signal. LATT[4:0] bits (**STAT1, 18H**) indicate the signal attenuation introduced by the cable in approximately 2 dB per step.

3.4.4 RECEIVE SENSITIVITY

For short haul application, the Receive Sensitivity for both E1 and T1/J1 is -10 dB. For long haul application, the receive sensitivity is -43 dB for E1 and -36 dB for T1/J1.

When the chip is configured by hardware, the short haul or long haul operating mode can be selected by setting EQ pin. For short haul mode, the Receive Sensitivity for both E1 and T1/J1 is -10 dB. For long haul mode, the receive sensitivity is -43 dB for E1 and -36 dB for T1/J1. Refer to [5 Hardware Control Pin Summary](#) for details.

3.4.5 DATA SLICER

The Data Slicer is used to generate a standard amplitude mark or a space according to the amplitude of the input signals. The threshold can be 40%, 50%, 60% or 70%, as selected by the SLICE[1:0] bits (**RCF2, 0CH**). The output of the Data Slicer is forwarded to the CDR (Clock & Data Recovery) unit or to the RDP/RDN pins directly if the CDR is disabled.

3.4.6 CDR (CLOCK & DATA RECOVERY)

The CDR is used to recover the clock and data from the received signal. The recovered clock tracks the jitter in the data output from the Data Slicer and keeps the phase relationship between data and clock during the absence of the incoming pulse. The CDR can also be by-passed in the Dual Rail mode. When CDR is by-passed, the data from the Data Slicer is output to the RDP/RDN pins directly.

3.4.7 DECODER

In T1/J1 applications, the R_MD[1:0] bits (**RCF0, 0AH**) is used to select the AMI decoder or B8ZS decoder. In E1 applications, the R_MD[1:0] bits (**RCF0, 0AH**) are used to select the AMI decoder or HDB3 decoder.

When the chip is configured by hardware, the operation mode of receive and transmit path can be selected by setting RXTXM1 and RXTXM0 pins. Refer to [5 Hardware Control Pin Summary](#) for details.