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DUAL CHANNEL T1/E1/J1 LONG HAUL/SHORT HAUL LINE INTERFACE UNIT

IDT82V2082

FEATURES:

- **Dual channel T1/E1/J1 long haul/short haul line interfaces**
- **Supports HPS (Hitless Protection Switching) for 1+1 protection without external relays**
- **Receiver sensitivity exceeds -36 dB@772KHz and -43 dB@1024 KHz**
- **Programmable T1/E1/J1 switchability allowing one bill of material for any line condition**
- **Single 3.3 V power supply with 5 V tolerance on digital interfaces**
- **Meets or exceeds specifications in**
  - ANSI T1.102, T1.403 and T1.408
  - ITU I.431, G.703, G.736, G.775 and G.823
  - ETSI 300-166, 300-233 and TBR12/13
  - AT&T Pub 62411
- **Software programmable or hardware selectable on:**
  - Wave-shaping templates for short haul and long haul LBO (Line Build Out)
  - Line terminating impedance (T1:100 Ω, J1:110 Ω, E1: 75 Ω/120 Ω)
  - Adjustment of arbitrary pulse shape
  - JA (Jitter Attenuator) position (receive path or transmit path)
  - Single rail/dual rail system interfaces
  - B8ZS/HDB3/AMI line encoding/decoding
  - Active edge of transmit clock (TCLK) and receive clock (RCLK)
  - Active level of transmit data (TDATA) and receive data (RDATA)
  - Receiver or transmitter power down
  - High impedance setting for line drivers
  - PRBS (Pseudo Random Bit Sequence) generation and detection with 2^{15}-1 PRBS polynomials for E1
  - QRSS (Quasi Random Sequence Signals) generation and detection with 2^{20}-1 QRSS polynomials for T1/J1
  - 16-bit BPV (Bipolar Pulse Violation) / Excess Zero/ PRBS or QRSS error counter
  - Analog loopback, Digital loopback, Remote loopback and Inband loopback
- **Cable attenuation indication**
- **Adaptive receive sensitivity**
- **Non-intrusive monitoring per ITU G.772 specification**
- **Short circuit protection and internal protection diode for line drivers**
- **LOS (Loss Of Signal) and AIS (Alarm Indication Signal) detection**
- **JTAG interface**
- **Supports serial control interface, Motorola and Intel Non-Multiplexed interfaces and hardware control mode**
- **Pin compatible to 82V2042E T1/E1/J1 Short Haul LIU and 82V2052E E1 Short Haul LIU**
- **Available in 80-pin TQFP and 81-pin FPBGA**
  Green package options available

DESCRIPTION:

The IDT82V2082 can be configured as a dual channel T1, E1 or J1 Line Interface Unit. In receive path, an Adaptive Equalizer is integrated to remove the distortion introduced by the cable attenuation. The IDT82V2082 also performs clock/data recovery, AMI/B8ZS/HDB3 line decoding and detects and reports the LOS conditions. In transmit path, there is an AMI/B8ZS/HDB3 encoder, Waveform Shaper and LBOs. There is one Jitter Attenuator, which can be placed in either the receive path or the transmit path. The Jitter Attenuator can also be disabled. The IDT82V2082 supports both Single Rail and Dual Rail system interfaces. To facilitate the network maintenance, a PRBS/QRSS generation/detection circuit is integrated in the chip, and different types of loopbacks can be set according to the applications. Four different kinds of line terminating impedance, 75 Ω,100 Ω, 110 Ω and 120 Ω are selectable on a per channel basis. The chip also provides driver short-circuit protection and internal protection diode and supports JTAG boundary scanning. The chip can be controlled by either software or hardware.

The IDT82V2082 can be used in LAN, WAN, Routers, Wireless Base Stations, IADs, IMAs, IMAPs, Gateways, Frame Relay Access Devices, CSU/DSU equipment, etc.

FUNCTIONAL BLOCK DIAGRAM

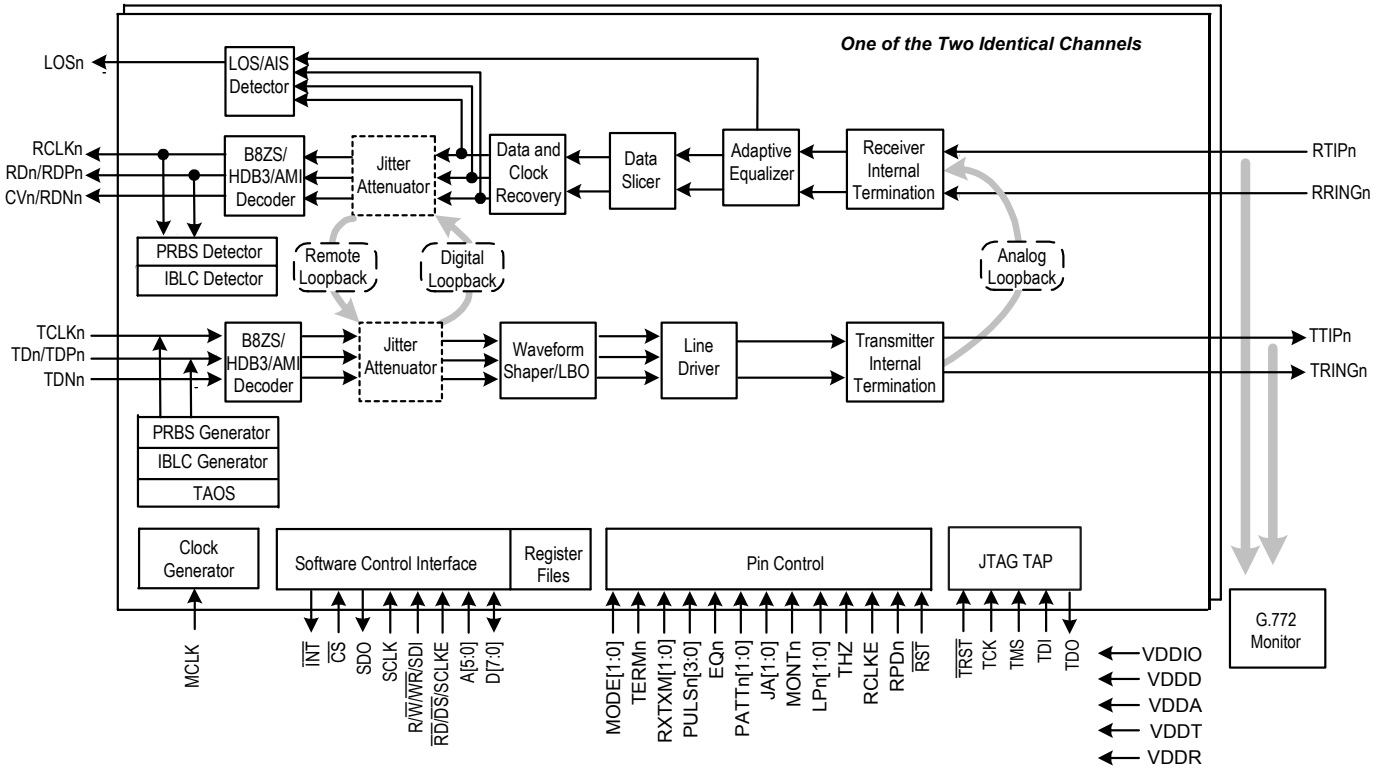

Figure-1 Block Diagram

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1 IDT82V2082 PIN CONFIGURATIONS

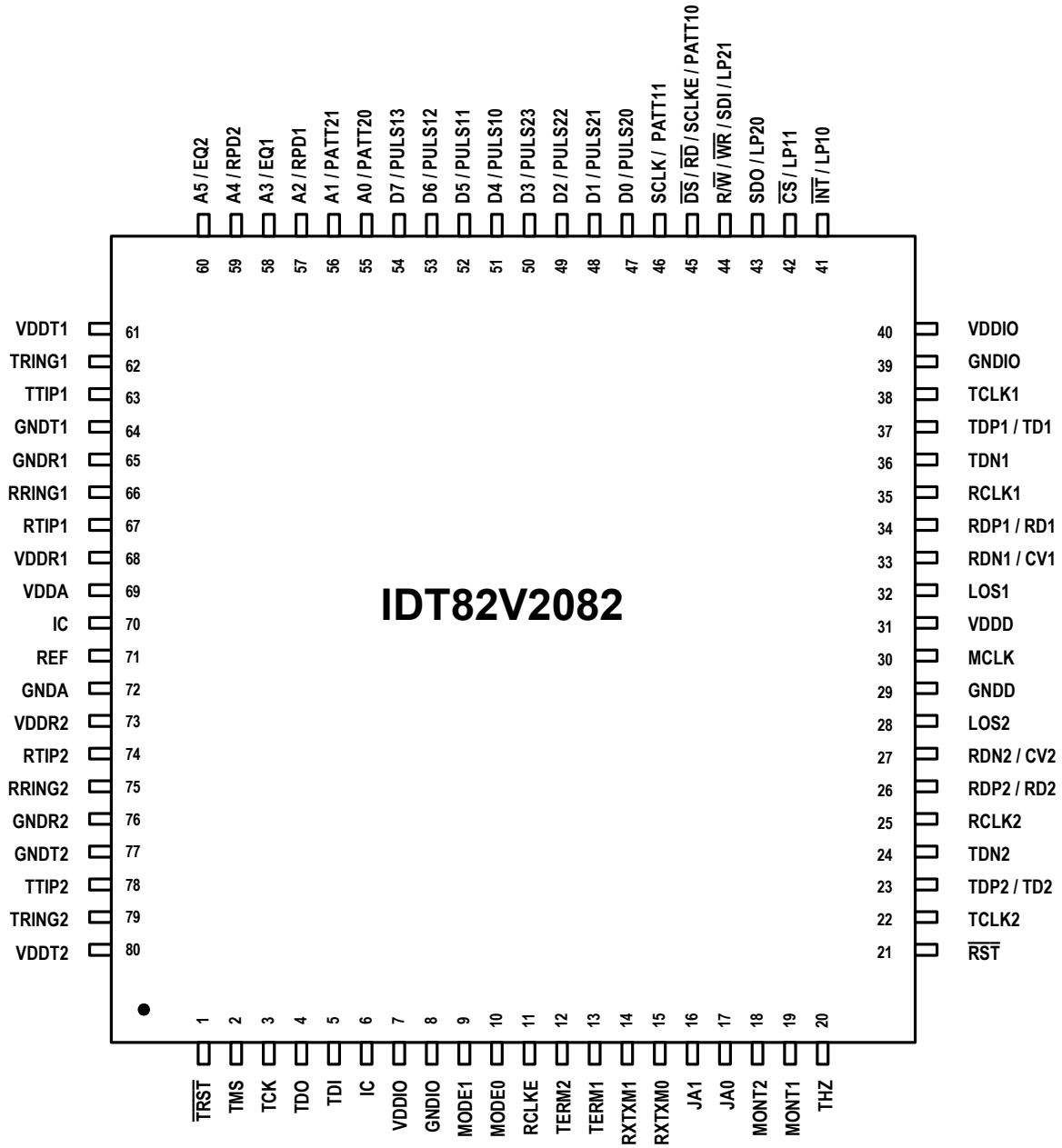

Figure-2 IDT82V2082 TQFP80 Package Pin Assignment

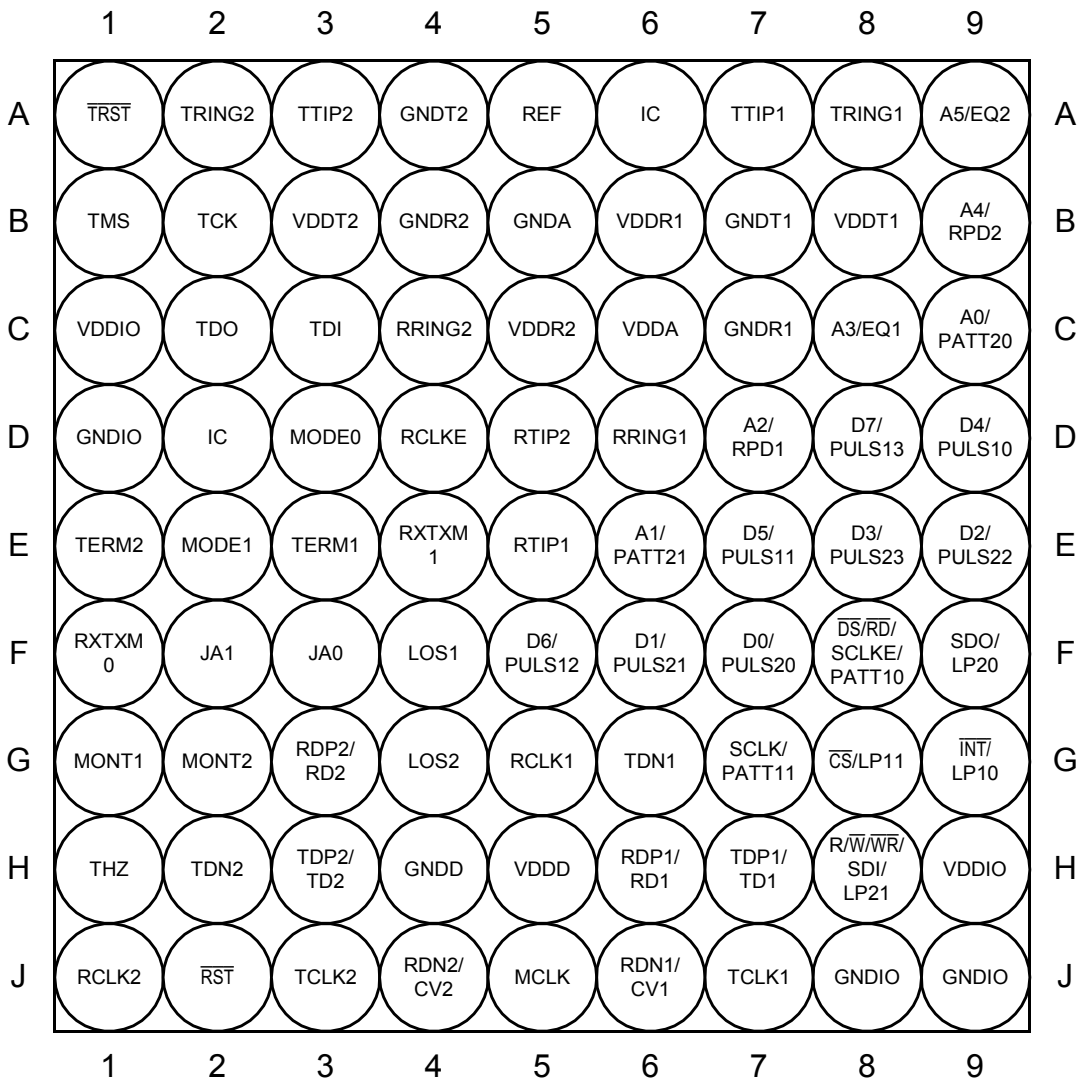

Figure-3 IDT82V2082 FPBGA81 Package Pin Assignment (Top View)

2 PIN DESCRIPTION

Table-1 Pin Description

Name	Type	TQFP80 Pin No.	FPBGA81 Pin No.	Description
TTIP1 TTIP2 TRING1 TRING2	Analog Output	63 78 62 79	A7 A3 A8 A2	**TTIPn[1]/TRINGn: Transmit Bipolar Tip/Ring for Channel 1~2** These pins are the differential line driver outputs and can be set to high impedance state globally or individually. A logic high on THZ pin turns all these pins into high impedance state. When THZ bit (**TCF1, 03H...**)[2] is set to '1', the TTIPn/TRINGn in the corresponding channel is set to high impedance state. In summary, these pins will become high impedance in the following conditions: • THZ pin is high: all TTIPn/TRINGn enter high impedance; • THZn bit is set to 1: the corresponding TTIPn/TRINGn become high impedance; • Loss of MCLK: all TTIPn/TRINGn pins become high impedance; • Loss of TCLKn: the corresponding TTIPn/TRINGn become HZ (exceptions: Remote Loopback; Transmit internal pattern by MCLK); • Transmitter path power down: the corresponding TTIPn/TRINGn become high impedance; • After software reset; pin reset and power on: all TTIPn/TRINGn enter high impedance.
RTIP1 RTIP2 RRING1 RRING2	Analog Input	67 74 66 75	E5 D5 D6 C4	**RTIPn/RRINGn: Receive Bipolar Tip/Ring for Channel 1~2** These signals are the differential receiver inputs.
TD1/TDP1 TD2/TDP2 TDN1 TDN2	I	37 23 36 24	H7 H3 G6 H2	**TDn: Transmit Data for Channel 1~2** When the device is in single rail mode, the NRZ data to be transmitted is input on this pin. Data on TDn pin is sampled into the device on the active edge of TCLKn and is encoded by AMI, HDB3 or B8ZS line code rules before being transmitted. In this mode, TDNn should be connected to ground. **TDPn/TDNn: Positive/Negative Transmit Data** When the device is in dual rail mode, the NRZ data to be transmitted for positive/negative pulse is input on these pins. Data on TDPn/TDNn pin is sampled into the device on the active edge of TCLKn. The active polarity is also selectable. Refer to 3.3.1 TRANSMIT PATH SYSTEM INTERFACE for details. The line code in dual rail mode is as follows: TDPn / TDNn / Output Pulse 0 / 0 / Space 0 / 1 / Positive Pulse 1 / 0 / Negative Pulse 1 / 1 / Space
TCLK1 TCLK2	I	38 22	J7 J3	**TCLKn: Transmit Clock for Channel 1~2** This pin inputs 1.544 MHz for T1/J1 mode or 2.048 MHz for E1 mode transmit clock. The transmit data at TDn/TDPn or TDNn is sampled into the device on the active edge of TCLKn. If TCLKn is missing[3] and the TCLKn missing interrupt is not masked, an interrupt will be generated.

Notes:

1. The footprint 'n' (n = 1~2) represents one of the two channels.
2. The name and address of the registers that contain the preceding bit. Only the address of channel 1 register is listed, the rest addresses are represented by '...'. Users can find these omitted addresses in the *Register Description* section.
3. TCLKn missing: the state of TCLKn continues to be high level or low level over 70 MCLK cycles.

Table-1 Pin Description (Continued)

Name	Type	TQFP80 Pin No.	FPBGA81 Pin No.	Description
RD1/ RDP1 RD2/ RDP2 CV1/ RDN1 CV2/ RDN2	O	34 26 33 27	H6 G3 J6 J4	**RDn: Receive Data output for Channel 1~2** In single rail mode, this pin outputs NRZ data. The data is decoded according to AMI, HDB3 or B8ZS line code rules. **CVn: Code Violation indication** In single rail mode, the BPV/CV errors in received data stream will be reported by driving the CVn pin to high level for a full clock cycle. B8ZS/HDB3 line code violation can be indicated if the B8ZS/HDB3 decoder is enabled. When AMI decoder is selected, bipolar violation will be indicated. In hardware control mode, the EXZ, BPV/CV errors in received data stream are always monitored by the CVn pin if single rail mode is chosen. **RDPn/RDNn: Positive/Negative Receive Data output for Channel 1~2** In dual rail mode, these pins output the re-timed NRZ data when CDR is enabled, or directly outputs the raw RZ slicer data if CDR is bypassed. **Active edge and level select:** Data on RDPn/RDNn or RDn is clocked with either the rising or the falling edge of RCLKn. The active polarity is also selectable. Refer to 3.4.8 RECEIVE PATH SYSTEM INTERFACE for details.
RCLK1 RCLK2	O	35 25	G5 J1	**RCLKn: Receive Clock output for Channel 1~2** This pin outputs 1.544 MHz for T1/J1 mode or 2.048 MHz for E1 mode receive clock. Under LOS conditions with AIS enabled (bit AISE=1), RCLKn is derived from MCLK. In clock recovery mode, this signal provides the clock recovered from the RTIPn/RRINGn signal. The receive data (RDn in single rail mode or RDPn and RDNn in dual rail mode) is clocked out of the device on the active edge of RCLKn. If clock recovery is bypassed, RCLKn is the exclusive OR (XOR) output of the dual rail slicer data RDPn and RDNn. This signal can be used in applications with external clock recovery circuitry.
MCLK	I	30	J5	**MCLK: Master Clock input** A built-in clock system that accepts selectable 2.048 MHz reference for E1 operating mode and 1.544 MHz reference for T1/J1 operating mode. This reference clock is used to generate several internal reference signals: • Timing reference for the integrated clock recovery unit. • Timing reference for the integrated digital jitter attenuator. • Timing reference for microcontroller interface. • Generation of RCLKn signal during a loss of signal condition. • Reference clock to transmit All Ones, all zeros, PRBS/QRSS pattern as well as activate or deactivate Inband Loopback code if MCLK is selected as the reference clock. Note that for ATAO and AIS, MCLK is always used as the reference clock. • Reference clock during Transmit All Ones (TAO) condition or sending PRBS/QRSS in hardware control mode. The loss of MCLK will turn TTIP/TRING into high impedance status.
LOS1 LOS2	O	32 28	F4 G4	**LOSn: Loss of Signal Output for Channel 1~2** These pins are used to indicate the loss of received signals. When LOSn pin becomes high, it indicates the loss of received signal in channel n. The LOS pin will become low automatically when valid received signal is detected again. The criteria of loss of signal are described in 3.6 LOS AND AIS DETECTION.
REF	I	71	A5	**REF: reference resister** An external resistor (3kΩ, 1%) is used to connect this pin to ground to provide a standard reference current for internal circuit.

Table-1 Pin Description (Continued)

<table>
<tr><th>Name</th><th>Type</th><th>TQFP80 Pin No.</th><th>FPBGA81 Pin No.</th><th>Description</th></tr>
<tr><td>MODE1
MODE0</td><td>I</td><td>9
10</td><td>E2
D3</td><td>MODE[1:0]: operation mode of control interface select
The level on this pin determines which control mode is used to control the device as follows:

<table><tr><th>MODE[1:0]</th><th>Control Interface mode</th></tr><tr><td>00</td><td>Hardware interface</td></tr><tr><td>01</td><td>Serial Microcontroller Interface</td></tr><tr><td>10</td><td>Motorola non-multiplexed</td></tr><tr><td>11</td><td>Intel non-multiplexed</td></tr></table>• The serial microcontroller interface consists of $\overline{CS}$, SCLK, SCLKE, SDI, SDO and $\overline{INT}$ pins. SCLKE is used for the selection of the active edge of SCLK.
• The parallel non-multiplexed microcontroller interface consists of $\overline{CS}$, A[5:0], D[7:0], $\overline{DS}$/$\overline{RD}$, R/$\overline{W}$/$\overline{WR}$ and $\overline{INT}$ pins. (Refer to 3.12 MICROCONTROLLER INTERFACES for details)
• Hardware interface consists of PULSn[3:0], THZ, RCLKE, LPn[1:0], PATTn[1:0], JA[1:0], MONTn, TERMn, EQn, RPDn, MODE[1:0] and RXTXM[1:0] (n=1, 2).</td></tr>
<tr><td>RCLKE</td><td>I</td><td>11</td><td>D4</td><td>RCLKE: the active edge of RCLKn select
In hardware control mode, this pin selects the active edge of RCLKn
• L= update RDPn/RDNn on the rising edge of RCLKn
• H= update RDPn/RDNn on the falling edge of RCLKn
In software control mode, this pin should be connected to GNDIO.</td></tr>
<tr><td>RXTXM1
RXTXM0</td><td>I</td><td>14
15</td><td>E4
F1</td><td>RXTXM[1:0]: Receive and transmit path operation mode select
In hardware control mode, these pins are used to select the single rail or dual rail operation modes as well as AMI or HDB3/B8ZS line coding:
• 00= single rail with HDB3/B8ZS coding
• 01= single rail with AMI coding
• 10= dual rail interface with CDR enabled
• 11= slicer mode (dual rail interface with CDR disabled)
In software control mode, these pins should be connected to ground.</td></tr>
<tr><td>$\overline{CS}$

LP11</td><td>I</td><td>42</td><td>G8</td><td>$\overline{CS}$: Chip Select
In serial or parallel microcontroller interface mode, this is the active low enable signal. A low level on this pin enables serial or parallel microcontroller interface.

LP11/LP10: Loopback mode select for channel 1
When the chip is configured by hardware, this pin is used to select loopback operation modes for channel 1 (Inband Loopback is not provided in hardware control mode).
• 00 = no loopback
• 01 = analog loopback
• 10 = digital loopback
• 11 = remote loopback</td></tr>
<tr><td>$\overline{INT}$

LP10</td><td>O

I</td><td>41</td><td>G9</td><td>$\overline{INT}$: Interrupt Request
In software control mode, this pin outputs the general interrupt request for all interrupt sources. If INTM_GLB bit (GCF, 20H) is set to ‘1’, all the interrupt sources will be masked. These interrupt sources can be masked individually via registers (INTM0, 13H...) and (INTM1, 14H...). The interrupt status is reported via the registers (INTCH, 21H), (INTS0, 18H...) and (INTS1, 19H...).

Output characteristics of this pin can be defined to be push-pull (active high or active low) or open-drain (active low) by setting bits INT_PIN[1:0] (GCF, 20H)

LP11/LP10: Loopback mode select for channel 1
See above LP11.</td></tr>
</table>

Table-1 Pin Description (Continued)

<table>
<tr><th>Name</th><th>Type</th><th>TQFP80 Pin No.</th><th>FPBGA81 Pin No.</th><th>Description</th></tr>
<tr><td>SCLK</td><td>I</td><td>46</td><td>G7</td><td>SCLK: Shift Clock
In serial microcontroller interface mode, this signal is the shift clock for the serial interface. Configuration data on SDI pin is sampled on the rising edge of SCLK. Configuration and status data on SDO pin is clocked out of the device on the rising edge of SCLK if SCLKE pin is low, or on the falling edge of SCLK if SCLKE pin is high.
In parallel non-multiplexed interface mode, this pin should be connected to ground.</td></tr>
<tr><td>PATT11</td><td></td><td></td><td></td><td>PATT11/PATT10: Transmit pattern select for channel 1
In hardware control mode, this pin selects the transmit pattern
• 00 = normal
• 01= All Ones
• 10= PRBS
• 11= transmitter power down</td></tr>
<tr><td>SCLKE</td><td>I</td><td>45</td><td>F8</td><td>SCLKE: Serial Clock Edge Select
In serial microcontroller interface mode, this signal selects the active edge of SCLK for outputting SDO. The output data is valid after some delay from the active clock edge. It can be sampled on the opposite edge of the clock. The active clock edge which clocks the data out of the device is selected as shown below:
<table><tr><th>SCLKE</th><th>SCLK</th></tr><tr><td>Low</td><td>Rising edge is the active edge.</td></tr><tr><td>High</td><td>Falling edge is the active edge.</td></tr></table></td></tr>
<tr><td>$\overline{DS}$</td><td></td><td></td><td></td><td>$\overline{DS}$: Data Strobe
In Motorola parallel non-multiplexed interface mode, this signal is the data strobe of the parallel interface. In a write operation (R/$\overline{W}$ = 0), the data on D[7:0] is sampled into the device. In a read operation (R/$\overline{W}$ = 1), the data is driven to D[7:0] by the device.</td></tr>
<tr><td>$\overline{RD}$</td><td></td><td></td><td></td><td>$\overline{RD}$: Read Strobe
In Intel parallel non-Multiplexed interface mode, the data is driven to D[7:0] by the device during low level of $\overline{RD}$ in a read operation.</td></tr>
<tr><td>PATT10</td><td></td><td></td><td></td><td>PATT11/PATT10: Transmit pattern select for channel 1
See above PATT11.</td></tr>
<tr><td>SDI</td><td>I</td><td>44</td><td>H8</td><td>SDI: Serial Data Input
In serial microcontroller interface mode, this signal is the input data to the serial interface. Configuration data at SDI pin is sampled by the device on the rising edge of SCLK.</td></tr>
<tr><td>R/$\overline{W}$</td><td></td><td></td><td></td><td>R/$\overline{W}$: Read/Write Select
In Motorola parallel non-multiplexed interface mode, this pin is low for write operation and high for read operation.</td></tr>
<tr><td>$\overline{WR}$</td><td></td><td></td><td></td><td>$\overline{WR}$: Write Strobe
In Intel parallel non-multiplexed interface mode, this pin is asserted low by the microcontroller to initiate a write cycle. The data on D[7:0] is sampled into the device in a write operation.</td></tr>
<tr><td>LP21</td><td></td><td></td><td></td><td>LP21/LP20: loopback mode select for channel 2
When the chip is configured by hardware, this pin is used to select loopback operation modes for channel 2 (Inband Loopback is not provided in hardware control mode).
• 00 = no loopback
• 01 = analog loopback
• 10 = digital loopback
• 11 = remote loopback</td></tr>
</table>

Table-1 Pin Description (Continued)

Name	Type	TQFP80 Pin No.	FPBGA81 Pin No.	Description
SDO	O	43	F9	**SDO: Serial Data Output** In serial microcontroller interface mode, this signal is the output data of the serial interface. Configuration or Status data at SDO pin is clocked out of the device on the rising edge of SCLK if SCLKE pin is low, or on the falling edge of SCLK if SCLKE pin is high. In parallel non-multiplexed interface mode, this pin should be left open.
LP20	I			**LP21/LP20: loopback mode select for channel 2** See above LP21.
D7	I/O	54	D8	**D7: Data Bus bit7** In Intel/Motorola non-multiplexed interface mode, this signal is the bi-directional data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor.
PULS13	I			**PULS1[3:0]: these pins are used to select the following functions for channel 1 in hardware control mode:** • T1/E1/J1 mode • Transmit pulse template • Internal termination impedance (75Ω/120Ω/100Ω/110Ω) Refer to 5 HARDWARE CONTROL PIN SUMMARY for details. Note that PULS13 to PULS10 determine the T1/E1/J1 mode of common block.
D6	I/O	53	F5	**D6: Data Bus bit6** In Intel/Motorola non-multiplexed interface mode, this signal is the bi-directional data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor.
PULS12	I			See above.
D5	I/O	52	E7	**D5: Data Bus bit5** In Intel/Motorola non-multiplexed interface mode, this signal is the bi-directional data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor.
PULS11	I			See above.
D4	I/O	51	D9	**D4: Data Bus bit4** In Intel/Motorola non-multiplexed interface mode, this signal is the bi-directional data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor.
PULS10	I			See above.
D3	I/O	50	E8	**D3: Data Bus bit3** In Intel/Motorola non-multiplexed interface mode, this signal is the bi-directional data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor.
PULS23	I			**PULS2[3:0]: these pins are used to select the following functions for channel 2 in hardware control mode:** • T1/E1/J1 mode • Transmit pulse template • Internal termination impedance (75 Ω/120 Ω/100 Ω/110 Ω) Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.
D2	I/O	49	E9	**D2: Data Bus bit2** In Intel/Motorola non-multiplexed interface mode, this signal is the bi-directional data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor.
PULS22	I			See above.
D1	I/O	48	F6	**D1: Data Bus bit1** In Intel/Motorola non-multiplexed interface mode, this signal is the bi-directional data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor.
PULS21	I			See above.

Table-1 Pin Description (Continued)

Name	Type	TQFP80 Pin No.	FPBGA81 Pin No.	Description
D0	I/O	47	F7	**D0: Data Bus bit0** In Intel/Motorola non-multiplexed interface mode, this signal is the bi-directional data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor.
PULS20	I			See above.
A5	I	60	A9	**A5: Address Bus bit5** In Intel/Motorola non-multiplexed interface mode, this signal is the address bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground.
EQ2				**EQ2: Equalizer on/off for receiver2 in hardware control mode** 0= short haul (10 dB) 1= long haul (36 dB for T1/J1, 43 dB for E1)
A4	I	59	B9	**A4: Address Bus bit4** In Intel/Motorola non-multiplexed interface mode, this signal is the address bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground.
RPD2				**RPD2: Power down control for receiver2 in hardware control mode** 0= receiver 2 normal operation 1= receiver 2 power down
A3	I	58	C8	**A3: Address Bus bit3** In Intel/Motorola non-multiplexed interface mode, this signal is the address bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground.
EQ1				**EQ1: Equalizer on/off for receiver1 in hardware control mode** 0= short haul (10 dB) 1= long haul (36 dB for T1/J1, 43 dB for E1)
A2	I	57	D7	**A2: Address Bus bit2** In Intel/Motorola non-multiplexed interface mode, this signal is the address bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground.
RPD1				**RPD1: Power down control for receiver1 in hardware control mode** 0= receiver 1 normal operation 1= receiver 1 power down
A1	I	56	E6	**A1: Address Bus bit1** In Intel/Motorola non-multiplexed interface mode, this signal is the address bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground.
PATT21				**PATT21/PATT20: Transmit pattern select for channel 2** In hardware control mode, this pin selects the transmit pattern 00 = normal 01= All Ones 10= PRBS 11= transmitter power down
A0	I	55	C9	**A0: Address Bus bit 0** In Intel/Motorola non-multiplexed interface mode, this signal is the address bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground.
PATT20				See above

Table-1 Pin Description (Continued)

Name	Type	TQFP80 Pin No.	FPBGA81 Pin No.	Description
TERM1 TERM2	I	13 12	E3 E1	**TERMn: Selects internal or external impedance matching for channel 1 and channel 2 in hardware control mode** 0 = ternary interface with internal impedance matching network 1 = ternary interface with external impedance matching network in E1 mode; ternary interface with external impedance matching network for receiver and ternary interface with internal impedance matching network for transmitter in T1/J1 mode. (This applies to ZB die revision only.) In software control mode, this pin should be connected to ground.
JA1	I	16	F2	**JA[1:0]: Jitter attenuation position, bandwidth and the depth of FIFO select for channel 1 and channel 2 (only used in hardware control mode)** • 00 = JA is disabled • 01= JA in receiver, broad bandwidth, FIFO=64 bits • 10 = JA in receiver, narrow bandwidth, FIFO=128 bits • 11= JA in transmitter, narrow bandwidth, FIFO=128 bits In software control mode, this pin should be connected to ground.
JA0	I	17	F3	See above.
MONT2	I	18	G2	**MONT2: Receive Monitor gain select for channel 2** In hardware control mode with ternary interface, this pin selects the receive monitor gain of receiver: 0= 0dB 1= 26dB In software control mode, this pin should be connected to ground.
MONT1	I	19	G1	**MONT1: Receive Monitor gain select for channel 1** In hardware control mode with ternary interface, this pin selects the receive monitor gain of receiver: 0= 0dB 1= 26dB In software control mode, this pin should be connected to ground.
$\overline{\text{RST}}$	I	21	J2	**$\overline{\text{RST}}$: Hardware Reset** The chip is forced to reset state if a low signal is input on this pin for more than 100ns. MCLK must be active during reset.
THZ	I	20	H1	**THZ: Transmitter Driver High Impedance Enable** This signal enables or disables all transmitter drivers on a global basis. A low level on this pin enables the driver while a high level on this pin places all drivers in high impedance state. Note that the functionality of the internal circuits is not affected by this signal.
JTAG Signals				
$\overline{\text{TRST}}$	I Pullup	1	A1	**$\overline{\text{TRST}}$: JTAG Test Port Reset** This is the active low asynchronous reset to the JTAG Test Port. This pin has an internal pull-up resistor. To ensure deterministic operation of the test logic, TMS should be held high while the signal applied to $\overline{\text{TRST}}$ changes from low to high. For normal signal processing, this pin should be connected to ground. If JTAG is not used, this pin must be connected to ground.
TMS	I Pullup	2	B1	**TMS: JTAG Test Mode Select** This pin is used to control the test logic state machine and is sampled on the rising edge of TCK. TMS has an internal pull-up resistor. If JTAG is not used, this pin may be left unconnected.
TCK	I	3	B2	**TCK: JTAG Test Clock** This is the input clock for JTAG. The data on TDI and TMS are clocked into the device on the rising edge of TCK while the data on TDO is clocked out of the device on the falling edge of TCK. When TCK is idle at low state, all the stored-state devices contained in the test logic will retain their state indefinitely. If JTAG is not used, this pin may be left unconnected.
TDO	O	4	C2	**TDO: JTAG Test Data Output** This output pin is high impedance normally and is used for reading all the serial configuration and test data from the test logic. The data on TDO is clocked out of the device on the falling edge of TCK. If JTAG is not used, this pin should be left unconnected.

Table-1 Pin Description (Continued)

Name	Type	TQFP80 Pin No.	FPBGA81 Pin No.	Description
TDI	I Pullup	5	C3	**TDI: JTAG Test Data Input** This pin is used for loading instructions and data into the test logic and has an internal pull-up resistor. The data on TDI is clocked into the device on the rising edge of TCK. If JTAG is not used, this pin may be left unconnected.
Power Supplies and Grounds				
VDDIO	-	7,40	C1, H9	3.3 V I/O power supply
GNDIO	-	8,39	D1, J8, J9	I/O ground
VDDT1 VDDT2	-	61 80	B8 B3	3.3 V power supply for transmitter driver
GNDT1 GNDT2	-	64 77	B7 A4	Analog ground for transmitter driver
VDDR1 VDDR2	-	68 73	B6 C5	Power supply for receive analog circuit
GNDR1 GNDR2	-	65 76	C7 B4	Analog ground for receive analog circuit
VDDD	-	31	H5	3.3V digital core power supply
GNDD	-	29	H4	Digital core ground
VDDA	-	69	C6	Analog core circuit power supply
GNDA	-	72	B5	Analog core circuit ground
Others				
IC	-	70	A6	**IC: Internal Connection** Internal Use. This pin should be left open in normal operation.
IC	-	6	D2	**IC: Internal Connection** Internal Use. This pin should be connected to ground in normal operation.

3 FUNCTIONAL DESCRIPTION

3.1 CONTROL MODE SELECTION

The IDT82V2082 can be configured by software or by hardware. The software control mode supports Serial Control Interface, Motorola non-Multiplexed Control Interface and Intel non-Multiplexed Control Interface. The Control mode is selected by MODE1 and MODE0 pins as follows:

	Control Interface Mode
00	Hardware interface
01	Serial Microcontroller Interface.
10	Parallel -non-Multiplexed -Motorola Interface
11	Parallel -non-Multiplexed -Intel Interface

- The serial microcontroller Interface consists of $\overline{CS}$, SCLK, SCLKE, SDI, SDO and $\overline{INT}$ pins. SCLKE is used for the selection of active edge of SCLK.
- The parallel non-Multiplexed microcontroller Interface consists of $\overline{CS}$, A[5:0], D[7:0], $\overline{DS}$/$\overline{RD}$, R/$\overline{W}$/$\overline{WR}$ and $\overline{INT}$ pins.
- Hardware interface consists of PULSn[3:0], THZ, RCLKE, LPn[1:0], PATTn[1:0], JA[1:0], MONTn, TERMn, EQn, RPDn, MODE[1:0] and RXTXM[1:0] (n=1, 2). Refer to 5 HARDWARE CONTROL PIN SUMMARY for details about hardware control.

3.2 T1/E1/J1 MODE SELECTION

When the chip is configured by software, T1/E1/J1 mode is selected by the T1E1 bit (**GCF, 20H**). In E1 application, the T1E1 bit (**GCF, 20H**) should be set to '0'. In T1/J1 application, the T1E1 bit should be set to '1'.

When the chip is configured by hardware, T1/E1/J1 mode is selected by PULSn[3:0] pins on a per channel basis. These pins also determine transmit pulse template and internal termination impedance. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

3.3 TRANSMIT PATH

The transmit path of each channel of IDT82V2082 consists of an Encoder, an optional Jitter Attenuator, a Waveform Shaper, a set of LBOs, a Line Driver and a Programmable Transmit Termination.

3.3.1 TRANSMIT PATH SYSTEM INTERFACE

The transmit path system interface consists of TCLKn pin, TDn/TDPn pin and TDNn pin. In E1 mode, TCLKn is a 2.048 MHz clock. In T1/J1 mode, TCLKn is a 1.544 MHz clock. If TCLKn is missing for more than 70 MCLK cycles, an interrupt will be generated if it is not masked.

Transmit data is sampled on the TDn/TDPn and TDNn pins by the active edge of TCLKn. The active edge of TCLKn can be selected by the TCLK_SEL bit (**TCF0, 04H...**). And the active level of the data on TDn/TDPn and TDNn can be selected by the TD_INV bit (**TCF0, 04H...**). In hardware control mode, the falling edge of TCLKn and the active high of transmit data are always used.

The transmit data from the system side can be provided in two different ways: Single Rail and Dual Rail. In Single Rail mode, only TDn pin is used for transmitting data and the T_MD[1] bit (**TCF0, 04H...**) should be set to '0'. In Dual Rail Mode, both TDPn pin and TDNn pin are used for transmitting data, the T_MD[1] bit (**TCF0, 04H...**) should be set to '1'.

3.3.2 ENCODER

In Single Rail mode, when T1/J1 mode is selected, the Encoder can be selected to be a B8ZS encoder or an AMI encoder by setting T_MD[0] bit (**TCF0, 04H...**).

In Single Rail mode, when E1 mode is selected, the Encoder can be configured to be a HDB3 encoder or an AMI encoder by setting T_MD[0] bit (**TCF0, 04H...**).

In both T1/J1 mode and E1 mode, when Dual Rail mode is selected (bit T_MD[1] is '1'), the Encoder is by-passed. In Dual Rail mode, a logic '1' on the TDPn pin and a logic '0' on the TDNn pin results in a negative pulse on the TTIPn/TRINGn; a logic '0' on TDPn pin and a logic '1' on TDNn pin results in a positive pulse on the TTIPn/TRINGn. If both TDPn and TDNn are high or low, the TTIPn/TRINGn outputs a space (Refer to TDn/TDPn, TDNn Pin Description).

In hardware control mode, the operation mode of receive and transmit path can be selected by setting RXTXM1 and RXTXM0 pins on a global basis. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

3.3.3 PULSE SHAPER

The IDT82V2082 provides three ways of manipulating the pulse shape before sending it. The first is to use preset pulse templates for short haul application, the second is to use LBO (Line Build Out) for long haul application and the other way is to use user-programmable arbitrary waveform template.

In software control mode, the pulse shape can be selected by setting the related registers.

In hardware control mode, the pulse shape can be selected by setting PULSn[3:0] pins on a per channel basis. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

3.3.3.1 Preset Pulse Templates

For E1 applications, the pulse shape is shown in Figure-4 according to the G.703 and the measuring diagram is shown in Figure-5. In internal impedance matching mode, if the cable impedance is 75 Ω, the PULS[3:0] bits (**TCF1, 05H...**) should be set to '0000'; if the cable impedance is 120 Ω, the PULS[3:0] bits (**TCF1, 05H...**) should be set to '0001'. In external impedance matching mode, for both E1/75 Ω and E1/120 Ω cable impedance, PULS[3:0] should be set to '0001'.

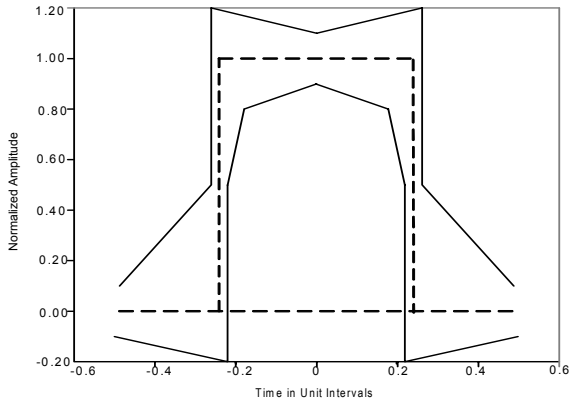

Figure-4 E1 Waveform Template Diagram

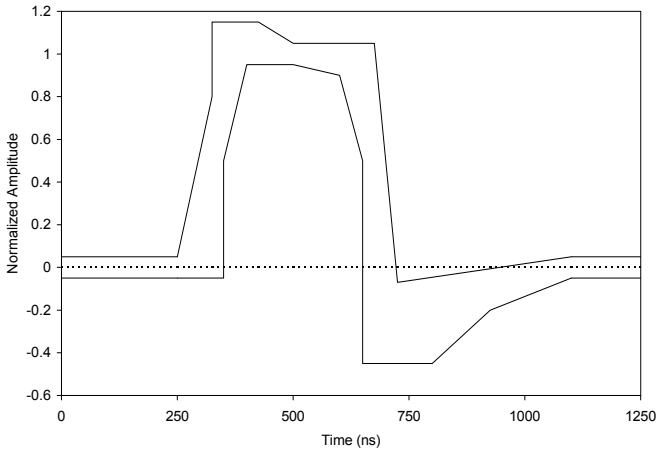

Figure-6 DSX-1 Waveform Template

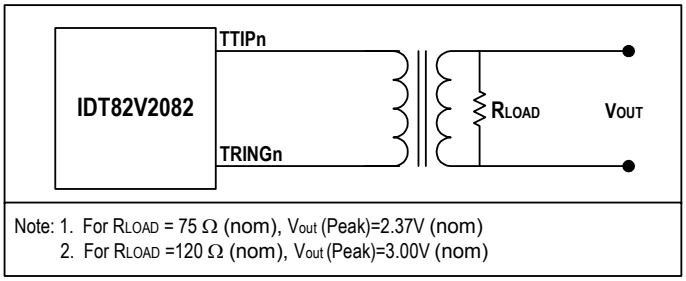

Figure-5 E1 Pulse Template Test Circuit

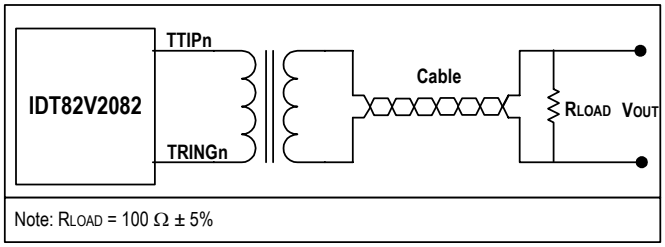

Figure-7 T1 Pulse Template Test Circuit

For T1 applications, the pulse shape is shown in Figure-6 according to the T1.102 and the measuring diagram is shown in Figure-7. This also meets the requirement of G.703, 2001. The cable length is divided into five grades, and there are five pulse templates used for each of the cable length. The pulse template is selected by PULS[3:0] bits (**TCF1, 05H...**).

For J1 applications, the PULS[3:0] (**TCF1, 05H...**) should be set to '0111'. Table-14 lists these values.

3.3.3.2 LBO (Line Build Out)

To prevent the cross-talk at the far end, the output of TTIPn/TRINGn could be attenuated before transmission for long haul applications. The FCC Part 68 Regulations specifies four grades of attenuation with a step of 7.5 dB. Three LBOs are used to implement the pulse attenuation. The PULS[3:0] bits (**TCF1, 05H...**) are used to select the attenuation grade. Both Table-14 and Table-15 list these values.

3.3.3.3 User-Programmable Arbitrary Waveform

When the PULS[3:0] bits are set to '11xx', user-programmable arbitrary waveform generator mode can be used in the corresponding channel. This allows the transmitter performance to be tuned for a wide variety of line condition or special application.

Each pulse shape can extend up to 4 UIs (Unit Interval), addressed by UI[1:0] bits (**TCF3, 07H...**) and each UI is divided into 16 sub-phases, addressed by the SAMP[3:0] bits (**TCF3, 07H...**). The pulse amplitude of each phase is represented by a binary byte, within the range from +63 to -63, stored in WDAT[6:0] bits (**TCF4, 08H...**) in signed magnitude form. The most positive number +63 (D) represents the maximum positive amplitude of the transmit pulse while the most negative number -63 (D) represents the maximum negative amplitude of the transmit pulse. Therefore, up to 64 bytes are used. For each channel, a 64 bytes RAM is available.

There are twelve standard templates which are stored in an on-chip ROM. User can select one of them as reference and make some changes to get the desired waveform.

User can change the wave shape and the amplitude to get the desired pulse shape. In order to do this, firstly, users can choose a set of waveform value from the following twelve tables, which is the most similar to the desired pulse shape. Table-2, Table-3, Table-4, Table-5, Table-6, Table-7, Table-8, Table-9, Table-10, Table-11, Table-12 and Table-13 list the sample data and scaling data of each of the twelve templates. Then modify the corresponding sample data to get the desired transmit pulse shape.

Secondly, through the value of SCAL[5:0] bits increased or decreased by 1, the pulse amplitude can be scaled up or down at the percentage ratio against the standard pulse amplitude if needed. For different pulse shapes, the value of SCAL[5:0] bits and the scaling percentage ratio are different. The following twelve tables list these values.

Do the followings step by step, the desired waveform can be programmed, based on the selected waveform template:

(1).Select the UI by UI[1:0] bits (**TCF3, 07H...**)

(2).Specify the sample address in the selected UI by SAMP [3:0] bits (**TCF3, 07H...**)

(3).Write sample data to WDAT[6:0] bits (**TCF4, 08H...**). It contains the data to be stored in the RAM, addressed by the selected UI and the corresponding sample address.

(4).Set the RW bit (**TCF3, 07H...**) to '0' to implement writing data to RAM, or to '1' to implement read data from RAM

(5).Implement the Read from RAM/Write to RAM by setting the DONE bit (**TCF3, 07H...**)

Repeat the above steps until all the sample data are written to or read from the internal RAM.

(6).Write the scaling data to SCAL[5:0] bits (**TCF2, 06H...**) to scale the amplitude of the waveform based on the selected standard pulse amplitude

When more than one UI is used to compose the pulse template, the overlap of two consecutive pulses could make the pulse amplitude overflow (exceed the maximum limitation) if the pulse amplitude is not set properly. This overflow is captured by DAC_OV_IS bit (**INTS1, 19H...**), and, if enabled by the DAC_OV_IM bit (**INTM1, 14H...**), an interrupt will be generated.

The following tables give all the sample data based on the preset pulse templates and LBOs in detail for reference. For preset pulse templates and LBOs, scaling up/down against the pulse amplitude is not supported.

1. Table-2 Transmit Waveform Value for E1 75 Ω
2. Table-3 Transmit Waveform Value for E1 120 Ω
3. Table-4 Transmit Waveform Value for T1 0~133 ft
4. Table-5 Transmit Waveform Value for T1 133~266 ft
5. Table-6 Transmit Waveform Value for T1 266~399 ft
6. Table-7 Transmit Waveform Value for T1 399~533 ft
7. Table-8 Transmit Waveform Value for T1 533~655 ft
8. Table-9 Transmit Waveform Value for J1 0~655 ft
9. Table-10 Transmit Waveform Value For DS1 0 dB LBO
10. Table-11 Transmit Waveform Value For DS1 -7.5 dB LBO
11. Table-12 Transmit Waveform Value For DS1 -15.0 dB LBO
12. Table-13 Transmit Waveform Value For DS1 -22.5 dB LBO

Table-2 Transmit Waveform Value For E1 75 Ohm

Sample	UI 1	UI 2	UI 3	UI 4
1	0000000	0000000	0000000	0000000
2	0000000	0000000	0000000	0000000
3	0000000	0000000	0000000	0000000
4	0001100	0000000	0000000	0000000
5	0110000	0000000	0000000	0000000
6	0110000	0000000	0000000	0000000
7	0110000	0000000	0000000	0000000
8	0110000	0000000	0000000	0000000
9	0110000	0000000	0000000	0000000
10	0110000	0000000	0000000	0000000
11	0110000	0000000	0000000	0000000
12	0110000	0000000	0000000	0000000
13	0000000	0000000	0000000	0000000
14	0000000	0000000	0000000	0000000
15	0000000	0000000	0000000	0000000
16	0000000	0000000	0000000	0000000

SCAL[5:0] = 100001 (default), One step change of this value of SCAL[5:0] results in 3% scaling up/down against the pulse amplitude.

Table-3 Transmit Waveform Value For E1 120 Ohm

Sample	UI 1	UI 2	UI 3	UI 4
1	0000000	0000000	0000000	0000000
2	0000000	0000000	0000000	0000000
3	0000000	0000000	0000000	0000000
4	0001111	0000000	0000000	0000000
5	0111100	0000000	0000000	0000000
6	0111100	0000000	0000000	0000000
7	0111100	0000000	0000000	0000000
8	0111100	0000000	0000000	0000000
9	0111100	0000000	0000000	0000000
10	0111100	0000000	0000000	0000000
11	0111100	0000000	0000000	0000000
12	0111100	0000000	0000000	0000000
13	0000000	0000000	0000000	0000000
14	0000000	0000000	0000000	0000000
15	0000000	0000000	0000000	0000000
16	0000000	0000000	0000000	0000000

SCAL[5:0] = 100001 (default), One step change of this value of SCAL[5:0] results in 3% scaling up/down against the pulse amplitude.

Table-4 Transmit Waveform Value For T1 0~133 ft

Sample	UI 1	UI 2	UI 3	UI 4
1	0010111	1000010	0000000	0000000
2	0100111	1000001	0000000	0000000
3	0100111	0000000	0000000	0000000
4	0100110	0000000	0000000	0000000
5	0100101	0000000	0000000	0000000
6	0100101	0000000	0000000	0000000
7	0100101	0000000	0000000	0000000
8	0100100	0000000	0000000	0000000
9	0100011	0000000	0000000	0000000
10	1001010	0000000	0000000	0000000
11	1001010	0000000	0000000	0000000
12	1001001	0000000	0000000	0000000
13	1000111	0000000	0000000	0000000
14	1000101	0000000	0000000	0000000
15	1000100	0000000	0000000	0000000
16	1000011	0000000	0000000	0000000

SCAL[5:0] = 110110[1] (default), One step change of this value of SCAL[5:0] results in 2% scaling up/down against the pulse amplitude.

1. In T1 mode, when arbitrary pulse for short haul application is configured, users should write '110110' to SCAL[5:0] bits if no scaling is required.

Table-5 Transmit Waveform Value For T1 133~266 ft

Sample	UI 1	UI 2	UI 3	UI 4
1	0011011	1000011	0000000	0000000
2	0101110	1000010	0000000	0000000
3	0101100	1000001	0000000	0000000
4	0101010	0000000	0000000	0000000
5	0101001	0000000	0000000	0000000
6	0101000	0000000	0000000	0000000
7	0100111	0000000	0000000	0000000
8	0100110	0000000	0000000	0000000
9	0100101	0000000	0000000	0000000
10	1010000	0000000	0000000	0000000
11	1001111	0000000	0000000	0000000
12	1001101	0000000	0000000	0000000
13	1001010	0000000	0000000	0000000
14	1001000	0000000	0000000	0000000
15	1000110	0000000	0000000	0000000
16	1000100	0000000	0000000	0000000
See Table-4				

Table-6 Transmit Waveform Value For T1 266~399 ft

Sample	UI 1	UI 2	UI 3	UI 4
1	0011111	1000011	0000000	0000000
2	0110100	1000010	0000000	0000000
3	0101111	1000001	0000000	0000000
4	0101100	0000000	0000000	0000000
5	0101011	0000000	0000000	0000000
6	0101010	0000000	0000000	0000000
7	0101001	0000000	0000000	0000000
8	0101000	0000000	0000000	0000000
9	0100101	0000000	0000000	0000000
10	1010111	0000000	0000000	0000000
11	1010011	0000000	0000000	0000000
12	1010000	0000000	0000000	0000000
13	1001011	0000000	0000000	0000000
14	1001000	0000000	0000000	0000000
15	1000110	0000000	0000000	0000000
16	1000100	0000000	0000000	0000000
See Table-4				

Table-7 Transmit Waveform Value For T1 399~533 ft

Sample	UI 1	UI 2	UI 3	UI 4
1	0100000	1000011	0000000	0000000
2	0111011	1000010	0000000	0000000
3	0110101	1000001	0000000	0000000
4	0101111	0000000	0000000	0000000
5	0101110	0000000	0000000	0000000
6	0101101	0000000	0000000	0000000
7	0101100	0000000	0000000	0000000
8	0101010	0000000	0000000	0000000
9	0101000	0000000	0000000	0000000
10	1011000	0000000	0000000	0000000
11	1011000	0000000	0000000	0000000
12	1010011	0000000	0000000	0000000
13	1001100	0000000	0000000	0000000
14	1001000	0000000	0000000	0000000
15	1000110	0000000	0000000	0000000
16	1000100	0000000	0000000	0000000
See Table-4				

Table-8 Transmit Waveform Value For T1 533~655 ft

Sample	UI 1	UI 2	UI 3	UI 4
1	0100000	1000011	0000000	0000000
2	0111111	1000010	0000000	0000000
3	0111000	1000001	0000000	0000000
4	0110011	0000000	0000000	0000000
5	0101111	0000000	0000000	0000000
6	0101110	0000000	0000000	0000000
7	0101101	0000000	0000000	0000000
8	0101100	0000000	0000000	0000000
9	0101001	0000000	0000000	0000000
10	1011111	0000000	0000000	0000000
11	1011110	0000000	0000000	0000000
12	1010111	0000000	0000000	0000000
13	1001111	0000000	0000000	0000000
14	1001001	0000000	0000000	0000000
15	1000111	0000000	0000000	0000000
16	1000100	0000000	0000000	0000000
See Table-4				

Table-9 Transmit Waveform Value For J1 0~655 ft

Sample	UI 1	UI 2	UI 3	UI 4
1	0010111	1000010	0000000	0000000
2	0100111	1000001	0000000	0000000
3	0100111	0000000	0000000	0000000
4	0100110	0000000	0000000	0000000
5	0100101	0000000	0000000	0000000
6	0100101	0000000	0000000	0000000
7	0100101	0000000	0000000	0000000
8	0100100	0000000	0000000	0000000
9	0100011	0000000	0000000	0000000
10	1001010	0000000	0000000	0000000
11	1001010	0000000	0000000	0000000
12	1001001	0000000	0000000	0000000
13	1000111	0000000	0000000	0000000
14	1000101	0000000	0000000	0000000
15	1000100	0000000	0000000	0000000
16	1000011	0000000	0000000	0000000

SCAL[5:0] = 110110 (default), One step change of this value of SCAL[5:0] results in 2% scaling up/down against the pulse amplitude.

Table-10 Transmit Waveform Value For DS1 0 dB LBO

Sample	UI 1	UI 2	UI 3	UI 4
1	0010111	1000010	0000000	0000000
2	0100111	1000001	0000000	0000000
3	0100111	0000000	0000000	0000000
4	0100110	0000000	0000000	0000000
5	0100101	0000000	0000000	0000000
6	0100101	0000000	0000000	0000000
7	0100101	0000000	0000000	0000000
8	0100100	0000000	0000000	0000000
9	0100011	0000000	0000000	0000000
10	1001010	0000000	0000000	0000000
11	1001010	0000000	0000000	0000000
12	1001001	0000000	0000000	0000000
13	1000111	0000000	0000000	0000000
14	1000101	0000000	0000000	0000000
15	1000100	0000000	0000000	0000000
16	1000011	0000000	0000000	0000000

SCAL[5:0] = 110110 (default), One step change of this Value results in 2% scaling up/down against the pulse amplitude.

Table-11 Transmit Waveform Value For DS1 -7.5 dB LBO

Sample	UI 1	UI 2	UI 3	UI 4
1	0000000	0010100	0000010	0000000
2	0000010	0010010	0000010	0000000
3	0001001	0010000	0000010	0000000
4	0010011	0001110	0000010	0000000
5	0011101	0001100	0000010	0000000
6	0100101	0001011	0000001	0000000
7	0101011	0001010	0000001	0000000
8	0110001	0001001	0000001	0000000
9	0110110	0001000	0000001	0000000
10	0111010	0000111	0000001	0000000
11	0111001	0000110	0000001	0000000
12	0110000	0000101	0000001	0000000
13	0101000	0000100	0000000	0000000
14	0100000	0000100	0000000	0000000
15	0011010	0000011	0000000	0000000
16	0010111	0000011	0000000	0000000

SCAL[5:0] = 010001 (default), One step change of this value of SCAL[5:0] results in 6.25% scaling up/down against the pulse amplitude.

Table-12 Transmit Waveform Value For DS1 -15.0 dB LBO

Sample	UI 1	UI 2	UI 3	UI 4
1	0000000	0110101	0001111	0000011
2	0000000	0110011	0001101	0000010
3	0000000	0110000	0001100	0000010
4	0000001	0101101	0001011	0000010
5	0000100	0101010	0001010	0000010
6	0001000	0100111	0001001	0000001
7	0001110	0100100	0001000	0000001
8	0010100	0100001	0000111	0000001
9	0011011	0011110	0000110	0000001
10	0100010	0011100	0000110	0000001
11	0101010	0011010	0000101	0000001
12	0110000	0010111	0000101	0000001
13	0110101	0010101	0000100	0000001
14	0110111	0010100	0000100	0000000
15	0111000	0010010	0000011	0000000
16	0110111	0010000	0000011	0000000

SCAL[5:0] = 001000 (default), One step change of the value of SCAL[5:0] results in 12.5% scaling up/down against the pulse amplitude.

Table-13 Transmit Waveform Value For DS1 -22.5 dB LBO

Sample	UI 1	UI 2	UI 3	UI 4
1	0000000	0101100	0011110	0001000
2	0000000	0101110	0011100	0000111
3	0000000	0110000	0011010	0000110
4	0000000	0110001	0011000	0000101
5	0000001	0110010	0010111	0000101
6	0000011	0110010	0010101	0000100
7	0000111	0110010	0010100	0000100
8	0001011	0110001	0010011	0000011
9	0001111	0110000	0010001	0000011
10	0010101	0101110	0010000	0000010
11	0011001	0101100	0001111	0000010
12	0011100	0101001	0001110	0000010
13	0100000	0100111	0001101	0000001
14	0100011	0100100	0001100	0000001
15	0100111	0100010	0001010	0000001
16	0101010	0100000	0001001	0000001
SCAL[5:0] = 000100 (default), One step change of this value of SCAL[5:0] results in 25% scaling up/down against the pulse amplitude.				

3.3.4 TRANSMIT PATH LINE INTERFACE

The transmit line interface consists of TTIPn and TRINGn pins. The impedance matching can be realized by the internal impedance matching circuit or the external impedance matching circuit. If T_TERM[2] is set to '0', the internal impedance matching circuit will be selected. In this case, the T_TERM[1:0] bits (**TERM, 02H...**) can be set to choose 75 Ω, 100 Ω, 110 Ω or 120 Ω internal impedance of TTIPn/TRINGn. If T_TERM[2] is set to '1', the internal impedance matching circuit will be disabled. In this case, the external impedance matching circuit will be used to realize the impedance matching. For T1/J1 mode, the external impedance matching circuit for the transmitter is not supported.

Figure-9 shows the appropriate external components to connect with the cable for one channel. Table-14 is the list of the recommended impedance matching for transmitter.

In hardware control mode, TERMn pin can be used to select impedance matching for both receiver and transmitter on a per channel basis. If TERMn pin is low, internal impedance network will be used. If TERMn pin is high, external impedance network will be used in E1 mode, or external impedance network for receiver and internal impedance network for transmitter will be used in T1/J1 mode. (This applies to ZB die revision only). When internal impedance network is used, PULSn[3:0] pins should be set to select the specific internal impedance in the corresponding channel. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

The TTIPn/TRINGn can also be turned into high impedance globally by pulling THZ pin to high or individually by setting the THZ bit (**TCF1, 05H...**) to '1'. In this state, the internal transmit circuits are still active.

In hardware control mode, TTIPn/TRINGn pins can be turned into high impedance globally by pulling THZ pin to high. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

Besides, in the following cases, TTIPn/TRINGn will also become high impedance:

- Loss of MCLK;
- Loss of TCLKn (exceptions: Remote Loopback; Transmit internal pattern by MCLK);
- Transmit path power down;
- After software reset; pin reset and power on.

Table-14 Impedance Matching for Transmitter

Cable Configuration	Internal Termination			External Termination		
	T_TERM[2:0]	PULS[3:0]	R_T	T_TERM[2:0]	PULS[3:0]	R_T
E1/75 Ω	000	0000	0 Ω	1XX	0001	9.4 Ω
E1/120 Ω	001	0001			0001	
T1/0~133 ft	010	0010		-	-	-
T1/133~266 ft		0011				
T1/266~399 ft		0100				
T1/399~533 ft		0101				
T1/533~655 ft		0110				
J1/0~655 ft	011	0111				
0 dB LBO	010	1000				
-7.5 dB LBO		1001				
-15.0 dB LBO		1010				
-22.5 dB LBO		1011				

Note: The precision of the resistors should be better than ± 1%