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T1 / E1 / J1 Octal Framer
IDT82V2108

Version 5
November 26, 2012

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T1 / E1 / J1 Octal Framer · IDT82V2108

FEATURES

- Octal Framer supporting T1, E1 and J1 formats
- Provides programmable system interface to support Zarlink Semi-conductor Inc. ST-BUS®, AT&T® CHI and MVIP bus, supporting data rates of 1.544, 2.048 & 8.192 Mb/s; up to four links can be byte-interleaved on one system bus without external logic
- Provides up to three internal floating HDLC controllers for each framer to support ISDN PRI and V5.X interface. Each HDLC contains 128-byte deep FIFOs in both receive and transmit directions
- Provides jitter attenuation performance exceeding the requirements set by the associated standards for both Rx and Tx path
- Provides payload, line and digital loopbacks
- Provides a floating Pseudo Random Bit Sequence / repetitive pattern generator/detector, which can be assigned to any one of eight framers, the pattern may be inserted / detected on an unframed or Nx64K or Nx56K (T1 only) basis
- Provides signaling insertion / extraction for CCS / CAS and RBS signaling system
- Provides programmable codes insertion, data / sign inversion and digital milliwatt code insertion on a per channel / timeslot basis
- Supports automatic / manual alarming transmit and integration
- Provides performance monitor to count CRC error, framing bit error, far end block CRC error (E1), out of frame event (T1/J1) and change of frame alignment event (T1/J1)
- Provides programmable Inband Loopback Code transmitter/ receiver, Bit Oriented Message generator/detector
- Supports polled or interrupt driven processing for all events
- Supports multiplexed or non-multiplexed address/data bus MPU interface for configuration, control and status monitoring
- JTAG boundary scan meets IEEE 1149.1
- Low power 3.3 V CMOS technology with 5 V tolerant inputs
- Operating industrial temperature range: -40 °C to +85 °C
- Package available: 128 pin PQFP
  144 pin PBGA
  Green Package Option available

APPLICATIONS

- High density internet E1 or T1 / J1 interface for routers, multiplexers, switches and digital modems
- Frame relay switches and access devices (FRADS)
- SONET / SDH Add / Drop multiplexers
- Digital private branch exchanges (PBX)
- Channel service units (CSU) and data service units (DSU)
- Channel banks and multiplexers
- Digital Access and Cross-Connect systems (DACS)

STANDARDS

E1 MODE:

ITU-T:	G.704, G.706, G.732, G.802, G.737, G.738, G.739, G.742, G.823, G.964, G.965, I.431, O.151, O.152, O.153;
ETSI:	ETS 300 011, ETS 300 233, ETS 324-1, ETS 347-1, TBR 4, TBR 12, TBR 13;

GO - MVIP

T1/J1 MODE:

ANSI:	T1.107, T1.231, T1.403, T1.408;
TR:	TSY-000147, TSY-000191, NWT-000303, TSY-000312, TSY-000-499;
AT&T:	TR 54016, TR 62411
TTC:	JT-G 703, JT-G 704, JT-G706, JT-G 1431

DSC-6039/4

DESCRIPTION

The IDT82V2108 is a flexible feature-rich octal T1/E1/J1 Framer. Controlled by software, the IDT82V2108 can be globally configured as an Octal E1 or T1/J1 Framer. When E1 or T1/J1 has been set globally, the operation mode of each of the eight framers can be configured independently. The configuration is performed through a parallel Multiplexed/Non-Multiplexed microprocessor interface.

The IDT82V2108 realizes frame synchronization, frame generation, signaling extraction and insertion, alarm and test signals generation and detection in a single chip. It also integrates up to three HDLC receivers and HDLC transmitters for each of the eight framers.

In E1 Mode, the receive path of each framer can be configured to be Basic Frame, CRC Multi-Frame and Signaling Multi-Frame. The framing can also be bypassed (unframed mode). It detects and indicates the event of out of Basic Frame Synchronization, out of CRC Multi-Frame and out of Signaling Multi-Frame. It also detects and indicates the Remote Alarm Indication signal and the Remote Signaling Multi-Frame Alarm Indication signal. The Red and AIS alarms are monitored. Basic Frame Alignment Signal errors, Far End Block Errors (FEBE) and CRC errors are counted. Up to three HDLC links are provided to extract the HDLC message on TS16, the Sa National bits and/or any arbitrary time slot. An Elastic Store Buffer that optionally supports slip buffering and adaptation to backplane timing is provided. In E1 receive path, signaling debounce, signaling freezing, idle code substitution, digital milliwatt code insertion, trunk conditioning, data inversion and pattern generation or detection are also supported on a per-timeslot basis.

In E1 mode, the transmit path of each framer can be configured to generate Basic Frame, CRC Multi-Frame and Signaling Multi-Frame. The framing can also be disabled (unframed mode). It can also transmit Remote Alarm Indication signal, Remote Signaling Multi-Frame Alarm Indication signal, AIS signal and FEBE. Up to three HDLC links are provided to insert the HDLC message on TS16, the Sa National bits and/or any arbitrary time slot. The signaling insertion, idle code substitution, data insertion, data inversion and test pattern generation or detection are also supported on a per-timeslot basis.

In E1 mode, any four of the eight framers can be multiplexed or de-multiplexed to or from one of the two 8.192M bit/s buses.

In T1/J1 mode, the receive path of each framer can be configured to be in Super Frame (SF) or Extended Super Frame (ESF) formats. The framing can also be bypassed (unframed mode). It detects and indicates the out of SF/ESF synchronization event, the Yellow, Red and AIS alarms. It also detects the presence of inband loopback codes, bit oriented message. Frame Alignment Signal errors, CRC-6 errors, out of SF/ESF events and Frame Alignment position changes are counted. Up to two HDLC links are provides to extract the HDLC message on the F-bit or any arbitrary channels in ESF format. An Elastic Store Buffer that optionally supports controlled slip and adaptation to backplane timing is provided. In T1/J1 receive path, signaling debounce, signaling freezing, idle code substitution, digital milliwatt code insertion, idle code insertion, data inversion and pattern generation or detection are also supported on a per-channel basis.

In T1/J1 mode, the transmit path of each framer can be configured to generate SF or ESF. The framing can also be disabled (unframed mode). It can also transmit Yellow signal and AIS signal. Inband loopback codes and bit oriented message can also be transmitted. Up to two HDLC links are provided to insert the HDLC message on the F-bit or any arbitrary channels in ESF format. The signaling insertion, idle code substitution, data insertion, data inversion and test pattern generation or detection are also supported on a per-channel basis.

In T1/J1 mode, the data stream of 1.544M bit/s can be converted to/from the data stream of 2.048M bit/s on the system side by software configuration. In addition, any four of the eight framers can be multiplexed or de-multiplexed to or from one of the two 8.192M bit/s buses.

FUNCTIONAL BLOCK DIAGRAM

One of the Eight Framers

TSCCKA
TSCCKB/ MTSCCKB
TSCFS/ MTSCFS
MTSSIG[1:2]
MTSD[1:2]

TSFSn/ TSSIGn
TSDn

Transmit System Interface

Transmit Payload Control

Frame Generator

Transmit Clock

Transmit Jitter Attenuator

LTCKn
LTDn

HDLC Transmitter #1 | #2 | #3 (E1 only)

Inband Loopback Code Generator (T1/J1 only)

Bit-Oriented Message Transmitter (T1/J1 only)

Digital Loopback

XCK

Payload Loopback

PRBS Generator /Detector

Bit-Oriented Message Receiver (T1/J1 only)

Inband Loopback Code Detector (T1/J1 only)

Alarm Detector (T1/J1 only)

HDLC Receiver #1 | #2 | #3 (E1 only)

Line Loopback

MRSD[1:2]
MRSSIG[1:2]
MRSFS[1:2]
RSCCK/ MRSCCK
RSCFS/ MRSCFS

RSDn
RSCKn/ RSSIGn
RSFSn

Receive System Interface

Receive Payload Control

Receive CAS/RBS Buffer

Frame Processor

Elastic Store Buffer

Performance Monitor

Receive Jitter Attenuator

LRCKn
LRDn

Micro-Processor Interface

A[10:0]　$\overline{RD}$　$\overline{WR}$　$\overline{CS}$　ALE　$\overline{INT}$　$\overline{RST}$　D[7:0]

IEEE1149.1 JTAG

$\overline{TRST}$　TMS　TDI　TCLK　TDO

BIAS
VDDIO
VDDC
GNDIO
GNDC

1 PIN ASSIGNMENT

1.1 128 PIN PQFP PACKAGE (TOP VIEW)
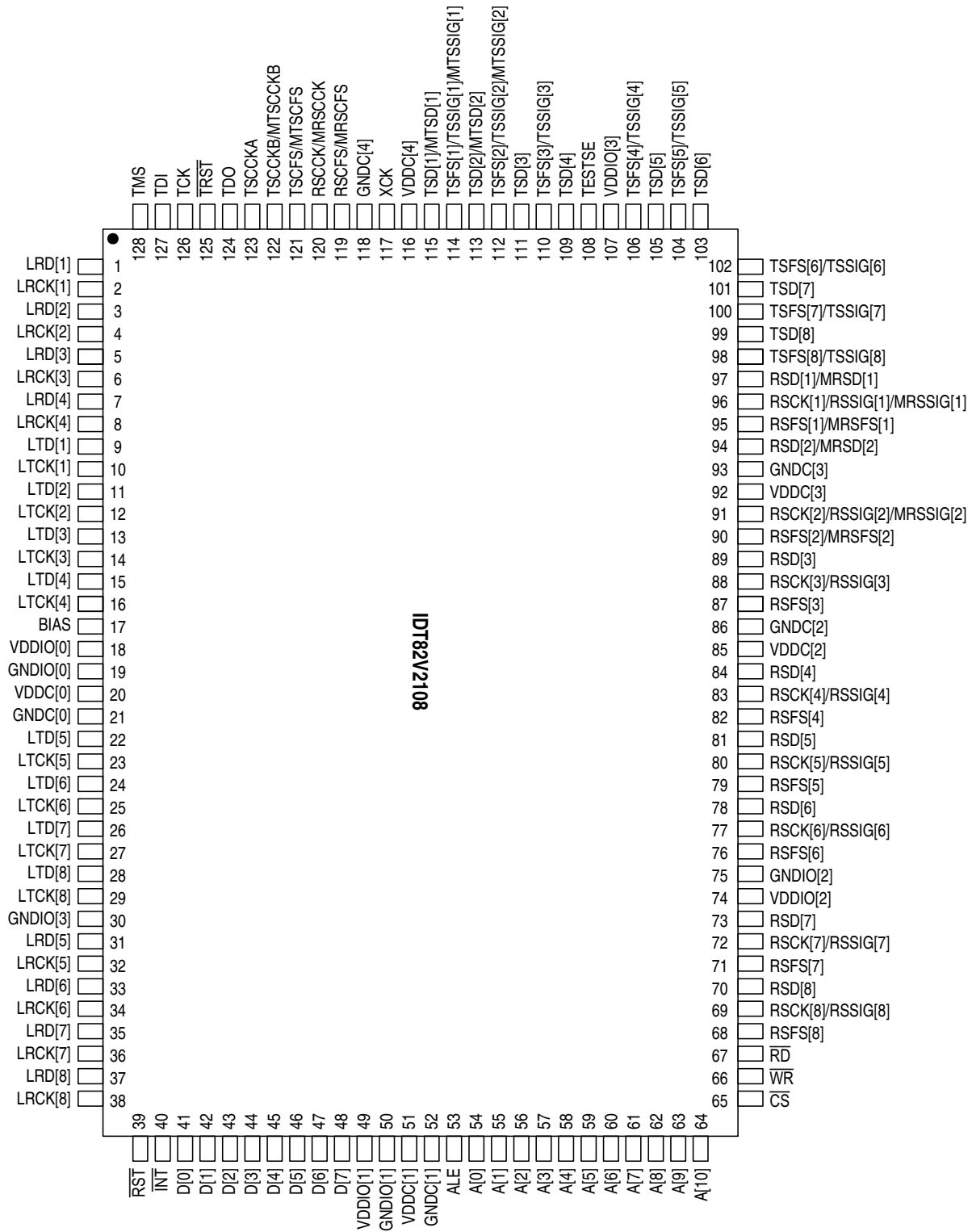
Figure 1. 128-Pin PQFP (Top View)

1.2   144 PIN PBGA PACKAGE (BOTTOM VIEW)

	12	11	10	9	8	7	6	5	4	3	2	1	
A	TSD[7]	TSD[6]	TSFS[4]/ TSSIG[4]	GNDC[4]	TSD[3]	TSFS[1]/ TSSIG[1]/ MTSSIG[1]	VDDC[3]	RSCCK/ MRSCCK	TSCCKA	TCK	LRD[1]	LRD[3]	A
B	RSD[1]/ MRSD[1]	TSD[8]	TSFS[6]/ TSSIG[6]	TSD[5]	TSFS[2]/ TSSIG[2]/ MTSSIG[2]	TSD[1]/ MTSD[1]	XCK	RSCFS/ MRSCFS	TSCCKB/ MTSCCKB	TMS	LRD[2]	LRD[4]	B
C	RSD[2]/ MRSD[2]	RSCK[1]/ RSSIG[1]/ MRSSIG[1]	TSFS[8]/ TSSIG[8]	TSFS[7]/ TSSIG[7]	VDDC[4]	TSFS[3]/ TSSIG[3]	GNDC[3]	TSCFS/ MTSCFS	TDO	LRCK[1]	LRCK[3]	LTCK[1]	C
D	RSCK[2]/ RSSIG[2]/ MRSSIG[2]	RSFS[2]/ MRSFS[2]	VDDIO[3]	RSFS[1]/ MRSFS[1]	TSFS[5]/ TSSIG[5]	TSD[4]	TSD[2]/ MTSD[2]	TRST	TDI	LRCK[2]	LTD[1]	LTCK[2]	D
E	RSCK[3]/ RSSIG[3]	RSFS[3]	RSD[3]	GNDIO[3]	VDDC[5]	VDDC[6]	VDDC[7]	VDDC[8]	LRCK[4]	LTD[2]	LTCK[4]	LTD[4]	E
F	RSD[4]	VDDC[2]	GNDC[2]	RSD[5]	VDDC[9]	VDDC[10]	VDDC[11]	VDDC[12]	LTD[3]	LTCK[3]	GNDIO[0]	VDDIO[0]	F
G	RSFS[4]	RSCK[4]/ RSSIG[4]	RSD[6]	RSCK[6]/ RSSIG[6]	GNDC[5]	GNDC[6]	GNDC[7]	GNDC[8]	BIAS	LTD[5]	GNDC[0]	VDDC[0]	G
H	RSFS[5]	RSCK[5]/ RSSIG[5]	TESTSE	RSCK[7]/ RSSIG[7]	GNDC[9]	GNDC[10]	GNDC[11]	GNDC[12]	LTCK[8]	LTCK[6]	LTCK[5]	LTD[6]	H
J	RSFS[6]	RSD[7]	RSFS[8]	A[9]	A[7]	VDDIO[1]	D[4]	INT	LRD[5]	LTD[8]	LTD[7]	LTCK[7]	J
K	VDDIO[2]	RSD[8]	WR	A[6]	A[3]	A[0]	D[5]	D[2]	LRCK[7]	LRCK[6]	LRCK[5]	GNDIO[1]	K
L	RSFS[7]	RD	A[10]	A[4]	A[1]	ALE	VDDC[1]	D[7]	D[0]	LRCK[8]	LRD[7]	LRD[6]	L
M	RSCK[8]/ RSSIG[8]	CS	A[8]	A[5]	A[2]	GNDC[1]	GNDIO[2]	D[6]	D[3]	D[1]	RST	LRD[8]	M
	12	11	10	9	8	7	6	5	4	3	2	1	

Figure 2. 144-Pin PBGA (Bottom View)

2   PIN DESCRIPTION

Name	Type	Pin No. PQFP	Pin No. PBGA	Description
				Line and System Interface
LRD[1] LRD[2] LRD[3] LRD[4] LRD[5] LRD[6] LRD[7] LRD[8]	Input	1 3 5 7 31 33 35 37	A2 B2 A1 B1 J4 L1 L2 M1	**LRD[1:8]: Line Receive Data for Framer 1 ~ 8** These pins receive the data stream from line interface units or from a higher demultiplex interface. Data on these pins are sampled on the active edge of the corresponding LRCKn.
LRCK[1] LRCK[2] LRCK[3] LRCK[4] LRCK[5] LRCK[6] LRCK[7] LRCK[8]	Input	2 4 6 8 32 34 36 38	C3 D3 C2 E4 K2 K3 K4 L3	**LRCK[1:8]: Line Receive Clock for Framer 1 ~ 8** These pins receive externally recovered line clock (2.048 or 1.544 MHz). The clock is used to sample the data on the corresponding LRDn.
RSCK[1] / RSSIG[1] / MRSSIG[1] RSCK[2] / RSSIG[2] / MRSSIG[2] RSCK[3] / RSSIG[3] RSCK[4] / RSSIG[4] RSCK[5] / RSSIG[5] RSCK[6] / RSSIG[6] RSCK[7] / RSSIG[7] RSCK[8] / RSSIG[8]	Output	96 91 88 83 80 77 72 69	C11 D12 E12 G11 H11 G9 H9 M12	**RSCK[1:8]: Receive Side System Clock for Framer 1 ~ 8** In Receive Clock Master Full E1 or T1/J1 mode, the clock is a smoothed version of the corresponding 2.048 or 1.544 MHz Line Receive Clock (LRCKn). The RSCKn is pulsed for each bit in the 256-bit or 193-bit frame. The corresponding RSFSn and RSDn pins are updated on the active edge of RSCKn. In Receive Clock Master Nx64K mode, the clock is a gapped version of the associated smoothed LRCKn. The pulse number of RSCKn in each frame is controllable from 0 to 255 or from 0 to 192 on a per-timeslot/channel basis. The corresponding RSFSn and RSDn pins are updated on the active edge of RSCKn. In Receive Clock Slave RSCK Reference mode, RSCKn can be selected to be either a 2.048/1.544 MHz jitter attenuated version of the corresponding LRCKn or an 8KHz clock divided down from the smoothed line clock LRCKn. **RSSIG[1:8]: Receive Side System Signaling for Framer 1 ~ 8** In Receive Clock Slave External Signaling mode, the extracted signaling is output on these pins. The signal on these pins is timeslot/channel-aligned with the data output on the corresponding RSDn pin and is updated on the active edge of RSCCK. The extracted signaling is located in the lower nibble (b5 ~ b8). In E1 mode, the extracted signaling repeats during the entire Signaling Multi-Frame for the same time slot. In T1/J1 mode, the extracted signaling repeats during the entire SF/ESF for the same channel. **MRSSIG[1:2]: Multiplexed Receive Side System Signaling** When the multiplexed bus structure is configured, the extracted signaling data from the selected framers are multiplexed on these pins using a byte-interleaved multiplexing scheme. The data on MRSSIG[1:2] are updated on the active edge of MRSCCK.
RSD[1] / MRSD[1] RSD[2] / MRSD[2] RSD[3] RSD[4] RSD[5] RSD[6] RSD[7] RSD[8]	Output	97 94 89 84 81 78 73 70	B12 C12 E10 F12 F9 G10 J11 K11	**RSD[1:8]: Receive Side System Data for Framer 1 ~ 8** The processed data stream is output on these pins. In Receive Clock Master mode, RSDn is updated on the active edge of the corresponding RSCKn. In Receive Clock Slave mode, RSDn is updated on the active edge of RSCCK. **MRSD[1:2]: Multiplexed Receive Side System Data** When the multiplexed bus structure is configured, the processed data stream from the selected framers is multiplexed on these pins using the byte-interleaved multiplexing scheme. The data on MRSD[1:2] are updated on the active edge of MRSCCK.

Name	Type	Pin No. PQFP	Pin No. PBGA	Description
RSFS[1] / MRSFS[1] RSFS[2] / MRSFS[2] RSFS[3] RSFS[4] RSFS[5] RSFS[6] RSFS[7] RSFS[8]	Output	95 90 87 82 79 76 71 68	D9 D11 E11 G12 H12 J12 L12 J10	**RSFS[1:8]: Receive Side System Frame Pulse for Framer 1 ~ 8** In E1 mode, RSFSn can be configured to indicate the beginning of Basic Frame, or CRC Multi-Frame or/and Signaling Multi-Frame for data stream on RSDn. When configured for the Basic Frame, RSFSn will pulse high/low during the first bit of each Basic Frame. When configured for CRC Multi-Frame, RSFSn will pulse during the first bit of the first frame of the CRC Multi-Frame. When configured for the Signaling Multi-Frame, RSFSn will pulse during the first bit of the first frame of the Signaling Multi-Frame. When configured to indicate both Signaling and CRC Multi-Frame, RSFSn will go high/low on the first bit of the first frame of the Signaling Multi-Frame and go the opposite after the first bit of the first frame of the CRC Multi-Frame. In T1/J1 mode, RSFSn can be configured to indicate each F-bit, or the first F-bit of every 12-frame SFs / every 24-frame ESFs. RSFSn pulses during the above F-bit. In both E1 and T1/J1 modes, when Receive Clock Master mode is active, RSFSn is updated on the active edge of the corresponding RSCKn. When Receive Clock Slave mode is active, RSFSn is updated on the active edge of RSCCK. **MRSFS[1:2]: Multiplexed Receive Side System Frame Pulse** When the multiplexed bus structure is configured, the signals on these pins indicate the beginning of a multiplexed frame. MRSFS[1:2] are updated on the active edge of MRSCCK.
RSCCK / MRSCCK	Input	120	A5	**RSCCK: Receive Side System Common Clock** RSCCK is used only in Receive Clock Slave mode. In E1 mode, it is a 2.048 or 4.096 MHz clock. In T1 mode, it is a 1.544 or 2.048 or 4.096 MHz clock. In Receive Clock Slave RSCK Reference mode, RSDn and RSFSn are updated and RSCFS is sampled on the active edge of RSCCK. In Receive Clock Slave External Signaling mode, RSDn, RSFSn and RSSIGn are updated and RSCFS is sampled on the active edge of RSCCK. **MRSCCK: Multiplexed Receive Side System Common Clock** When the multiplexed bus structure is configured, MRSCCK is an 8.192 or 16.384 MHz clock for the receive system multiplexed bus. MRSCFS is sampled and MRSD[1:2], MRSFS[1:2] and MRSSIG[1:2] are updated on the active edge of MRSCCK.
RSCFS / MRSCFS	Input	119	B5	**RSCFS: Receive Side System Common Frame Pulse** In Receive Clock Slave mode, RSCFS can be selected as a frame alignment reference. It is asserted on the request of each Basic Frame or each Multi-Frame in E1 mode, or it is asserted on the request of F-bit in T1/J1 mode. RSCFS is sampled on the active edge of RSCCK. **MRSCFS: Multiplexed Receive Side System Common Frame Pulse** When the multiplexed bus structure is configured, the signal on this pin aligns the multiplexed frame to the backplane timing. MRSCFS is sampled on the active edge of MRSCCK.
TSD[1] / MTSD[1] TSD[2] / MTSD[2] TSD[3] TSD[4] TSD[5] TSD[6] TSD[7] TSD[8]	Input	115 113 111 109 105 103 101 99	B7 D6 A8 D7 B9 A11 A12 B11	**TSD[1:8]: Transmit Side System Data for Framer 1 ~ 8** The data streams from the system backplane are input on these pins. In Transmit Clock Master mode, TSDn is sampled on the active edge of the corresponding LTCKn. In Transmit Clock Slave mode, TSDn is sampled on the active edge of TSCCKB. **MTSD[1:2]: Multiplexed Transmit Side System Data** When the multiplexed bus structure is configured, the data stream from the backplane is carried on the multiplexed bus for the selected framers. MTSD[1:2] are sampled on the active edge of MTSCCKB.

Name	Type	Pin No.		Description
		PQFP	**PBGA**	
TSFS[1] / TSSIG[1] / MTSSIG[1] TSFS[2] / TSSIG[2] / MTSSIG[2] TSFS[3] / TSSIG[3] TSFS[4] / TSSIG[4] TSFS[5] / TSSIG[5] TSFS[6] / TSSIG[6] TSFS[7] / TSSIG[7] TSFS[8] / TSSIG[8]	Output / Input	114 112 110 106 104 102 100 98	A7 B8 C7 A10 D8 B10 C9 C10	**TSFS[1:8]: Transmit Side System Frame Pulse for Framer 1 ~ 8** In Transmit Clock Master mode, TSFSn indicates the beginning of each Basic Frame in E1 mode, or indicates the F-bit of SF/ESF in T1/J1 mode. TSFSn is updated on the active edge of the corresponding LTCKn. In Transmit Clock Slave TSFS Enabled mode, TSFSn indicates the beginning of each Basic Frame in E1 mode, or indicates the F-bit of SF/ESF in T1/J1 mode. TSFSn is updated on the active edge of TSCCKB. **TSSIG[1:8]: Transmit Side System Signaling for Framer 1 ~ 8** In Transmit Clock Slave External Signaling mode, these are the TSSIG inputs. The signaling is located in the lower nibble (b5 ~ b8) and sampled on the active edge of TSCCKB. In E1 mode, the signaling repeats during the entire Signaling Multi-Frame for the same time slot. In T1/J1 mode, the signaling repeats during the entire SF/ESF for the same channel. **MTSSIG[1:2]: Multiplexed Transmit Side System Signaling** When the multiplexed bus structure is configured, the signaling on the bus is organized in a byte-interleaved scheme for the selected framers. MTSSIG[1:2] are sampled on the active edge of MTSCCKB.
TSCCKA	Input	123	A4	**TSCCKA: Transmit Side System Common Clock A** TSCCKA is one of the reference clocks for the transmit jitter attenuator DPLL. TSCCKA can be configured to input the clock as: 1. 16.384MHz clock; 2. Line rate: 2.048MHz (for E1) or 1.544MHz (for T1); 3. Nx8KHz (N is from 1 to 256) so long as TSCCKA is a jitter-free clock. The IDT82V2108 can be configured to ignore TSCCKA and utilize LRCK and TSCCKB instead. TSCCKA is replaced by LRCK if line loopback is enabled.
TSCCKB / MTSCCKB	Input	122	B4	**TSCCKB: Transmit Side System Common Clock B** In E1 mode, TSCCKB is a 2.048 or 4.096 MHz clock. In T1/J1 mode, TSCCKB is a 1.544 or 2.048 or 4.096 MHz clock. In Transmit Clock Slave TSFS mode, TSDn and TSCFS are sampled and TSFSn is updated on the active edge of TSCCKB. In Transmit Clock Slave External Signaling mode, TSDn, TSSIGn and TSCFS are sampled on the active edge of TSCCKB. **MTSCCKB: Multiplexed Transmit Side System Common Clock B** When the multiplexed bus structure is configured, MTSCCKB is an 8.192 or 16.384 MHz reference clock for the transmit system multiplexed bus. MTSCFS, MTSD[1:2] and MTSSIG[1:2] are sampled on the active edge of MTSCCKB.
TSCFS / MTSCFS	Input	121	C5	**TSCFS: Transmit Side System Common Frame Pulse** In Transmit Clock Slave mode, TSCFS is used to frame align all the framers to the system backplane. In E1 mode, the pulse can be configured to indicate the first bit of a Basic Frame, CRC Multi-Frame / Signaling Multi-Frame. In T1/J1 mode, the pulse can be configured to indicate the first bit of SF/ESF. The width of the pulse must be at least 1 TSCCKB cycle wide. TSCFS is sampled on the active edge of TSCCKB. **MTSCFS: Multiplexed Transmit Side System Common Frame Pulse** When the multiplexed bus structure is configured, MTSCFS is used to frame align the multiplexed frames to the system backplane. MTSCFS is sampled on the active edge of MTSCCKB.
LTD[1] LTD[2] LTD[3] LTD[4] LTD[5] LTD[6] LTD[7] LTD[8]	Output	9 11 13 15 22 24 26 28	D2 E3 F4 E1 G3 H1 J2 J3	**LTD[1:8]: Line Transmit Data for Framer 1 ~ 8** These pins output the data stream to line interface units or a higher multiplex interface. The data on LTDn is updated on the active edge of the corresponding LTCKn.

Name	Type	Pin No.		Description
		PQFP	**PBGA**	
LTCK[1] LTCK[2] LTCK[3] LTCK[4] LTCK[5] LTCK[6] LTCK[7] LTCK[8]	Output	10 12 14 16 23 25 27 29	C1 D1 F3 E2 H2 H3 J1 H4	**LTCKn: Line Transmit Clock for Framer 1 ~ 8** It is a nominal E1 (2.048MHz) or T1/J1 (1.544MHz) clock. LTCK can be derived from TSCCKA, TSCCKB, LRCK or XCK. On the active edge of LTCKn, the corresponding LTDn is updated.
XCK	Input	117	B6	**XCK: Crystal Clock** The clock frequency equals 49.152MHz ± 50 ppm 50% duty cycle for E1 and 37.056MHz ± 32 ppm 50% duty cycle for T1/J1.
Microprocessor Interface				
$\overline{RST}$	Input	39	M2	**$\overline{RST}$: Reset (Active Low)** A low signal for at least 100 ns on this pin will reset the device anytime. $\overline{RST}$ is a Schmitt-trigger input with weak pull-up.
$\overline{CS}$	Input	65	M11	**$\overline{CS}$: Chip Select (Active Low)** This pin must be asserted low to enable the microprocessor interface. The signal must be asserted high at least once after power up to clear the internal test modes. A transition from high to low must occur on this pin for each Read/Write operation and can not return to high until the operation is over.
$\overline{INT}$	Output	40	J5	**$\overline{INT}$: Open-Drain Interrupt Signal (Active Low)** This pin will keep low until all the active unmasked interrupt are acknowledged at their sources.
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7] A[8] A[9] A[10]	Input	54 55 56 57 58 59 60 61 62 63 64	K7 L8 M8 K8 L9 M9 K9 J8 M10 J9 L10	**A[10:0]: Address Bus** The signals on these pins select the register for the microprocessor to access.
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	Output / Input	41 42 43 44 45 46 47 48	L4 M3 K5 M4 J6 K6 M5 L5	**D[7:0]: Bi-directional Data Bus** Signals on these pins are the data for Read/Write operation.
$\overline{RD}$	Input	67	L11	**$\overline{RD}$: Read Strobe (Active Low)** A low signal on this pin enables a read operation on the selected register.
$\overline{WR}$	Input	66	K10	**$\overline{WR}$: Write Strobe (Active Low)** A low signal on this pin enables a write operation on the selected register.
ALE	Input	53	L7	**ALE: Address Latch Enable** In non-multiplexed address/data bus, the ALE is connected to High. It is internally pulled-up.
JTAG (per IEEE 1149.1)				

Name	Type	Pin No.		Description
		PQFP	**PBGA**	
$\overline{\text{TRST}}$	Input	125	D5	**$\overline{\text{TRST}}$: Test Reset (Active Low)** A low signal on this pin will reset the JTAG test port anytime. This pin is a Schmitt-triggered input with an internal pull-up resistor. It must be connected to the $\overline{\text{RST}}$ pin or ground when JTAG is not used.
TMS	Input	128	B3	**TMS: Test Mode Select** The signal on this pin controls the JTAG test performance and is clocked into the device on the rising edge of the TCK. This pin has an internal pull-up resistor.
TCK	Input	126	A3	**TCK: Test Clock** The clock for the JTAG test is input on this pin. The TDI and the TMS are clocked into the device on the rising edge of the TCK and the TDO is clocked out of the device on the falling edge of the TCK.
TDI	Input	127	D4	**TDI: Test Input** The test data are input on this pin. It is sampled on the rising edge of the TCK. This pin has an internal pull-up resistor.
TDO	Tri-State	124	C4	**TDO: Test Output** The test data are output on this pin. It is sampled on the falling edge of the TCK. This pin is in tri-state mode, except during the process of scanning of the data.
				Power & Ground
BIAS	Power	17	G4	**BIAS: +5V Bias** This pin enables +5 V tolerance on the inputs. When +5 V tolerance inputs are required, the BIAS must be connected to a well-decoupled +5 V rail. When +3 V input is required, the BIAS must be connected to a well-decoupled +3.3 V DC supply. During power up, the BIAS pin should be powered no later than any VDDC/VDDIO pin is powered.
VDDIO[0] VDDIO[1] VDDIO[2] VDDIO[3]	Power	18 49 74 107	F1 J7 K12 D10	**VDDIO[3:0]:** These pins must be connected to a common, well-decoupled +3.3 V DC supply together with the core power pins VDDC[4:0] externally.
VDDC[0] VDDC[1] VDDC[2] VDDC[3] VDDC[4] VDDC[5:12]	Power	20 51 85 92 116 -	G1 L6 F11 A6 C8 E8 E7 E6 E5 F8 F7 F6 F5	**VDDC[4:0]:** These pins must be connected to a common, well-decoupled +3.3 V DC supply together with the pad ring power pins VDDIO[3:0] externally. The VDDC[5:12] are extra power pins for PBGA.
GNDIO[0] GNDIO[1] GNDIO[2] GNDIO[3]	Ground	19 50 75 30	F2 K1 M6 E9	**GNDIO[3:0]:** These pins must be connected to a common ground together with the core ground pins GNDC[4:0].

Name	Type	Pin No.		Description
		PQFP	**PBGA**	
GNDC[0] GNDC[1] GNDC[2] GNDC[3] GNDC[4] GNDC[5:12]	Ground	21 52 86 93 118 -	G2 M7 F10 C6 A9 G8 G7 G6 G5 H8 H7 H6 H5	**GNDC[4:0]:** These pins must be connected to a common ground together with the pad ring ground pins GNDIO[3:0]. The GNDC[5:12] are extra ground pins for PBGA.
TEST				
TESTSE	Input	108	H10	This pin is connected to ground for normal operation and reserved for testing.

Note:

1. All outputs have 4 mA drive capability except for the D[7:0], the LTCK[1:8] and the RSCK[1:8] pins which have 6 mA drive capability.

2. All input and bi-directional pins present minimum capacitive loading.

3   FUNCTIONAL DESCRIPTION

3.1   T1 / E1 / J1 MODE SELECTION

The IDT82V2108 can be configured as a duplex eight ports E1 framer, or a duplex eight ports T1 framer, or a duplex eight ports J1 framer. When the TMODE (b0, 400H)[1] is set to '0', the device is in E1 mode. When the TMODE (b0, 400H) is set to '1', the device is in T1/J1 mode (default mode). In T1/J1 mode, when the JYEL (b3, T1/J1-020H) and the J1_YEL (b5, T1/J1-02CH) are both set to '0', the receive path of the corresponding framer is in T1 mode; when the JYEL (b3, T1/J1-020H) and the J1_YEL (b5, T1/J1-02CH) are both set to '1', the receive path of the corresponding framer is in J1 mode; when the J1_CRC (b6, T1/J1-044H) and the J1_YEL (b5, T1/J1-044H) are both set to '0', the transmit path of the corresponding framer is in T1 mode; when the J1_CRC (b6, T1/J1-044H) and the J1_YEL (b5, T1/J1-044H) are both set to '1', the transmit path of the corresponding framer is in J1 mode.

3.2   FRAME PROCESSOR (FRMP)

The Frame Processor of each framer operates independently.

3.2.1   E1 MODE

In E1 mode, the Frame Processor searches for Basic Frame synchronization, CRC Multi-Frame synchronization, and Channel Associated Signaling (CAS) Multi-Frame synchronization in the received data stream. Figure 3 shows the searching process.

Once the frame is synchronized, the Frame Processor keeps on monitoring the received data stream. The Frame Processor will indicate framing bit errors, CAS Multi-Frame alignment pattern errors, CRC Multi-Frame alignment pattern errors or CRC errors, if any. The status of loss of frame, loss of Signaling Multi-Frame and loss of CRC Multi-Frame can also be detected and declared based on user-selectable criteria. The reframe operation can be initiated by excessive CRC errors, or the CRC Multi-Frame alignment is not found within 400ms. A software reset will also make the Frame Processor reframe.

The Frame Processor can extract the data stream in TS16, and output the extracted data on a separate pin. The Frame Processor also extracts the contents of the International bits (from both the FAS and the NFAS frames), the National bits and the Extra bits (from TS16 in the frame 0 of the Signaling Multi-Frame), and stores these data in registers. The CRC Sub Multi-Frame alignment 4-bit codeword in the National bit positions Sa4 to Sa8 can also be extracted and stored in registers, and updated every CRC Sub Multi-Frame.

The Framer Processor identifies the Remote Alarm bit (bit 3 of TS0 of NFAS frames) and Remote Signaling Multi-Frame Alarm (bit 6 of TS16 of frame 0 of Signaling Multi-Frame). The "de-bounced" Remote Alarm and Remote Signaling Multi-Frame Alarm can be indicated if the corresponding bit has been a certain logic for consecutive 2 or 3 times. The AIS (Alarm Indication Signal) can also be detected, and if the AIS condition has persisted for at least 100 ms, an AIS Alarm is declared. The Frame Processor can also declare a Red Alarm if the out-of-frame condition has persisted for at least 100 ms.

An interrupt output is provided to indicate status changes and the occurrence of some events. The interrupts may be generated every Basic Frame, CRC Sub Multi-Frame, CRC Multi-Frame or Signaling Multi-Frame.

The Frame Processor can also be bypassed to receive unframed data.

Note:

1. The contents in the brackets indicate the position of this bit and the address of the register. If more than one register contains the same bit, the address is only for the first register, the addresses of the remaining registers are listed together with the first register in the Register Description paragraph.
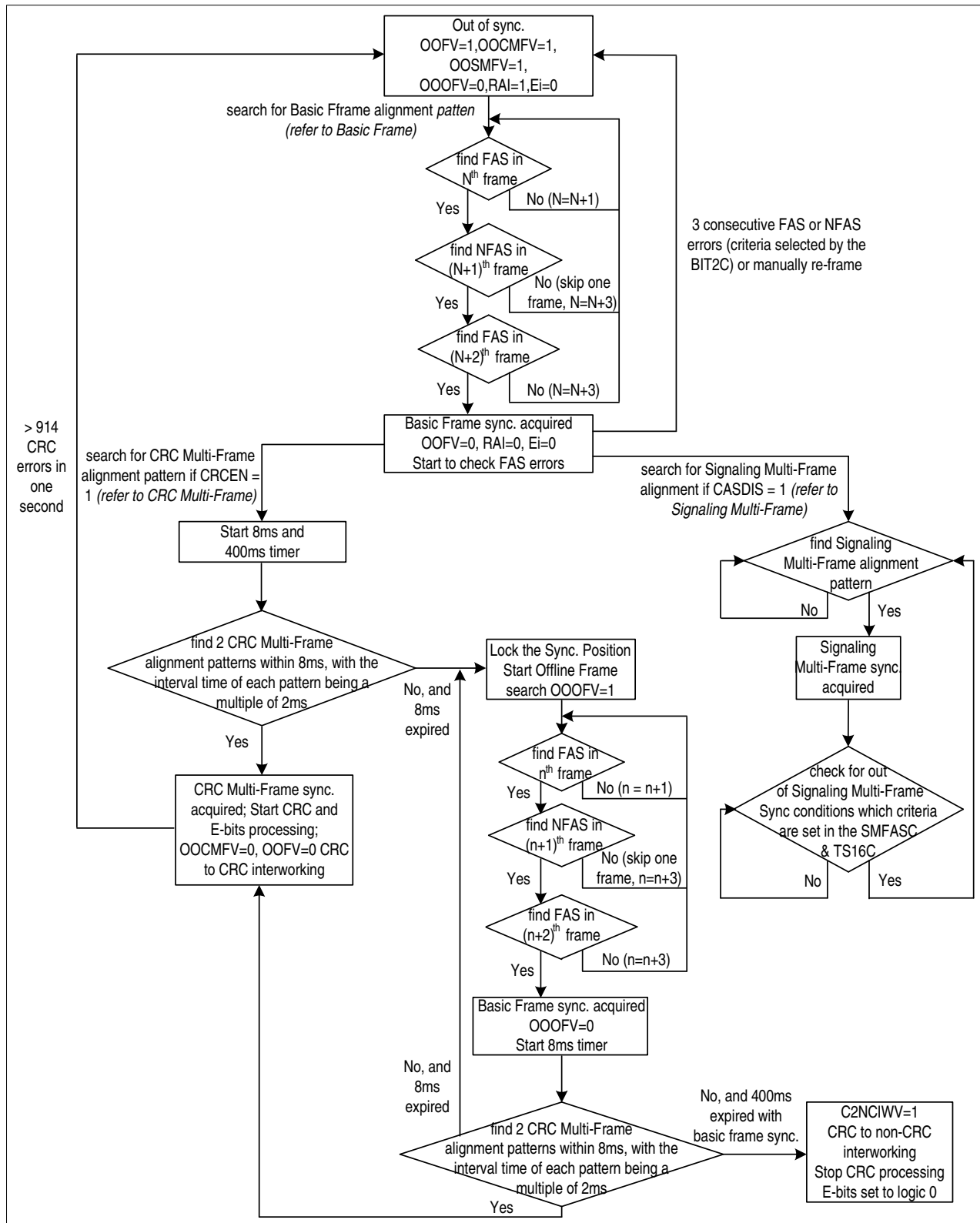
Figure 3. E1 Frame Searching Process

3.2.1.1   Synchronization Searching

All the frame synchronization functions can only be executed when the UNF (b6, E1-000H) is '0'.

3.2.1.1.1   Basic Frame

The algorithm of searching for the E1 Basic Frame alignment pattern (as shown in Figure 4) meets the ITU-T Recommendation G.706 4.1.2 and 4.2.
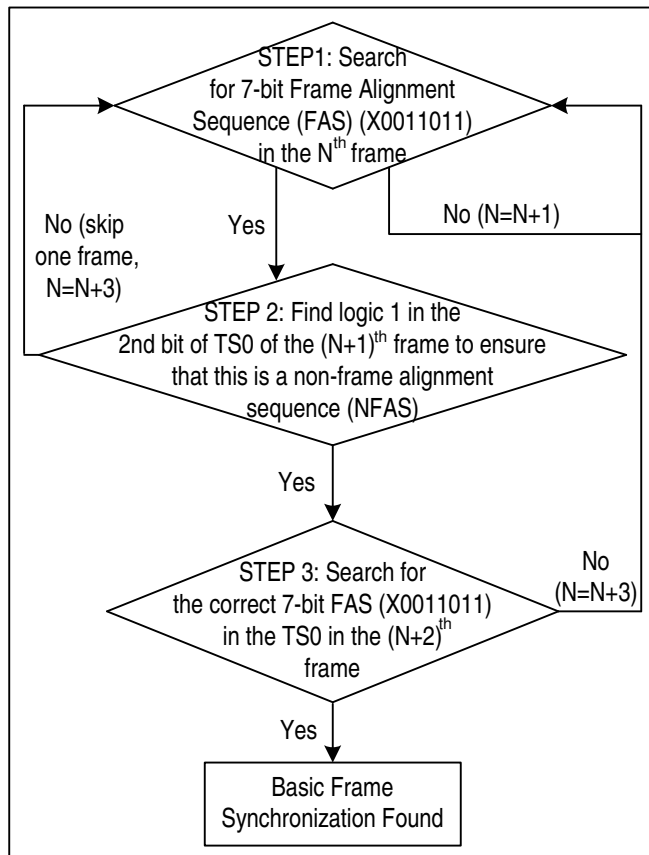

Figure 4. Basic Frame Searching Process

Generally, it is performed by detecting a successive FAS/NFAS/FAS sequence. If STEP 2 is not met, a new search will start after the following frame is skipped. If STEP 3 is not met, a new search will start immediately in the next frame. Once the Basic Frame alignment pattern is detected in the received PCM data stream, the Basic Frame synchronization is acquired and the OOFV (b6, E1-036H) will be set to '0' for indication. Then, this block goes on monitoring the received data stream. If the received Basic Frame alignment signal does not meet its pattern, the FERI (b2, E1-034H) will be set to '1'. The criteria of out of Basic Frame synchronization are determined by the BIT2C (b6, E1-031H). If one of the conditions set in the BIT2C (b6, E1-031H) is met, the search process will restart when the REFRDIS (b0, E1-030H) is '0'. Excessive CRC errors will also lead to re-searching for Basic Frame (refer to Chapter 3.2.1.1.2 CRC Multi-Frame for details).

However, the Basic Frame synchronization can also be forced to re-search for a new Basic Frame any time when there is a transition from '0' to '1' on the REFR (b2, E1-030H).

3.2.1.1.2   CRC Multi-Frame

The CRC Multi-Frame is provided to enhance the ability of verifying data stream. The structure of TS0 of CRC Multi-Frame is illustrated in Table 1:

A CRC Multi-Frame consists of 16 continuous Basic Frames (No. 0 ~ 15), which are numbered from a Basic Frame with FAS. Each CRC Multi-Frame can be divided into two Sub Multi-Frames (SMF I & SMF II).

The first bit of TS0 of each frame is called International (Si) bit. The Si bit in each even frame is the CRC bit. Thus, there are C1, C2, C3, C4 in each SMF. The C1 is the most significant bit, while the C4 is the least significant bit. The Si bits in the first six odd frames are the CRC Multi-Frame alignment pattern. The pattern is '001011'. The Si bits in Frame 13 and Frame 15 are E1 and E2 bits respectively. The E bits' value indicates the Far End Block Errors (FEBE).

After the Basic Frame has been synchronized, the Frame Processor initiates an 8 and 400ms timer to check the CRC Multi-Frame alignment signal if the CRCEN (b7, E1-030H) is '1'. The CRC Multi-Frame synchronization is declared with a '0' in the OOCMFV (b4, E1-036H) only if at least two CRC Multi-Frame alignment patterns are found within 8ms, with the interval time of each pattern being a multiple of 2ms. Then if the received CRC Multi-Frame alignment signal does not meet its pattern, the CMFERI (b0, E1-034H) will be set to '1'. The Frame Processor calculates the data in the SMF(N) per the algorithm in G.704 and G.706 to get a four-bit remainder, then compares the four-bit remainder with the C1, C2, C3, C4 in the next SMF. If there is a difference between them, bit errors exist in SMF(N) and a CRC error is counted. The CRCERR[9:0] (b7~0, E1-039H & b1~0, E1-03AH) are used to indicate the CRC error numbers and are updated every second. Once the CRCERR[9:0] (b7~0, E1-039H & b1~0, E1-03AH) are updated, a '1' will be set in the NEWDATA (b6, E1-03AH) for indication. If the CRCERR[9:0] are over-written, the OVR (b7, E1-03AH) will be asserted. When more than 914 CRC errors occur in one second which is indicated in the EXCRCERR (b0, E1-031H), a new search for the Basic Frame alignment pattern will start if the REFCRCE (b1, E1-030H) is set to '1' and the REFRDIS (b0, E1-030H) is set to '0'.

If the 2 CRC Multi-Frame alignment patterns can not be found within 8ms with the interval time being a multiple of 2ms, an offline search for the Basic Frame alignment pattern will start which is indicated in the OOOFV (b3, E1-036H). The process is the same as shown in Figure 4. This offline operation searches in parallel with the pre-found Basic Frame synchronization searching process. After the new Basic Frame synchronization is acquired by this offline search, the 8ms timer is restarted to check whether the two CRC Multi-Frame alignment patterns are found within 8ms, with the interval time of each pattern being a multiple of 2ms again. If the condition can not be met, the procedure will go on until the 400ms timer ends. If the condition still can not be met at that time and the Basic Frame is still synchronized, the device declares by the C2NCIWV (b7, E1-036) to run under the CRC to non-CRC interworking process. In this process, the CRC Multi-Frame alignment pattern can still be searched if the C2NCIWCK (b5, E1-030H) is set to '1'.

Table 1: Structure of TS0 of CRC Multi-Frame

	SMF	Basic Frame No. / Type	the Eight Bits in Time Slot 0							
			1 (Si bit)	2	3	4	5	6	7	8
CRC-4 Multi-Frame	SMF I	0 / FAS	C1	0	0	1	1	0	1	1
		1 / NFAS	0	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
		2 / FAS	C2	0	0	1	1	0	1	1
		3 / NFAS	0	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
		4 / FAS	C3	0	0	1	1	0	1	1
		5 / NFAS	1	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
		6 / FAS	C4	0	0	1	1	0	1	1
		7 / NFAS	0	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
	SMF II	8 / FAS	C1	0	0	1	1	0	1	1
		9 / NFAS	1	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
		10 / FAS	C2	0	0	1	1	0	1	1
		11 / NFAS	1	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
		12 / FAS	C3	0	0	1	1	0	1	1
		13 / NFAS	E1	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
		14 / FAS	C4	0	0	1	1	0	1	1
		15 / NFAS	E2	1	A	Sa4	Sa5	Sa6	Sa7	Sa8

3.2.1.1.3   CAS Signaling Multi-Frame

If the CRCEN (E1-030H) is '1', after the CRC Multi-Frame has been found, the Frame Processor starts to search for Signaling Multi-Frame alignment pattern when the CASDIS (E1-030H) is '0'. If the CRCEN is '0', after the Basic Frame has been found, the Frame Processor starts to search for Signaling Multi-Frame alignment signal when the CASDIS (E1-030H) is '0'. Refer to Figure 3.

The Signaling Multi-Frame alignment pattern is located in the 1 – 4 bits of TS16 of Frame 0 of Signaling Multi-Frame. The pattern is '0000'. Once the pattern is detected, the Signaling Multi-Frame synchronization is acquired which is indicated with a logic '0' in the OOSMFV (b5, E1-036H). If the received Signaling Multi-Frame alignment signal does not meet its pattern, the SMFERI (b1, E1-034H) will be set to '1'. The entire content in TS16 of Frame 0 of Signaling Multi-Frame is '0000XYXX'. The 'Y' is for remote Signaling Multi-Frame alarm indication and the 'X's are extra bits.

A new search of Signaling Multi-Frame alignment pattern is initiated when the out of the Signaling Multi-Frame criteria set in the SMFASC (b5, E1-031H) and the TS16C (b4, E1-031H) are met or when it is out of Basic Frame synchronization.

3.2.1.2   Alarms & Bit Extraction

3.2.1.2.1   RED Alarm

RED alarm is declared when the out of Basic Frame synchronization condition has persisted for 100 ms. RED alarm is removed when the out of Basic Frame synchronization condition has been absent for 100 ms. The RED alarm status is reflected in the RED (b3, E1-037H).

The received data stream is out of Basic Frame synchronization when any of the following conditions is met:

1) The Basic Frame has not been synchronized.

2) The received data stream meets the out of Basic Frame synchronization criteria set in the BIT2C (b6, E1-031H).

3) There are excessive CRC errors in the received data stream.

Any one of the three conditions will be indicated by the OOFV (b6, E1-036H).

The integration of RED alarm uses the following algorithm: The algorithm monitors the occurrence of out of Basic Frame over a 4 ms interval. A valid out of Basic Frame presence is accumulated when one or more out of Basic Frame indications occurred during the 4 ms interval. Each valid out of Basic Frame presence increases one accumulation. An invalid out of Basic Frame presence is also accumulated when there is no out of Basic Frame indication occurring during the 4 ms inverval. Each invalid out of Basic Frame indication decreases one accumulation (until the accumulation is zero). The RED alarm is declared when 25 valid out of Basic Frame presences have been accumulated. The RED alarm is removed when the out of Basic Frame presences reaches 0.

3.2.1.2.2   AIS Alarm

The AIS density criteria are determined by the AISC (b1, E1-031H). That is, if it is out of Basic Frame synchronization and less than 3 zeros are detected in a 512-bit stream, or if it is out of Basic Frame synchronization and less than 3 zeros are detected in each of 2 consecutive 512-bit streams, the status will be reported by the AISD (b5, E1-037H).