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INVERSE MULTIPLEXING FOR ATM
IDT82V2604

Version - 4
December 4, 2006

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FEATURES

- **Highlights**
  - *Provides API command set for convenient configuration and operation. An embedded controller and a downloaded software are used to interpret the commands. Functions can be added by software upgrading.*
  - *Supports IMA group auto detect.*
  - *Supports link backup so that a backup link can be automatically added when a previously configured link fails.*
  - *All the state machines are implemented in hardware.*
  - *Advanced cell buffer management algorithm to support ATM QoS requirements.*
- **Other Features**
  - *Accommodates up to 4 IMA logical groups.*
  - *Supports 4 T1/E1 channelized or unchannelized links.*
  - *Supports T1 ISDN links.*
  - *Supports MIXED mode: links not assigned to an IMA group can be used in UNI mode.*
  - *Supports symmetrical and asymmetrical operation.*
  - *Supports Common Transmit Clock (CTC) and Independent Transmit Clock (ITC) timing modes.*
  - *Provides 4 Utopia Level 2 8 bit cell level handshake MPHY interface to ATM device.*
  - *Supports maximum link delay tolerance of up to 212 ms for E1 or 281 ms for T1 (when 512 KB external memory is used).*
  - *Provides parameters for MIB (Management Information Base).*
  - *Supports dynamic addition/deletion of links to/from a working IMA group.*
  - *Supports non-multiplexed Intel or Motorola microprocessor interface.*
  - *Loopback capability at both TDM and Utopia ports.*
  - *Supports MVIP.*
  - *JTAG boundary scan meets IEEE 1149.1.*
  - *Package: 208 pin PBGA.*
  - *3.3V operation / 5V tolerant input.*

APPLICATIONS

- *DSLAM concentrator*
- *3G Wireless base station controller (NodeB) and Radio Network Controller (RNC)*
- *Integrated Access Devices (IAD)*

STANDARDS COMPLIANT

- **ATM-Forum**
  - *Utopia Level 2 Version 1.0, af-phy-0039.000, June 1995.*
  - *Inverse Multiplexing for ATM Specification version 1.1, af-phy-0086.001, March 1999.*
  - *Backward compatible with Inverse Multiplexing for ATM Specification version 1.0, af-phy-0086.000, September 1994.*
  - *DS1 Physical Layer Specification, af-phy-0016.000, September 1994.*
  - *E1 Physical Interface Specification, af-phy-0064.000, September 1996.*
- **ITU-T**
  - *I.432 B-ISDN User Network Interface PHY specification.*
  - *G.804 ATM Cell Mapping into Plesiochronous Digital Hierarchy (PDH).*
  - *G.802 Inter-working between networks based on different digital hierarchies and speech encoding laws.*
  - *I.610 B-ISDN operation and maintenance principles and functions.*
- **ANSI**
  - *ANSI T1.646-1995, Broadband-ISDN-Physical Layer Specification for User-Network Interface Including DS1/ATM, 1995.*
- **MVIP**

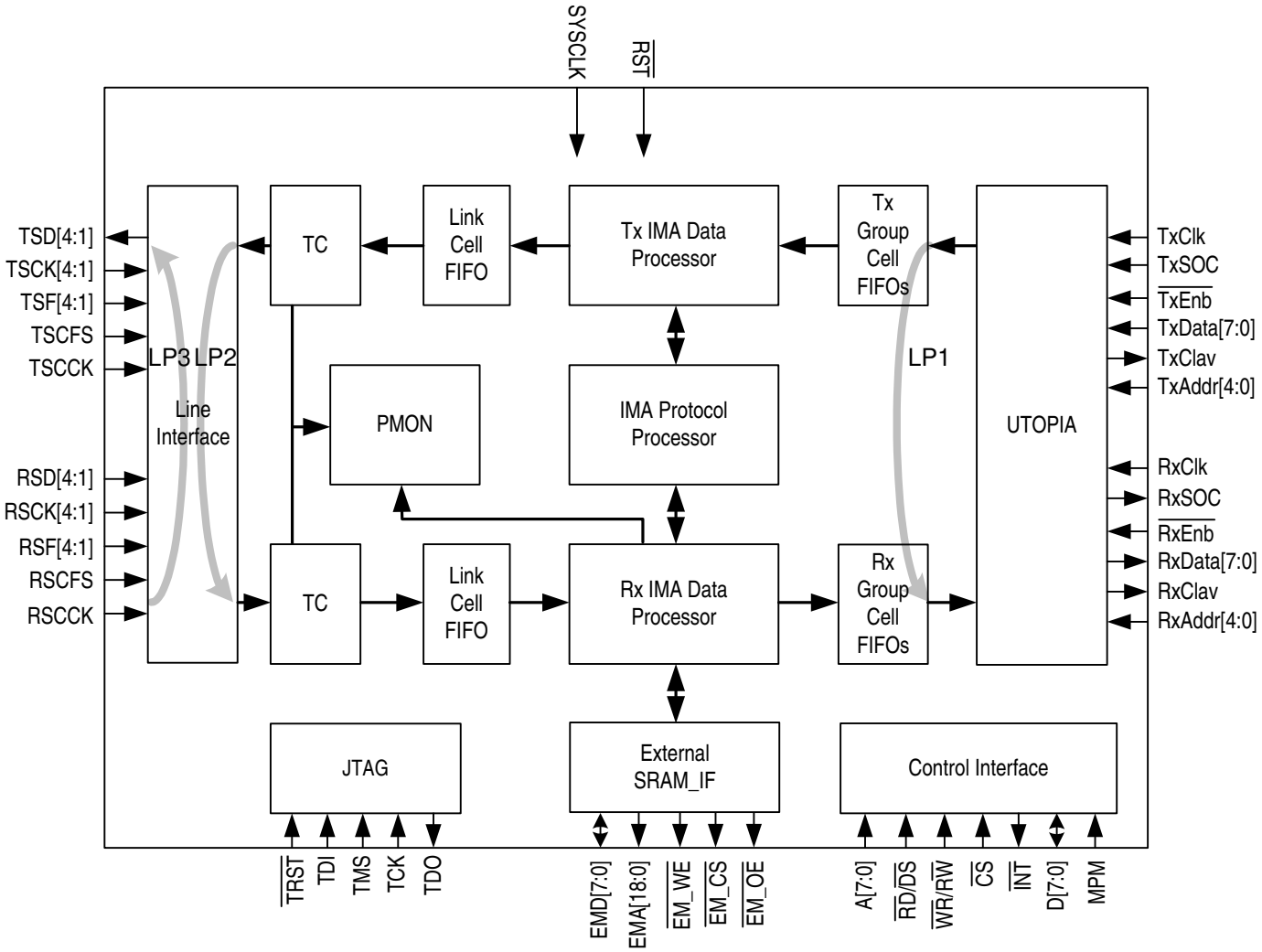
DESCRIPTION

The 4-port IDT82V2604 is a feature-rich device that provides the solution to implement IMA and UNI logical channels over T1 or E1 links in all public or private UNI, NNI and B-ICI applications. The chip is compliant with the ATM Forum IMA specification v1.1 and backward compatible with IMA specification v1.0.

In the chip architecture, up to 4 physically independent T1/E1 streams can be terminated through the utilization of most T1/E1 framers and LIUs in the market, and up to 4 logical IMA groups (i.e., 4 data channels) can be supported at the same time. To interface with most popular ATM layer chips in the market, IDT82V2604 supports Utopia Level 2 MPHY cell level handshake 8-bit bus interface.

Through a well-defined API command set, IMA function can be easily designed into various IMA systems and there is little necessity to access a large amount of registers. A downloaded software is used to interpret the command set and can be easily upgraded to meet specific requirement.

FUNCTIONAL BLOCK DIAGRAM



LP1: Utopia loopback
LP2: Line interface internal loopback
LP3: Line interface external loopback

Figure-1 Functional Diagram

1 PIN ASSIGNMENT

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	GND	IC	IC	EMD4	EMD0	EMA18	EMA15	EMA12	EMA11	EMA8	EMA5	EMA1	RxData2	RxData5	RxData7	GND	A
B	TMS	TDI	IC	EMD5	EMD1	$\overline{EM\_OE}$	EMA16	EMA13	EMA10	EMA7	EMA4	EMA0	RxData3	RxData6	RxSOC	RxClav	B
C	$\overline{TRST}$	TCK	IC	EMD6	EMD2	$\overline{EM\_CS}$	EMA17	EMA14	EMA9	EMA6	EMA3	RxData0	RxData4	RxAddr4	RxAddr3	RxAddr2	C
D	NC	TDO	IC	EMD7	EMD3	$\overline{EM\_WE}$	VDD	GND	GND	VDD	EMA2	RxData1	RxAddr1	RxAddr0	$\overline{RxENB}$	RxCLK	D
E	RSCK1	RSD1	VDD	SYSCLK									TxClav	TxCLK	TxAddr0	TxAddr1	E
F	RSCK2	RSD2	RSF1	VDD									TxAddr2	TxAddr3	TxAddr4	TxSOC	F
G	RSCK3	RSD3	RSF2	VDD			GND	GND	GND	GND			VDD	$\overline{TxENB}$	TxData7	TxData6	G
H	RSCK4	RSD4	RSF3	GND			GND	GND	GND	GND			GND	TxData5	TxData4	TxData3	H
J	RSF4	IC	IC	GND			GND	GND	GND	GND			GND	TxData0	TxData1	TxData2	J
K	IC	IC	IC	VDD			GND	GND	GND	GND			VDD	IC	IC	IC	K
L	IC	IC	IC	VDD									$\overline{CS}$	IC	IC	IC	L
M	IC	IC	IC	VDD									A6	A7	$\overline{RD}/\overline{DS}$	$\overline{WR}/\overline{RW}$	M
N	IC	RSCFS	RSCCK	VDD	VDD	VDD	VDD	GND	GND	VDD	VDD	A1	A2	A3	A4	A5	N
P	TSCCK	TSCFS	VDD	IC	IC	IC	IC	TSF4	TSCK2	TSCK1	IC	VDD	D6	D7	MPM	A0	P
R	VDD	NC	IC	IC	IC	IC	TSD4	TSD3	TSD2	TSD1	$\overline{RST}$	$\overline{INT}$	D2	D3	D4	D5	R
T	GND	VDD	IC	IC	IC	IC	TSCK4	TSCK3	TSF3	TSF2	TSF1	IC	NC	D0	D1	GND	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure-2 IDT82V2604 PBGA208 Package Pin Assignment (Top View)

2 PIN DESCRIPTION

Table-1 Pin Description

Name	Pin Number	Input/Output	Description
			Global Signals
SYSCLK	E4	I	**SYSCLK: System Clock** System clock for the IDT82V2604. Default is 20 MHz.
$\overline{\text{RST}}$	R11	I	**$\overline{\text{RST}}$: System Reset** System reset signal, low active. After reset, all registers are reset to default values, and both the contents in SRAM and the downloaded software are cleared.
			ATM Utopia Interface
TxClk	E14	I	**TxClk: Utopia Transmit Clock** Utopia transmit clock used to transfer data from the ATM layer to the IDT82V2604. The frequency of the TxClk should be less than or equal to that of the system clock. Data is sampled on the rising edge of this signal.
$\overline{\text{TxEnb}}$	G14	I	**$\overline{\text{TxEnb}}$: Utopia Transmit Enable** Utopia low active signal asserted by the ATM layer device during cycles when TxData contains valid cell data. The $\overline{\text{TxEnb}}$ input is sampled on the rising edge of TxClk.
TxAddr4 TxAddr3 TxAddr2 TxAddr1 TxAddr0	F15 F14 F13 E16 E15	I	**TxAddr[4:0]: Utopia Transmit Address** Utopia transmit port address driven from the ATM layer to poll and select an appropriate port. The TxAddr[4:0] input bus are sampled on the rising edge of TxClk.
TxData7 TxData6 TxData5 TxData4 TxData3 TxData2 TxData1 TxData0	G15 G16 H14 H15 H16 J16 J15 J14	I	**TxData[7:0]: Utopia Transmit Data** Utopia 8-bit data bus driven from the ATM layer to the IDT82V2604. The TxData[7:0] input bus are sampled on the rising edge of TxClk.
TxClav	E13	High-Z O	**TxClav: Utopia Transmit Cell Available** Utopia transmit cell available signal from the IDT82V2604 to the ATM layer. A polled port drives TxClav only during each cycle following one with its address on the TxAddr lines. The polled port asserts TxClav high to indicate its corresponding FIFO can accept the transfer of a complete cell, otherwise it deasserts the signal. The TxClav output is updated on the rising edge of TxClk. **Note:** This pin requires a pull-down resistor.
TxSOC	F16	I	**TxSOC: Utopia Transmit Start of Cell** Utopia start of cell signal. It will be driven high by the ATM layer when TxData[7:0] contain the first valid byte of a cell. The TxSOC input is sampled on the rising edge of TxClk.
RxClk	D16	I	**RxClk: Utopia Receive Clock** Utopia receive clock. The frequency of RxClk should be less than or equal to the frequency of the system clock. Data is sampled on the rising edge of this signal.
$\overline{\text{RxEnb}}$	D15	I	**$\overline{\text{RxEnb}}$: Utopia Receive Enable** When this pin is low, the received data will be transferred on RxData[7:0] in the following cycles. The $\overline{\text{RxEnb}}$ input is sampled on the rising edge of RxClk.

Table-1 Pin Description (Continued)

Name	Pin Number	Input/Output	Description
RxAddr4 RxAddr3 RxAddr2 RxAddr1 RxAddr0	C14 C15 C16 D13 D14	I	**RxAddr[4:0]: Utopia Receive Address** Utopia receive port address driven from the ATM layer to poll and select an appropriate port. The RxAddr[4:0] input bus are sampled on the rising edge of RxClk.
RxData7 RxData6 RxData5 RxData4 RxData3 RxData2 RxData1 RxData0	A15 B14 A14 C13 B13 A13 D12 C12	High-Z O	**RxData[7:0]: Utopia Receive Data** Utopia 8-bit data bus driven from the IDT82V2604 to the ATM layer. The RxData[7:0] output bus are updated on the rising edge of RxClk.
RxClav	B16	High-Z O	**RxClav: Utopia Receive Cell Available** Utopia cell available signal. A polled port drives RxClav only during each cycle following one with its address on the RxAddr lines. The polled port asserts RxClav high to indicate its corresponding FIFO has a complete cell available for transfer to the ATM layer, otherwise it deasserts the signal. The RxClav output is updated on the rising edge of RxClk. **Note:** This pin requires a pull-down resistor.
RxSOC	B15	High-Z O	**RxSOC: Utopia Receive Start of Cell** Utopia start of cell pulse. It will be driven high when RxData[7:0] contain the first valid byte of a cell. The RxSOC input is updated on the rising edge of RxClk.
T1/E1 Line Interface			
TSD4 TSD3 TSD2 TSD1	R7 R8 R9 R10	O	**TSDn: Transmit Side Data Output** TSDn contains the transmit data for the n-th link. The TSDn output is updated on the rising edge of TSCKn or TSCCK if common clock is used.
TSCK4 TSCK3 TSCK2 TSCK1	T7 T8 P9 P10	I	**TSCKn: Transmit Side Clock** TSCKn contains the transmit clock for the n-th link. **Note:** If unused, TSCKn should be connected to ground.
TSF4 TSF3 TSF2 TSF1	P8 T9 T10 T11	I	**TSFn: Transmit Side Frame pulse** TSFn is used to delineate each frame for the n-th link. The TSFn input is sampled on the falling edge of TSCKn or TSCCK if common clock is used. **Note:** If unused, TSFn should be connected to ground.
TSCCK	P1	I	**TSCCK: Transmit Side Common Clock** TSCCK is the transmit clock for links that are configured in Common Clock Mode. **Note:** If unused, TSCCK should be connected to ground.
TSCFS	P2	I	**TSCFS: Transmit Side Common Frame Pulse** This signal is used to delineate each frame for links that are configured in Common Clock Mode. The TSCFS input is sampled on the falling edge of TSCCK. **Note:** If unused, TSCFS should be connected to ground.

Table-1 Pin Description (Continued)

Name	Pin Number	Input/Output	Description
RSD4 RSD3 RSD2 RSD1	H2 G2 F2 E2	I	**RSDn: Receive Side Data Input** RSDn contains the receive data for the n-th link. The RSDn input is sampled on the falling edge of RSCKn or RSCCK if common clock is used. **Note:** If unused, RSDn should be connected to ground.
RSCK4 RSCK3 RSCK2 RSCK1	H1 G1 F1 E1	I	**RSCKn: Receive Side Clock** RSCKn contains the recovered line clock for the n-th link. **Note:** If unused, RSCKn should be connected to ground.
RSF4 RSF3 RSF2 RSF1	J1 H3 G3 F3	I	**RSFn: Receive Side Frame Pulse** RSFn is used to delineate each frame for the n-th link. The RSFn input is sampled on the falling edge of RSCKn or RSCCK if common clock is used. **Note:** If unused, RSFn should be connected to ground.
RSCCK	N3	I	**RSCCK: Receive Side Common Clock** RSCCK is the receive clock for links that are configured in Common Clock Mode. **Note:** If unused, RSCCK should be connected to ground.
RSCFS	N2	I	**RSCFS: Receive Side Common Frame Pulse** RSCFS is used to delineate each frame for links that are configured in Common Clock Mode. The RSCFS input is sampled on the falling edge of RSCCK. **Note:** if unused, RSCFS should be connected to ground.
Microprocessor Interface			
MPM	P15	I	**MPM: Microprocessor Interface Mode** Connected to VDD for Intel; connected to GND for Motorola.
$\overline{RD}/\overline{DS}$	M15	I	**$\overline{RD}$: Read Operation** In parallel Intel microprocessor interface mode, this pin is asserted low by the microprocessor to initiate a read cycle. Data is output to D[7:0] from the device. **$\overline{DS}$: Data Strobe** In parallel Motorola microprocessor interface mode, this pin is the data strobe of the parallel interface. During a write operation ($R\overline{W}$=0), data on D[7:0] is sampled into the device. During a read operation ($R\overline{W}$=1), data is output to D[7:0] from the device.
$\overline{WR}/R\overline{W}$	M16	I	**$\overline{WR}$: Write Operation** In parallel Intel microprocessor interface mode, this pin is asserted low by the microprocessor to initiate a write cycle. Data on D[7:0] is sampled into the device during a write operation. **$R\overline{W}$: Read/Write Select** In parallel Motorola microprocessor interface mode, this pin is asserted low for write operation and high for read operation.
D7 D6 D5 D4 D3 D2 D1 D0	P14 P13 R16 R15 R14 R13 T15 T14	I/O	**D[7:0]: Data Bus** These pins function as a bi-directional data bus of the microprocessor interface.

Table-1 Pin Description (Continued)

Name	Pin Number	Input/Output	Description
A7 A6 A5 A4 A3 A2 A1 A0	M14 M13 N16 N15 N14 N13 N12 P16	I	**A[7:0]: Address Bus** These pins function as an address bus of the microprocessor interface.
$\overline{CS}$	L13	I	**$\overline{CS}$: Chip Select** For each read or write operation, this pin must be changed from high to low, and remains low until the operation is over.
$\overline{INT}$	R12	Open_drain	**$\overline{INT}$: Interrupt Request** A low level on this pin indicates that an interrupt is pending inside the chip.
SRAM Interface			
EMD7 EMD6 EMD5 EMD4 EMD3 EMD2 EMD1 EMD0	D4 C4 B4 A4 D5 C5 B5 A5	I/O	**EMD[7:0]: Data Bus** Data Input/Output pins for the external SRAM. Used for data exchange between the IDT82V2604 and the external SRAM.
EMA18 EMA17 EMA16 EMA15 EMA14 EMA13 EMA12 EMA11 EMA10 EMA9 EMA8 EMA7 EMA6 EMA5 EMA4 EMA3 EMA2 EMA1 EMA0	A6 C7 B7 A7 C8 B8 A8 A9 B9 C9 A10 B10 C10 A11 B11 C11 D11 A12 B12	O	**EMA[18:0]: Address Bus** Address of the external SRAM. Used to select a data entry in the external SRAM.
$\overline{EM\_WE}$	D6	O	**$\overline{EM\_WE}$: Write Enable** Write enable signal for the external SRAM. When $\overline{EM\_WE}$ pin and $\overline{EM\_CS}$ pin are both low, data can be written to the external SRAM.
$\overline{EM\_OE}$	B6	O	**$\overline{EM\_OE}$: Output Enable** Output enable signal for the external SRAM. When $\overline{EM\_OE}$ pin and $\overline{EM\_CS}$ pin are both low, data can be read from the external SRAM.
$\overline{EM\_CS}$	C6	O	**$\overline{EM\_CS}$: Chip Select** Chip enable signal for the external SRAM.

Table-1 Pin Description (Continued)

Name	Pin Number	Input/Output	Description
			JTAG & Scan Interface
TCK	**C2**	**I**	**TCK: JTAG Test Clock** This pin is the input clock for JTAG.
TMS	**B1**	**I**	**TMS: JTAG Test Mode Select** This pin has an internal pull-up resistor.
TDI	**B2**	**I**	**TDI: JTAG Test Data Input** This pin is used to load instructions and data into the test logic and has an internal pull-up resistor.
TDO	**D2**	**High-Z**	**TDO: JTAG Test Data Output** This is normally high impedance and is used to read all the serial configuration and test data from the test logic.
$\overline{\text{TRST}}$	**C1**	**I**	**$\overline{\text{TRST}}$: JTAG Test Port Reset** This pin has an internal pull-up resistor.
			Power Supplies and Grounds
VDD	**D7,D10,E3,F4,G4,G13, K4,K13,L4,M4,N4,N5, N6,N7,N10,N11,P3, P12,R1,T2**	**-**	**3.3V Power Supply**
GND	**A1,A16,D8,D9,G7,G8, G9,G10,H4,H7,H8,H9, H10,H13,J4,J7,J8,J9, J10,J13,K7,K8,K9, K10,N8,N9,T1,T16**	**-**	**Ground**
			Others
IC	**L16**	**-**	**IC: Internal Connected** Internal use. For normal operation, these pins should be connected to VDD.
IC	**A2,A3,B3,C3,D3,J2, J3,K1,K2,K3,L1,L2,L3, L15,M1,M2,M3,N1,P4, P5,P6,P7,P11,T3,T4, T5,T6,T12**	**-**	**IC: Internal Connected** Internal use. For normal operation, these pins should be connected to ground.
IC	**K14,K15,K16,L14,R3, R4,R5,R6**	**-**	**IC: Internal Connected** Internal use. For normal operation, these pins should be left open.
NC	**D1,R2,T13**	**-**	**NC: No Connection**

3 INTERFACE

3.1 UTOPIA INTERFACE

The Utopia interface operates in Level 2 mode. The IDT82V2604 supports up to 4 Utopia Level 2 ports. Each port is assigned an address ranging from 0 to 30. The address value of 31 is reserved and should not be used. All the 31 ports can be individually enabled or disabled by **ConfigUtopiaIF** command.

Each IMA group or UNI link corresponds to a port. For each IMA group, the port address can be assigned by **ConfigGroupInterface** command. For each UNI link, the port address can be assigned by **ConfigUNILink** command. Inside the device, each port corresponds to a GCF (Group Cell FIFO) which is 2 cells deep.

The IDT82V2604 uses cell level handshake for cell transfer. One entire cell is transferred before another port can be selected. The start of a cell is marked by TxSOC and RxSOC signals in the transmit and the receive directions respectively. These two signals are active during the first byte of a cell.

3.1.1 UTOPIA LOOPBACK FUNCTION

For diagnostic purpose, the capability to loop back all Utopia traffic to Utopia bus is provided. This loopback is called Utopia loopback and can be enabled by **ConfigLoopMode** command. In this mode, cells are taken from TGCFs (Transmit Group Cell FIFO) and sent to the respective RGCFs (Receive Group Cell FIFO). When in Utopia loopback mode, cells will not be transmitted to the line interface. Refer to Figure-3.

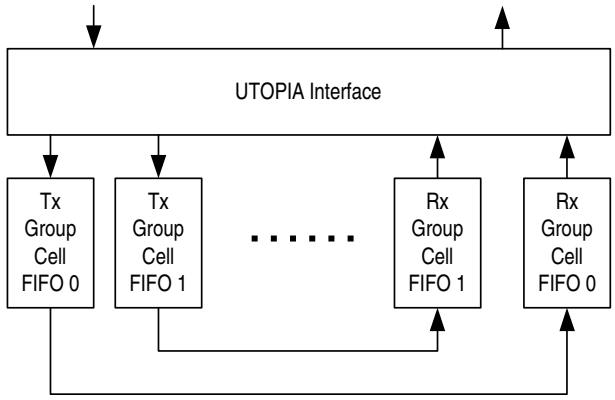


Figure-3 Utopia Loopback

3.2 LINE INTERFACE

3.2.1 LINE INTERFACE WORK MODES

For different framers, the line interface can be configured to different Work Mode to adapt to different data format. Figure-4 shows all the 16 Work Modes and Table-2 lists IMA layer data rate for each mode.

In channelized mode, all the framing bits and signalling bits are set to zero in transmit direction. And all the received signalling bits and framing bits are discarded in receive direction. In unchannelized mode, all bits are utilized for data transfer.

Work Mode is selected by **AddTxLink** or **AddRxLink** command when a link is in an IMA group. The Work Mode is selected by **ConfigUNILink** command when a link is used as a UNI link.

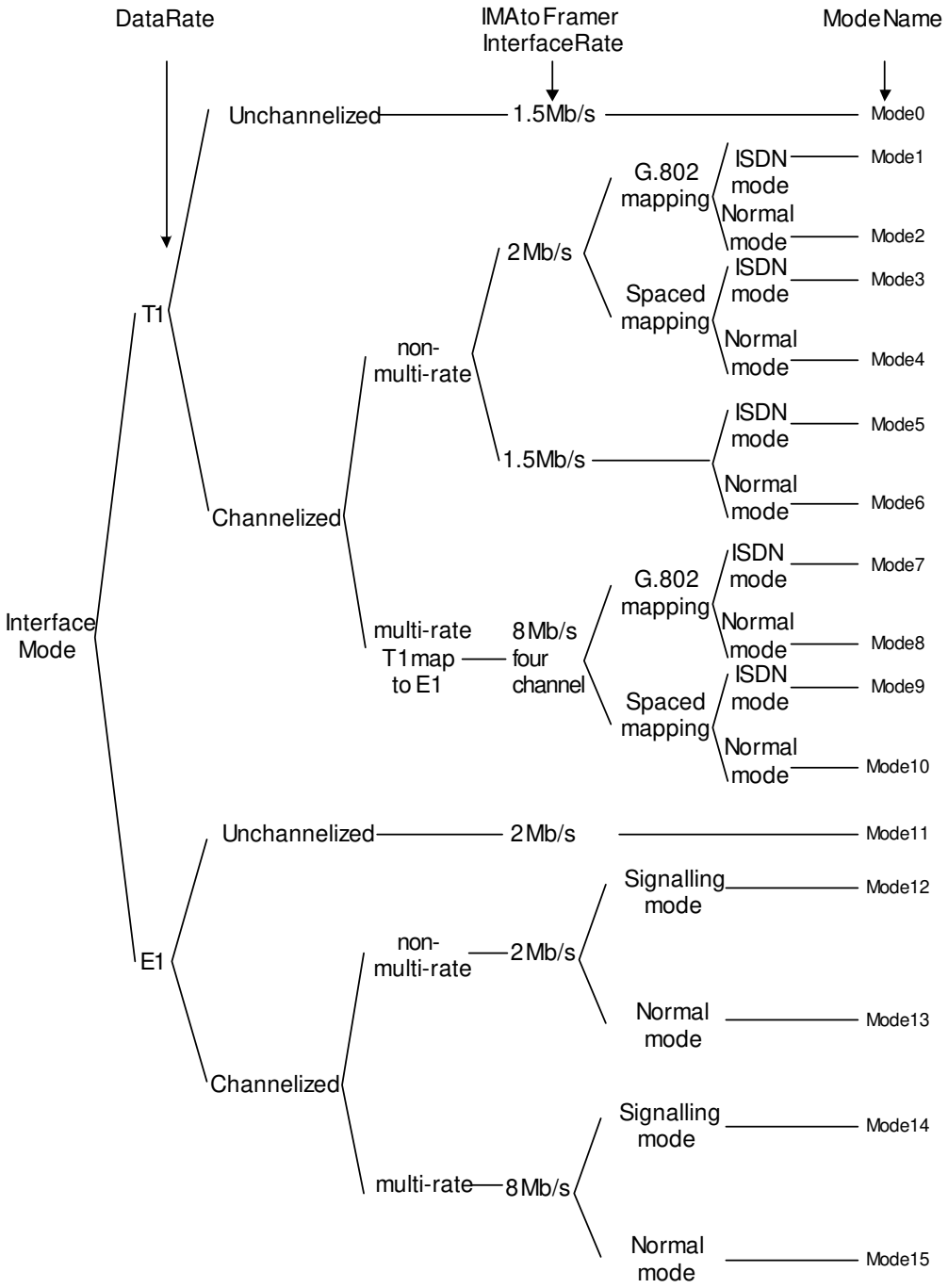


Figure-4 Line Interface Work Modes

Table-2 Data Rates of Different Modes

Mode	IMA Data Rate Per Channel (Maximum)	Interface Clock (Maximum)
Mode0	1.544 Mb/s	1.544 MHz
Mode1	1.472 Mb/s	2.048 MHz
Mode2	1.536 Mb/s	2.048 MHz
Mode3	1.472 Mb/s	2.048 MHz
Mode4	1.536 Mb/s	2.048 MHz
Mode5	1.472 Mb/s	1.544 MHz
Mode6	1.536 Mb/s	1.544 MHz
Mode7	1.472 Mb/s	8.192 MHz
Mode8	1.536 Mb/s	8.192 MHz
Mode9	1.472 Mb/s	8.192 MHz
Mode10	1.536 Mb/s	8.192 MHz
Mode11	2.048 Mb/s	2.048 MHz
Mode12	1.920 Mb/s	2.048 MHz
Mode13	1.984 Mb/s	2.048 MHz
Mode14	1.920 Mb/s	8.192 MHz
Mode15	1.984 Mb/s	8.192 MHz

3.2.1.1 Mode0

In this mode, the transmit and receive data are viewed as a continuous 1.544 Mb/s serial stream. There is no concept of time slot in an unchannelized link. Each eight bits are grouped into an octet with arbitrary alignment. The first bit received/transmitted is the most significant bit of an octet while the last bit is the least significant bit. The 1.544 MHz data stream clock is provided by the system.

The 1.544 MHz clock in Tx and Rx directions can be either common clock or independent clock. If common clock is used, TSCCK and RSCCK are used as Tx clock and Rx clock respectively, and TSCFS and RSCFS are used as common frame pulse in Tx and Rx directions respectively. If independent clock is used, TSCK[i] and RSCK[i] are used as Tx clock and Rx clock respectively, and TSF[i] and RSF[i] are used as the frame pulse in Tx and Rx directions respectively.

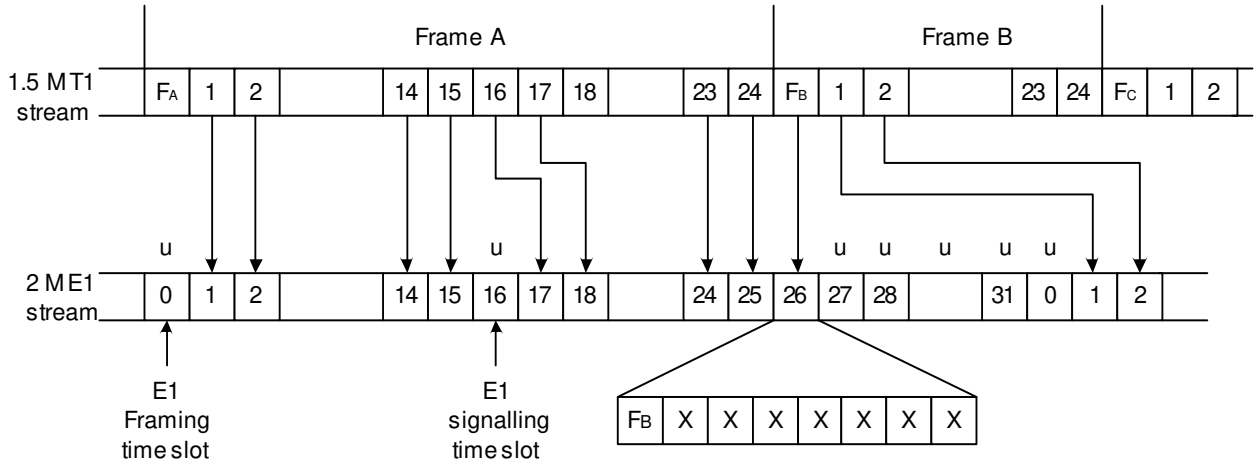
3.2.1.2 Mode1~Mode4

In these four modes, the transmit/receive data rate is T1 channelized while the line interface timing clock is 2.048 MHz (E1 clock). Thus the mapping between T1 frame and E1 frame is needed. Two mapping modes can be used: G.802 mapping mode and spaced mapping mode. Each mapping mode can be further divided into two data modes: T1 ISDN mode and T1 normal mode. The mapping is done in a frame-by-frame fashion and the unassigned time slots are set to zero.

In these modes, the clock for Tx and Rx can be either common clock or independent clock. If common clock is used, TSCCK and RSCCK are used as Tx clock and Rx clock respectively, and TSCFS and RSCFS are used as common frame pulse in Tx and Rx directions respectively. If independent clock is used, TSCK[i] and RSCK[i] are used as Tx clock and Rx clock respectively, and TSF[i] and RSF[i] are used as the frame pulse in Tx and Rx directions respectively.

G.802 Mapping

This mode supports ITU-T Recommendation G.802, which describes how 24 (or 23, in signalling mode) T1 time slots and one framing bit (totally 193/185 bits per T1/T1-ISDN frame) are mapped to 32 E1 time slots (256 bits). This mapping is done by mapping the 24 (or 23 in T1-ISDN mode) T1 time slots to TS1~TS15 and TS17~TS25 (or TS17~TS24), and mapping the framing bit to bit 1 of TS26/TS25. TS0, TS16, TS27/TS26 through TS31 are all unassigned and set to zero (refer to Figure-5).

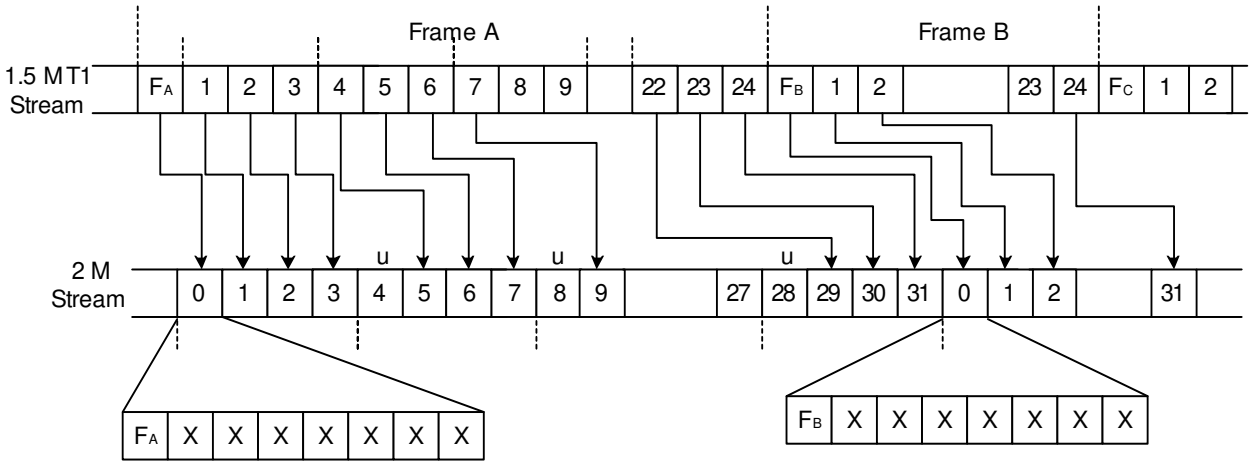


1. X=unused bit
2. u=unassigned time slot
3. F_A, F_B and F_C are T1 framing bits for frame A, B and C respectively.

Figure-5 G.802 Mapping Mode

Spaced Mapping

In this mode, T1 to E1 mapping makes every fourth time slot unassigned (i.e., 4, 8, 12, 16, 20, 24 and 28). Refer to Figure-6. Suppose T1 time slot x is mapped to E1 time slot y. We have y=x+int((x-1)/3), where int(n) is the largest integer no greater than n. The framing bit is assigned to the first bit of TS0. This distribution of unassigned time slots averages out the idle time slots and optimizes the framer's slip buffer's usage.



1. X=unused bits
2. u=unassigned time slot
3. F_A, F_B and F_C are T1 framing bits for frame A, B and C respectively.
4. Mapping rule: If T1 time slot x is mapped to E1 time slot y, y = x+int(x/3). Here int(n) is the largest integer no greater than n.

Figure-6 Spaced Mapping Mode

T1 ISDN Mode

The T1 ISDN mode corresponds to the use of 23 time slots to transmit data, that is, T1 data is not transmitted during the framing bit and time slot 24. Therefore, only 23 time slots are considered useful and are mapped while time slot 24 and the framing bit are meaningless and are not mapped.

T1 Normal Mode

In this mode, data is not transmitted during the framing bit. The other 24 time slots are useful.

3.2.1.3 Mode5~Mode6

In these modes, the transmit/receive data rate is T1 channelized, and the line interface timing clock is 1.544 MHz (T1 clock). The ISDN mode and normal mode are defined in T1 ISDN Mode and T1 Normal Mode on page 21.

In these modes, the clock for Tx and Rx can be either common clock or independent clock. If common clock is used, TSCCK and RSCCK are used as Tx clock and Rx clock respectively, and TSCFS and RSCFS are used as common frame pulse in Tx and Rx directions respectively. If independent clock is used, TSCK[i] and RSCK[i] are used as Tx clock and Rx clock respectively, and TSF[i] and RSF[i] are used as the frame pulse in Tx and Rx directions respectively.

3.2.1.4 Mode7~Mode10

In these modes, only TSCCK and RSCCK are used to input the 8.192 MHz clock in Tx and Rx directions respectively, and TSCFS and RSCFS are used as common frame pulse in Tx and Rx directions respectively. All the TSCK[i], TSF[i], RSCK[i] and RSF[i] pins are not used and should be connected to ground. The unused RSD pins should also be connected to ground.

The data pins used for multiplexing are shown in the table below:

Table-3 Pins Used in Multi-Rate Multiplex Mode

Tx Pin Name	Rx Pin Name	Multiplexed Channel
TSD[1]	RSD[1]	channel 1~channel 4

Multi-rate

Multi-rate is used for multiplexing four E1 streams into one high-speed stream. Figure-7 shows four 2.048 MHz E1 streams multiplexed into a single 8.192 MHz stream through one data pin. The multiplexing uses the round-robin technology. The system provides 8.192 MHz common clock and 8 kHz common frame pulse.

For T1 channel, before multiplexing, a mapping from each T1 frame to E1 frame is first done. Then the mapped 4 E1 channels are multiplexed into one 8.192 MHz stream as shown in Figure-7.

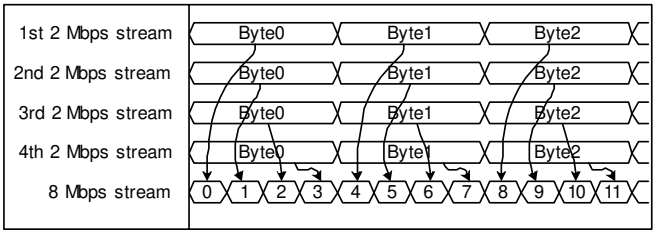


Figure-7 Multiplexing Four 2 MHz Streams into One 8 MHz Stream

T1 Multi-Rate Mode

Since there are two T1 to E1 mapping methods that can be used as described in G.802 Mapping and Spaced Mapping on page 19, two new modes can be derived when multiplexing is further used. Again, T1 ISDN data mode and T1 normal mode can be applied, thus we have 4 more modes: mode7~mode10.

3.2.1.5 Mode11

In this mode, the transmit and receive data are viewed as a continuous 2.048 Mb/s serial stream. There is no concept of time slot in an unchannelized link. Each eight bits are grouped into an octet. TSF or TSCFS signal determine whether the data stream is in byte alignment or not. The first bit received/transmitted is the most significant bit of an octet while the last bit is the least significant bit. The 2.048 MHz data stream clock is provided by the system.

In this mode, the clock for Tx and Rx can be either common clock or independent clock. If common clock is used, TSCCK and RSCCK are used as Tx clock and Rx clock respectively. If independent clock is used, the clock for the i-th link comes from TSCK[i] and RSCK[i] in Tx and Rx directions respectively.

In Common Clock Mode, the TSCFS signal is used for byte alignment pulse for the transmitted bit stream while in Independent Clock Mode, the TSF[i] signal is used for byte alignment pulse for the i-th transmit link.

The frequency for TSF[i] (or TSCSF) is the result of TSCK[i] (or TSCCK) divided by 256 and the pulse width of this signal is one cycle of TSCK[i] or TSCCK signal.

3.2.1.6 Mode12~Mode13

These two modes are E1 non-multi-rate combined with different signalling modes. The non-multi-rate is the channelized generic E1 interface, i.e., a 2.048 MHz channel is divided into 32 sub-channels (also called time slots), and these sub-channels are used to exchange data.

In these modes, the clock for Tx and Rx can be either common clock or independent clock. If common clock is used, TSCCK and RSCCK are used as Tx clock and Rx clock respectively, and TSCFS and RSCFS are used as common frame pulse in Tx and Rx directions respectively. If independent clock is used, TSCK[i] and RSCK[i] are used as Tx clock and Rx clock respectively, and TSF[i] and RSF[i] are used as the frame pulse in Tx and Rx directions respectively.

Channelized Non-Multi-Rate E1

In this mode, the system provides 2.048 MHz clock and 8 kHz frame pulse for E1 bit stream exchange between the IDT82V2604 and the line interface. The E1 time slot 0 is not used for data exchange while time slot 16 may or may not be used for data exchange, depending on Signalling or Non-Signalling mode.

Signalling and Non-Signalling

In signalling mode, time slot 0 and time slot 16 are not used for data exchange between the IDT82V2604 and the line interface. In non-signalling mode, only time slot 0 is not used for data exchange.

3.2.1.7 Mode14~Mode15

The multi-rate concept is defined in Multi-rate on page 21, and the signalling and non-signalling concepts are defined in Signalling and Non-Signalling on page 22. The system provides 8.192 MHz common clock and 8 kHz common frame pulse.

In these modes, only the TSCCK and RSCCK pins are used to input the 8.192 MHz clock in Tx and Rx directions respectively, and TSCFS and RSCFS are used as common frame pulse in Tx and Rx directions respectively. The TSCK[i], TSF[i], RSCK[i] and RSF[i] pins are not used and should be connected to ground. The unused RSD pins should also be connected to ground.

The data pins used for multiplexing are shown in Table-3.

3.2.2 LINE INTERFACE TIMING CLOCK MODES

Two timing clock modes can be selected. One is Common Clock Mode, the other is Independent Clock Mode. The timing clock mode can be individually configured for each link. In IMA mode, **AddTxLink** command and **AddRxLink** command can be used to configure the clock mode in the transmit and receive directions respectively. In UNI mode, **ConfigUNILink** command can be used to configure the clock mode.

If a link is configured in Common Clock Mode, TSCCK and RSCCK are used as Tx clock and Rx clock respectively, and TSCFS and RSCFS are used as common frame pulse in Tx and Rx directions respectively.

If a link is configured in Independent Clock Mode, TSCK[i] and RSCK[i] are used as Tx clock and Rx clock respectively, and TSF[i] and RSF[i] are used as the frame pulse in Tx and Rx directions respectively.

These two timing clock modes can be configured at the same time, i.e., some links can work in Common Clock Mode while other links can work in Independent Clock Mode.

The line interface mode7~mode10 and mode14~mode15 cannot be used in Independent Clock Mode.

3.2.3 LINE INTERFACE LOOPBACK FUNCTION

The line interface supports two line loopback functions, one is external loopback mode and the other is internal loopback mode. The two loopback modes can be selected by **ConfigLoopMode** command.

In external loopback mode, all the data received at the line side is looped back to the transmit side and is transmitted out. When this function is enabled, all the links will be in external loopback mode. Data will not be transmitted to the Utopia interface.

In internal loopback mode, the data transmitted are also sent to the receive side. When this function is enabled, all the links will be in internal loopback mode. Data will not be transmitted to the FE Utopia interface.

3.3 EXTERNAL MICROPROCESSOR INTERFACE

The IDT82V2604 uses an embedded controller and a downloaded software (IMAOS04 or IMAOS04_Slave[1]) to communicate with the external microprocessor. The external microprocessor sends commands to configure the device and read feedbacks. The downloaded software interprets these commands and the embedded controller executes these commands. This relieves programmers from accessing vast registers. Just by accessing a few registers, programmers can use a set of well-defined commands to communicate with IDT82V2604.

3.3.1 EXTERNAL MICROPROCESSOR INTERFACE SELECTION

The IDT82V2604 supports both non-multiplexed Intel and non-multiplexed Motorola microprocessor interfaces. For Intel microprocessor interface, the MPM pin should be connected to VDD; for Motorola microprocessor interface, the MPM pin should be connected to ground.

1. IMAOS04 is used when the device is in normal communication while IMAOS04_Slave is used when the device operates in Slave Mode. Refer to 8.1 Group Auto Detect.

3.3.2 COMMAND FIFOS

The embedded controller uses two FIFOs to communicate with the external microprocessor. One is Input FIFO, which is used to receive commands and data from the external microprocessor; the other is Output FIFO, which is used to send data to the external microprocessor. The lengths of these two FIFOs are both 16 bytes. These two FIFOs can only be accessed through registers.

3.3.3 REGISTERS

The IDT82V2604 provides 9 registers for the external microprocessor to load software to the device, send commands and read feedbacks.

3.3.4 REGISTER MAP

Table-4 Register Map

Address (Hex)	Register	R/W	Map							
			b7	b6	b5	b4	b3	b2	b1	b0
00	INPUT_FIFO_LENGTH_REG	R/W	-	-	-	Input_Message_Length[4:0]				
01	OUTPUT_FIFO_LENGTH_REG	R	-	-	-	Output_Message_Length[4:0]				
02	OUTPUT_FIFO_DATA_REG	R	Output_Data[7:0]							
03	INPUT_FIFO_DATA_REG	R/W	Input_Data[7:0]							
04	FIFO_INT_ENABLE_REG	R/W	-	-	-	-	-	Input_FIFO_empty_int_en	Input_FIFO_overflow_int_en	Output_FIFO_msg_available_int_en
05	FIFO_STATE_REG	R	HW_version					Input_FIFO_empty_state	Input_FIFO_overflow_state	Output_FIFO_msg_available_state
06	FIFO_INT_RESET_REG	W	-	-	-	-	-	-	Input_FIFO_overflow&empty_int_rst	Output_FIFO_msg_available_int_rst
07	OUTPUT_FIFO_INTERNAL_STATE_REG	R	-	-	-	Output_remain_msg_length[4:0]				
08	INPUT_FIFO_INTERNAL_STATE_REG	R	-	-	-	Input_remain_msg_length[4:0]				

3.3.5 REGISTER DESCRIPTION

Table-5 Input FIFO Data Length Register (INPUT_FIFO_LENGTH_REG)
(R/W, Address=00H)

Symbol	Position	Default	Description
-	7-5	0	Reserved.
Input_Message_Length[4:0]	4-0	0	These 5 bits contain the message length in the Input FIFO which should be written after the message is sent to the Input FIFO. The valid length is from 0 to 16 bytes.

Table-6 Output FIFO Data Length Register (OUTPUT_FIFO_LENGTH_REG)
(R, Address=01H)

Symbol	Position	Default	Description
-	7-5	0	Reserved.
Output_Message_Length[4:0]	4-0	0	These 5 bits contain the length of the message in the Output FIFO. Valid length is from 0 to 16 bytes.

Table-7 Output FIFO Data Register (OUTPUT_FIFO_DATA_REG)
(R, Address=02H)

Symbol	Position	Default	Description
Output_Data[7:0]	7-0	0	These bits contain the data from the message Output FIFO. The complete message can be retrieved by continuously reading this register.

Table-8 Input FIFO Data Register (INPUT_FIFO_DATA_REG)
(R/W, Address=03H)

Symbol	Position	Default	Description
Input_Data[7:0]	7-0	0	These bits contain data to be sent to the Input FIFO. By continuously writing to this register, a complete message can be sent. Before the message is sent, the Input_FIFO_empty_state bit in the EP_interrupt status register should be polled to see whether the Input FIFO is available for writing. After the message is sent, the message length should be written to the EP_Tx_length register.

Table-9 FIFO Interrupt Enable Register (FIFO_INT_ENABLE_REG)
(R/W, Address=04H)

Symbol	Position	Default	Description
-	7-3	0	Reserved.
Input_FIFO_empty_int_en	2	0	Input FIFO empty interrupt enable 0: Interrupt disabled 1: Interrupt enabled
Input_FIFO_overflow_int_en	1	0	Input FIFO overflow interrupt enable 0: Interrupt disabled 1: Interrupt enabled
Output_FIFO_msg_available_int_en	0	0	Output FIFO message available interrupt enable 0: Interrupt disabled 1: Interrupt enabled

Table-10 FIFO Interrupt Status Register (FIFO_STATE_REG)
(R, Address=05H)

Symbol	Position	Default	Description
HW_version	7-3	1	Current device version. For revision A and B, these bits are '0000'. For revision C, these bits are '0001'.
Input_FIFO_empty_state	2	1	Input FIFO availability status 0: Input FIFO is not available for writing. 1: Input FIFO is available for writing.
Input_FIFO_overflow_state	1	0	Input FIFO overflow status 0: Input FIFO is not full. 1: Input FIFO is full.
Output_FIFO_msg_available_state	0	0	Output FIFO message availability status 0: No message is in the Output FIFO. 1: A message is in the Output FIFO.

Table-11 FIFO Interrupt Reset Register (FIFO_INT_RESET_REG)
(W, Address=06H)

Symbol	Position	Default	Description
-	7-2	0	Reserved.
Input_FIFO_overflow&empty_int_rst	1	0	Write '1' to clear the Input_FIFO_overflow_state status and Input_FIFO_empty_state status.
Output_FIFO_msg_available_int_rst	0	0	Write '1' to clear the Output_FIFO_msg_available_state status.

Table-12 Output FIFO Internal State Register (OUTPUT_FIFO_INTERNAL_STATE_REG)
(R, Address=07H)

Symbol	Position	Default	Description
-	7-5	0	Reserved.
Output_remain_msg_length[4:0]	4-0	0	The length of the message remaining in the Output FIFO to be read by the external microprocessor.