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Table of Contents

FEATURES	9
HIGHLIGHTS.....	9
MAIN FEATURES	9
OTHER FEATURES.....	9
APPLICATIONS	9
DESCRIPTION	10
FUNCTIONAL BLOCK DIAGRAM	11
1 PIN ASSIGNMENT	12
2 PIN DESCRIPTION	13
3 FUNCTIONAL DESCRIPTION	19
3.1 RESET	19
3.2 MASTER CLOCK	19
3.3 INPUT CLOCKS & FRAME SYNC SIGNAL	20
3.3.1 Input Clocks	20
3.3.2 Frame SYNC Input Signals	20
3.4 INPUT CLOCK PRE-DIVIDER	21
3.5 INPUT CLOCK QUALITY MONITORING	23
3.5.1 LOS Monitoring	23
3.5.2 Activity Monitoring	23
3.5.3 Frequency Monitoring	24
3.6 T0 / T4 DPLL INPUT CLOCK SELECTION	25
3.6.1 External Fast Selection (T0 only)	25
3.6.2 Forced Selection	26
3.6.3 Automatic Selection	26
3.7 SELECTED INPUT CLOCK MONITORING	27
3.7.1 T0 / T4 DPLL Locking Detection	27
3.7.1.1 Fast Loss	27
3.7.1.2 Coarse Phase Loss	27
3.7.1.3 Fine Phase Loss	27
3.7.1.4 Hard Limit Exceeding	27
3.7.2 Locking Status	27
3.7.3 Phase Lock Alarm (T0 only)	28
3.8 SELECTED INPUT CLOCK SWITCH	29
3.8.1 Input Clock Validity	29
3.8.2 Selected Input Clock Switch	29
3.8.2.1 Revertive Switch	29
3.8.2.2 Non-Revertive Switch (T0 only)	30
3.8.3 Selected / Qualified Input Clocks Indication	30
3.9 SELECTED INPUT CLOCK STATUS VS. DPLL OPERATING MODE	31
3.9.1 T0 Selected Input Clock vs. DPLL Operating Mode	31
3.9.2 T4 Selected Input Clock vs. DPLL Operating Mode	33
3.10 T0 / T4 DPLL OPERATING MODE	34
3.10.1 T0 DPLL Operating Mode	34
3.10.1.1 Free-Run Mode	34
3.10.1.2 Pre-Locked Mode	34
3.10.1.3 Locked Mode	34

3.10.1.3.1	Temp-Holdover Mode	34
3.10.1.4	Lost-Phase Mode	34
3.10.1.5	Holdover Mode	34
3.10.1.5.1	Automatic Instantaneous	35
3.10.1.5.2	Automatic Slow Averaged	35
3.10.1.5.3	Automatic Fast Averaged	35
3.10.1.5.4	Manual	35
3.10.1.5.5	Holdover Frequency Offset Read	35
3.10.1.6	Pre-Locked2 Mode	35
3.10.2	T4 DPLL Operating Mode	35
3.10.2.1	Free-Run Mode	35
3.10.2.2	Locked Mode	35
3.10.2.3	Holdover Mode	35
3.11	T0 / T4 DPLL OUTPUT	37
3.11.1	PFD Output Limit	37
3.11.2	Frequency Offset Limit	37
3.11.3	PBO (T0 only)	37
3.11.4	Phase Offset Selection (T0 only)	37
3.11.5	Four Paths of T0 / T4 DPLL Outputs	37
3.11.5.1	T0 Path	37
3.11.5.2	T4 Path	38
3.12	T0 / T4 APLL	39
3.13	OUTPUT CLOCKS & FRAME SYNC SIGNALS	39
3.13.1	Output Clocks	39
3.13.2	Frame SYNC Output Signals	42
3.14	MASTER / SLAVE CONFIGURATION	44
3.15	INTERRUPT SUMMARY	45
3.16	T0 AND T4 SUMMARY	45
3.17	POWER SUPPLY FILTERING TECHNIQUES	46
4	TYPICAL APPLICATION	47
4.1	MASTER / SLAVE APPLICATION	47
5	MICROPROCESSOR INTERFACE	48
5.1	EPROM MODE	49
5.2	MULTIPLEXED MODE	50
5.3	INTEL MODE	52
5.4	MOTOROLA MODE	54
5.5	SERIAL MODE	56
6	JTAG	58
7	PROGRAMMING INFORMATION	59
7.1	REGISTER MAP	59
7.2	REGISTER DESCRIPTION	65
7.2.1	Global Control Registers	65
7.2.2	Interrupt Registers	74
7.2.3	Input Clock Frequency & Priority Configuration Registers	79
7.2.4	Input Clock Quality Monitoring Configuration & Status Registers	102
7.2.5	T0 / T4 DPLL Input Clock Selection Registers	116
7.2.6	T0 / T4 DPLL State Machine Control Registers	120
7.2.7	T0 / T4 DPLL & APLL Configuration Registers	122
7.2.8	Output Configuration Registers	136
7.2.9	PBO & Phase Offset Control Registers	146
7.2.10	Synchronization Configuration Registers	148
8	THERMAL MANAGEMENT	149
8.1	JUNCTION TEMPERATURE	149

8.2	EXAMPLE OF JUNCTION TEMPERATURE CALCULATION	149
8.3	HEATSINK EVALUATION	149
8.4	TQFP EPAD THERMAL RELEASE PATH	150
9	ELECTRICAL SPECIFICATIONS	151
9.1	ABSOLUTE MAXIMUM RATING	151
9.2	RECOMMENDED OPERATION CONDITIONS	151
9.3	I/O SPECIFICATIONS	152
9.3.1	AMI Input / Output Port	152
9.3.1.1	Structure	152
9.3.1.2	I/O Level	152
9.3.1.3	Over-Voltage Protection	154
9.3.2	CMOS Input / Output Port	154
9.3.3	PECL / LVDS Input / Output Port	155
9.3.3.1	PECL Input / Output Port	155
9.3.3.2	LVDS Input / Output Port	157
9.3.3.3	Single-Ended Input for Differential Input	158
9.4	JITTER & WANDER PERFORMANCE	159
9.5	OUTPUT WANDER GENERATION	162
9.6	INPUT / OUTPUT CLOCK TIMING	163
9.7	OUTPUT CLOCK TIMING	164
	PACKAGE DIMENSIONS.....	169
	ORDERING INFORMATION.....	172



List of Tables

Table 1: Pin Description	13
Table 2: Related Bit / Register in Chapter 3.2	19
Table 3: Related Bit / Register in Chapter 3.3	20
Table 4: Related Bit / Register in Chapter 3.4	22
Table 5: Related Bit / Register in Chapter 3.5	24
Table 6: Input Clock Selection for T0 Path	25
Table 7: Input Clock Selection for T4 Path	25
Table 8: External Fast Selection	25
Table 9: Related Bit / Register in Chapter 3.6	26
Table 10: Coarse Phase Limit Programming (the selected input clock of 2 kHz, 4 kHz or 8 kHz)	27
Table 11: Coarse Phase Limit Programming (the selected input clock of other than 2 kHz, 4 kHz and 8 kHz)	27
Table 12: Related Bit / Register in Chapter 3.7	28
Table 13: Conditions of Qualified Input Clocks Available for T0 & T4 Selection	29
Table 14: Related Bit / Register in Chapter 3.8	30
Table 15: T0 DPLL Operating Mode Control	31
Table 16: T4 DPLL Operating Mode Control	33
Table 17: Related Bit / Register in Chapter 3.9	33
Table 18: Frequency Offset Control in Temp-Holdover Mode	34
Table 19: Frequency Offset Control in Holdover Mode	35
Table 20: Holdover Frequency Offset Read	35
Table 21: Related Bit / Register in Chapter 3.10	36
Table 22: Related Bit / Register in Chapter 3.11	38
Table 23: Related Bit / Register in Chapter 3.12	39
Table 24: Outputs on OUT1 ~ OUT7 if Derived from T0/T4 DPLL Outputs	40
Table 25: Outputs on OUT1 ~ OUT7 if Derived from T0/T4 APLL	41
Table 26: Outputs on OUT8 & OUT9	41
Table 27: Synchronization Control	42
Table 28: Related Bit / Register in Chapter 3.13	43
Table 29: Device Master / Slave Control	44
Table 30: Related Bit / Register in Chapter 3.15	45
Table 31: Microprocessor Interface	48
Table 32: Access Timing Characteristics in EPROM Mode	49
Table 33: Read Timing Characteristics in Multiplexed Mode	50
Table 34: Write Timing Characteristics in Multiplexed Mode	51
Table 35: Read Timing Characteristics in Intel Mode	52
Table 36: Write Timing Characteristics in Intel Mode	53
Table 37: Read Timing Characteristics in Motorola Mode	54
Table 38: Write Timing Characteristics in Motorola Mode	55
Table 39: Read Timing Characteristics in Serial Mode	56
Table 40: Write Timing Characteristics in Serial Mode	57
Table 41: JTAG Timing Characteristics	58
Table 42: Register List and Map	59
Table 43: Power Consumption and Maximum Junction Temperature	149
Table 44: Thermal Data	149
Table 45: Absolute Maximum Rating	151
Table 46: Recommended Operation Conditions	151
Table 47: AMI Input / Output Port Electrical Characteristics	153
Table 48: CMOS Input Port Electrical Characteristics	154

Table 49: CMOS Input Port with Internal Pull-Up Resistor Electrical Characteristics	154
Table 50: CMOS Input Port with Internal Pull-Down Resistor Electrical Characteristics	154
Table 51: CMOS Output Port Electrical Characteristics	154
Table 52: PECL Input / Output Port Electrical Characteristics	156
Table 53: LVDS Input / Output Port Electrical Characteristics	157
Table 54: Output Clock Jitter Generation	159
Table 55: Output Clock Phase Noise	160
Table 56: Input Jitter Tolerance (155.52 MHz)	160
Table 57: Input Jitter Tolerance (1.544 MHz)	160
Table 58: Input Jitter Tolerance (2.048 MHz)	160
Table 59: Input Jitter Tolerance (8 kHz)	160
Table 60: T0 DPLL Jitter Transfer & Damping Factor	161
Table 61: T4 DPLL Jitter Transfer & Damping Factor	161
Table 62: Input/Output Clock Timing 3	163
Table 63: Output Clock Timing	164



List of Figures

Figure 1. Functional Block Diagram	11
Figure 2. Pin Assignment (Top View)	12
Figure 3. Pre-Divider for An Input Clock	21
Figure 4. Input Clock Activity Monitoring	23
Figure 5. External Fast Selection	25
Figure 6. Qualified Input Clocks for Automatic Selection	26
Figure 7. T0 Selected Input Clock vs. DPLL Automatic Operating Mode	32
Figure 8. T4 Selected Input Clock vs. DPLL Automatic Operating Mode	33
Figure 9. On Target Frame Sync Input Signal Timing	42
Figure 10. 0.5 UI Early Frame Sync Input Signal Timing	42
Figure 11. 0.5 UI Late Frame Sync Input Signal Timing	43
Figure 12. 1 UI Late Frame Sync Input Signal Timing	43
Figure 13. Physical Connection Between Two Devices	44
Figure 14. IDT82V3280 Power Decoupling Scheme	46
Figure 15. Typical Application	47
Figure 16. EPROM Access Timing Diagram	49
Figure 17. Multiplexed Read Timing Diagram	50
Figure 18. Multiplexed Write Timing Diagram	51
Figure 19. Intel Read Timing Diagram	52
Figure 20. Intel Write Timing Diagram	53
Figure 21. Motorola Read Timing Diagram	54
Figure 22. Motorola Write Timing Diagram	55
Figure 23. Serial Read Timing Diagram (CLKE Asserted Low)	56
Figure 24. Serial Read Timing Diagram (CLKE Asserted High)	56
Figure 25. Serial Write Timing Diagram	57
Figure 26. JTAG Interface Timing Diagram	58
Figure 27. Assembly for Expose Pad thermal Release Path (Side View)	150
Figure 28. 64 kHz + 8 kHz Signal Structure	152
Figure 29. 64 kHz + 8 kHz + 0.4 kHz Signal Structure	152
Figure 30. 64 kHz + 8 kHz / 64 kHz + 8 kHz + 0.4 kHz Signal Input Level	152
Figure 31. 64 kHz + 8 kHz / 64 kHz + 8 kHz + 0.4 kHz Signal Output Level	152
Figure 32. AMI Input / Output Port Line Termination (Recommended)	153
Figure 33. Recommended PECL Input Port Line Termination	155
Figure 34. Recommended PECL Output Port Line Termination	155
Figure 35. Recommended LVDS Input Port Line Termination	157
Figure 36. Recommended LVDS Output Port Line Termination	157
Figure 37. Example of Single-Ended Signal to Drive Differential Input	158
Figure 38. Output Wander Generation	162
Figure 39. Input / Output Clock Timing	163
Figure 40. 100-Pin EQG Package Dimensions (a) (in Millimeters)	169
Figure 41. 100-Pin EQG Package Dimensions (b) (in Millimeters)	170
Figure 42. EQG100 Recommended Land Pattern with Exposed Pad (in Millimeters)	171

FEATURES

HIGHLIGHTS

- The first single PLL chip:
 - Features 0.5 mHz to 560 Hz bandwidth
 - Exceeds GR-253-CORE (OC-12) and ITU-T G.813 (STM-16/Option I) jitter generation requirements
 - Provides node clocks for Cellular and WLL base-station (GSM and 3G networks)
 - Provides clocks for DSL access concentrators (DSLAM), especially for Japan TCM-ISDN network timing based ADSL equipments

MAIN FEATURES

- Provides an integrated single-chip solution for Synchronous Equipment Timing Source, including Stratum 2, 3E, 3, SMC, 4E and 4 clocks
- Employs DPLL and APLL to feature excellent jitter performance and minimize the number of the external components
- Integrates T0 DPLL and T4 DPLL; T4 DPLL locks independently or locks to T0 DPLL
- Supports Forced or Automatic operating mode switch controlled by an internal state machine; the primary operating modes are Free-Run, Locked and Holdover
- Supports programmable DPLL bandwidth (0.5 mHz to 560 Hz in 19 steps) and damping factor (1.2 to 20 in 5 steps)
- Supports 1.1×10^{-5} ppm absolute holdover accuracy and 4.4×10^{-8} ppm instantaneous holdover accuracy
- Supports PBO to minimize phase transients on T0 DPLL output to be no more than 0.61 ns
- Supports phase absorption when phase-time changes on T0 selected input clock are greater than a programmable limit over an interval of less than 0.1 seconds
- Supports programmable input-to-output phase offset adjustment
- Limits the phase and frequency offset of the outputs
- Supports manual and automatic selected input clock switch
- Supports automatic hitless selected input clock switch on clock failure
- Supports three types of input clock sources: recovered clock from STM-N or OC-n, PDH network synchronization timing and external synchronization reference timing
- Provides a 2 kHz, 4 kHz or 8 kHz frame sync input signal, and a 2 kHz and an 8 kHz frame sync output signals
- Provides 14 input clocks whose frequency cover from 2 kHz to 622.08 MHz
- Provides 9 output clocks whose frequency cover from 1 Hz to 622.08 MHz
- Provides output clocks for BITS, GPS, 3G, GSM, etc.
- Supports AMI, PECL/LVDS and CMOS input/output technologies
- Supports master clock calibration
- Supports Master/Slave application (two chips used together) to enable system protection against single chip failure
- Meets Telcordia GR-1244-CORE, GR-253-CORE, GR-1377-CORE, ITU-T G.812, ITU-T G.813 and ITU-T G.783 criteria

OTHER FEATURES

- Multiple microprocessor interface modes: EPROM, Multiplexed, Intel, Motorola and Serial
- IEEE 1149.1 JTAG Boundary Scan
- Single 3.3 V operation with 5 V tolerant CMOS I/Os
- 100-pin TQFP package, Green package options available

APPLICATIONS

- BITS / SSU
- SMC / SEC (SONET / SDH)
- DWDM cross-connect and transmission equipments
- Central Office Timing Source and Distribution
- Core and access IP switches / routers
- Gigabit and Terabit IP switches / routers
- IP and ATM core switches and access equipments
- Cellular and WLL base-station node clocks
- Broadband and multi-service access equipments
- Any other telecom equipments that need synchronous equipment system timing

DESCRIPTION

The IDT82V3280 is an integrated, single-chip solution for the Synchronous Equipment Timing Source for Stratum 2, 3E, 3, SMC, 4E and 4 clocks in SONET / SDH equipments, DWDM and Wireless base station, such as GSM, 3G, DSL concentrator, Router and Access Network applications.

The device supports three types of input clock sources: recovered clock from STM-N or OC-n, PDH network synchronization timing and external synchronization reference timing.

Based on ITU-T G.783 and Telcordia GR-253-CORE, the device consists of T0 and T4 paths. The T0 path is a high quality and highly configurable path to provide system clock for node timing synchronization within a SONET / SDH network. The T4 path is simpler and less configurable for equipment synchronization. The T4 path locks independently from the T0 path or locks to the T0 path.

An input clock is automatically or manually selected for T0 and T4 each for DPLL locking. Both the T0 and T4 paths support three primary operating modes: Free-Run, Locked and Holdover. In Free-Run mode, the DPLL refers to the master clock. In Locked mode, the DPLL locks to the selected input clock. In Holdover mode, the DPLL resorts to the fre-

quency data acquired in Locked mode. Whatever the operating mode is, the DPLL gives a stable performance without being affected by operating conditions or silicon process variations.

If the DPLL outputs are processed by T0/T4 APLL, the outputs of the device will be in a better jitter/wander performance.

The device provides programmable DPLL bandwidths: 0.5 mHz to 560 Hz in 19 steps and damping factors: 1.2 to 20 in 5 steps. Different settings cover all SONET / SDH clock synchronization requirements.

A high stable input is required for the master clock in different applications. The master clock is used as a reference clock for all the internal circuits in the device. It can be calibrated within ± 741 ppm.

All the read/write registers are accessed through a microprocessor interface. The device supports five microprocessor interface modes: EPROM, Multiplexed, Intel, Motorola and Serial.

In general, the device can be used in Master/Slave application. In this application, two devices should be used together to enable system protection against single chip failure. See [Chapter 4 Typical Application](#) for details.

FUNCTIONAL BLOCK DIAGRAM

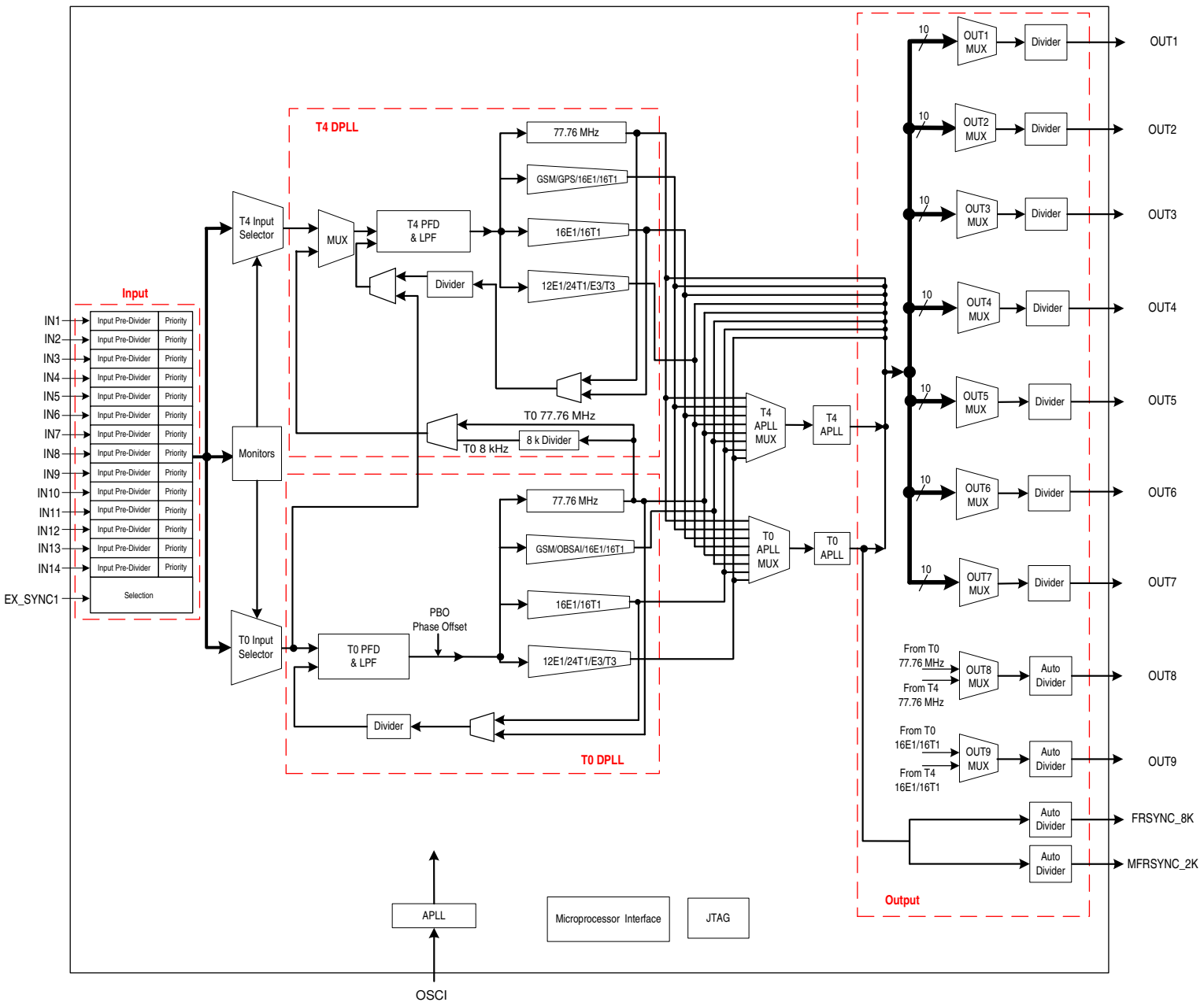


Figure 1. Functional Block Diagram

1 PIN ASSIGNMENT

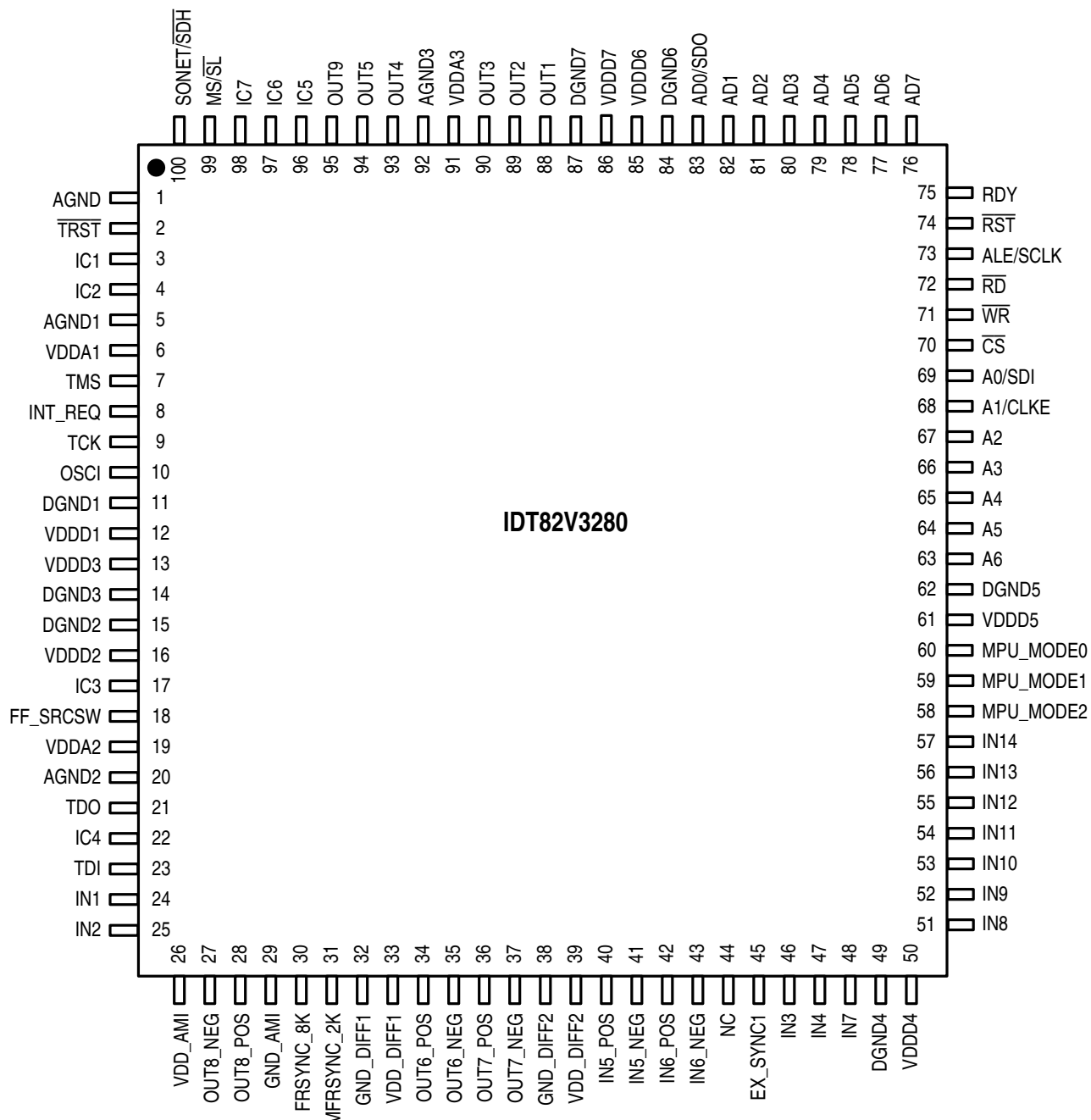


Figure 2. Pin Assignment (Top View)

2 PIN DESCRIPTION

Table 1: Pin Description

Name	Pin No.	I/O	Type	Description ¹
Global Control Signal				
OSCI	10	I	CMOS	OSCI: Crystal Oscillator Master Clock A nominal 12.8000 MHz clock provided by a crystal oscillator is input on this pin. It is the master clock for the device.
FF_SRC SW	18	I pull-down	CMOS	FF_SRC SW: External Fast Selection Enable During reset, this pin determines the default value of the EXT_SW bit (b4, 0BH) ² . The EXT_SW bit determines whether the External Fast Selection is enabled. High: The default value of the EXT_SW bit (b4, 0BH) is '1' (External Fast selection is enabled); Low: The default value of the EXT_SW bit (b4, 0BH) is '0' (External Fast selection is disabled). After reset, this pin selects an input clock pair for the T0 DPLL if the External Fast selection is enabled: High: Pair IN3 / IN5 is selected. Low: Pair IN4 / IN6 is selected. After reset, the input on this pin takes no effect if the External Fast selection is disabled.
MS/SL	99	I pull-up	CMOS	MS/SL: Master / Slave Selection This pin, together with the MS_SL_CTRL bit (b0, 13H), controls whether the device is configured as the Master or as the Slave. Refer to Chapter 3.14 Master / Slave Configuration for details. The signal level on this pin is reflected by the MASTER_SLAVE bit (b1, 09H).
SONET/SDH	100	I pull-down	CMOS	SONET/SDH: SONET / SDH Frequency Selection During reset, this pin determines the default value of the IN_SONET_SDH bit (b2, 09H): High: The default value of the IN_SONET_SDH bit is '1' (SONET); Low: The default value of the IN_SONET_SDH bit is '0' (SDH). After reset, the value on this pin takes no effect.
RST	74	I pull-up	CMOS	RST: Reset A low pulse of at least 50 μ s on this pin resets the device. After this pin is high, the device will still be held in reset state for 500 ms (typical).
Frame Synchronization Input Signal				
EX_SYNC1	45	I pull-down	CMOS	EX_SYNC1: External Sync Input 1 A 2 kHz, 4 kHz or 8 kHz signal is input on this pin.
Input Clock				
IN1	24	I	AMI	IN1: Input Clock 1 A 64 kHz + 8 kHz or 64 kHz + 8 kHz + 0.4 kHz composite clock is input on this pin.
IN2	25	I	AMI	IN2: Input Clock 2 A 64 kHz + 8 kHz or 64 kHz + 8 kHz + 0.4 kHz composite clock is input on this pin.
IN3	46	I pull-down	CMOS	IN3: Input Clock 3 A 2 kHz, 4 kHz, N x 8 kHz ³ , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is input on this pin.
IN4	47	I pull-down	CMOS	IN4: Input Clock 4 A 2 kHz, 4 kHz, N x 8 kHz ³ , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is input on this pin.

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description ¹
IN5_POS IN5_NEG	40 41	I	PECL/LVDS	IN5_POS / IN5_NEG: Positive / Negative Input Clock 5 A 2 kHz, 4 kHz, N x 8 kHz ³ , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz or 622.08 MHz clock is differentially input on this pair of pins. Whether the clock signal is PECL or LVDS is automatically detected. Single-ended input for differential input is also supported. Refer to Chapter 9.3.3.3 Single-Ended Input for Differential Input .
IN6_POS IN6_NEG	42 43	I	PECL/LVDS	IN6_POS / IN6_NEG: Positive / Negative Input Clock 6 A 2 kHz, 4 kHz, N x 8 kHz ³ , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz or 622.08 MHz clock is differentially input on this pair of pins. Whether the clock signal is PECL or LVDS is automatically detected. Single-ended input for differential input is also supported. Refer to Chapter 9.3.3.3 Single-Ended Input for Differential Input .
IN7	48	I pull-down	CMOS	IN7: Input Clock 7 A 2 kHz, 4 kHz, N x 8 kHz ³ , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is input on this pin.
IN8	51	I pull-down	CMOS	IN8: Input Clock 8 A 2 kHz, 4 kHz, N x 8 kHz ³ , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is input on this pin.
IN9	52	I pull-down	CMOS	IN9: Input Clock 9 A 2 kHz, 4 kHz, N x 8 kHz ³ , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is input on this pin.
IN10	53	I pull-down	CMOS	IN10: Input Clock 10 A 2 kHz, 4 kHz, N x 8 kHz ³ , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is input on this pin.
IN11	54	I pull-down	CMOS	IN11: Input Clock 11 A 2 kHz, 4 kHz, N x 8 kHz ³ , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is input on this pin. In Slave operation, the frequency of the T0 selected input clock IN11 is recommended to be 6.48 MHz.
IN12	55	I pull-down	CMOS	IN12: Input Clock 12 A 2 kHz, 4 kHz, N x 8 kHz ³ , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is input on this pin.
IN13	56	I pull-down	CMOS	IN13: Input Clock 13 A 2 kHz, 4 kHz, N x 8 kHz ³ , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is input on this pin.
IN14	57	I pull-down	CMOS	IN14: Input Clock 14 A 2 kHz, 4 kHz, N x 8 kHz ³ , 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is input on this pin.
Output Frame Synchronization Signal				
FRSYNC_8K	30	O	CMOS	FRSYNC_8K: 8 kHz Frame Sync Output An 8 kHz signal is output on this pin.
MFRSYNC_2K	31	O	CMOS	MFRSYNC_2K: 2 kHz Multiframe Sync Output A 2 kHz signal is output on this pin.
Output Clock				
OUT1	88	O	CMOS	OUT1: Output Clock 1 A 1 Hz, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 ⁴ , N x T1 ⁵ , N x 13.0 MHz ⁶ , N x 3.84 MHz ⁷ , 5 MHz, 10 MHz, 20 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is output on this pin.

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description ¹
OUT2	89	O	CMOS	OUT2: Output Clock 2 A 1 Hz, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 ⁴ , N x T1 ⁵ , N x 13.0 MHz ⁶ , N x 3.84 MHz ⁷ , 5 MHz, 10 MHz, 20 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is output on this pin.
OUT3	90	O	CMOS	OUT3: Output Clock 3 A 1 Hz, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 ⁴ , N x T1 ⁵ , N x 13.0 MHz ⁶ , N x 3.84 MHz ⁷ , 5 MHz, 10 MHz, 20 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is output on this pin.
OUT4	93	O	CMOS	OUT4: Output Clock 4 A 1 Hz, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 ⁴ , N x T1 ⁵ , N x 13.0 MHz ⁶ , N x 3.84 MHz ⁷ , 5 MHz, 10 MHz, 20 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is output on this pin.
OUT5	94	O	CMOS	OUT5: Output Clock 5 A 1 Hz, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 ⁴ , N x T1 ⁵ , N x 13.0 MHz ⁶ , N x 3.84 MHz ⁷ , 5 MHz, 10 MHz, 20 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is output on this pin.
OUT6_POS OUT6_NEG	34 35	O	PECL/LVDS	OUT6_POS / OUT6_NEG: Positive / Negative Output Clock 6 A 1 Hz, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 ⁴ , N x T1 ⁵ , N x 13.0 MHz ⁶ , N x 3.84 MHz ⁷ , 5 MHz, 10 MHz, 20 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz or 622.08 MHz clock is differentially output on this pair of pins.
OUT7_POS OUT7_NEG	36 37	O	PECL/LVDS	OUT7_POS / OUT7_NEG: Positive / Negative Output Clock 7 A 1 Hz, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 ⁴ , N x T1 ⁵ , N x 13.0 MHz ⁶ , N x 3.84 MHz ⁷ , 5 MHz, 10 MHz, 20 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz or 622.08 MHz clock is differentially output on this pair of pins.
OUT8_POS OUT8_NEG	28 27	O	AMI	OUT8_POS / OUT8_NEG: Positive / Negative Output Clock 8 A 64 kHz + 8 kHz or 64 kHz + 8 kHz + 0.4 kHz composite clock is differentially output on this pair of pins.
OUT9	95	O	CMOS	OUT9: Output Clock 9 A 1.544 MHz (SONET) / 2.048 MHz (SDH) BITS/SSU clock is output on this pin.
Microprocessor Interface				
\overline{CS}	70	I pull-up	CMOS	\overline{CS}: Chip Selection A transition from high to low must occur on this pin for each read or write operation and this pin should remain low until the operation is over.
INT_REQ	8	O	CMOS	INT_REQ: Interrupt Request This pin is used as an interrupt request. The output characteristics are determined by the HZ_EN bit (b1, 0CH) and the INT_POL bit (b0, 0CH).
MPU_MODE0 MPU_MODE1 MPU_MODE2	60 59 58	I pull-down	CMOS	MPU_MODE[2:0]: Microprocessor Interface Mode Selection The device supports five microprocessor interface modes: EPROM, Multiplexed, Intel, Motorola and Serial. During reset, these pins determine the default value of the MPU_SEL_CNFG[2:0] bits (b2-0, 7FH) as follows: 001 (EPROM mode); 010 (Multiplexed mode); 011 (Intel mode); 100 (Motorola mode); 101 (Serial mode); 110 - 111 (Reserved). After reset, these pins are general purpose inputs. The microprocessor interface mode is selected by the MPU_SEL_CNFG[2:0] bits (b2-0, 7FH). The value of these pins is always reflected by the MPU_PIN_STS[2:0] bits (b2-0, 02H).

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description ¹
A0 / SDI	69	I pull-down	CMOS	A[6:0]: Address Bus In ERPOM, Intel and Motorola modes, these pins are the address bus of the microprocessor interface.
A1 / CLKE	68			
A2	67			
A3	66			
A4	65			
A5	64			
A6	63			
AD0 / SDO	83	I/O pull-down	CMOS	AD[7:0]: Address / Data Bus In EPROM, Intel and Motorola modes, these pins are the bi-directional data bus of the microprocessor interface. In Multiplexed mode, these pins are the bi-directional address/data bus of the microprocessor interface.
AD1	82			
AD2	81			
AD3	80			
AD4	79			
AD5	78			
AD6	77			
AD7	76			
\overline{WR}	71	I pull-up	CMOS	\overline{WR}: Write Operation In Multiplexed and Intel modes, this pin is asserted low to initiate a write operation. In Motorola mode, this pin is asserted low to initiate a write operation or asserted high to initiate a read operation. In EPROM and Serial modes, this pin should be connected to ground.
\overline{RD}	72	I pull-up	CMOS	\overline{RD}: Read Operation In Multiplexed and Intel modes, this pin is asserted low to initiate a read operation. In EPROM, Motorola and Serial modes, this pin should be connected to ground.
ALE / SCLK	73	I pull-down	CMOS	ALE: Address Latch Enable In Multiplexed mode, the address on AD[7:0] pins is sampled into the device on the falling edge of ALE. SCLK: Shift Clock In Serial mode, a shift clock is input on this pin. Data on SDI is sampled by the device on the rising edge of SCLK. Data on SDO is updated on the active edge of SCLK. The active edge is determined by the CLKE. In EPROM, Intel and Motorola modes, this pin should be connected to ground.

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description ¹
RDY	75	O	CMOS	RDY: Ready/Data Acknowledge In Multiplexed and Intel modes, a high level on this pin indicates that a read/write cycle is completed. A low level on this pin indicates that wait state must be inserted. In Motorola mode, a low level on this pin indicates that valid information on the data bus is ready for a read operation or acknowledges the acceptance of the written data during a write operation. In EPROM and Serial modes, this pin should be connected to ground.
JTAG (per IEEE 1149.1)				
$\overline{\text{TRST}}$	2	I pull-down	CMOS	$\overline{\text{TRST}}$: JTAG Test Reset (Active Low) A low signal on this pin resets the JTAG test port. This pin should be connected to ground when JTAG is not used.
TMS	7	I pull-up	CMOS	TMS: JTAG Test Mode Select The signal on this pin controls the JTAG test performance and is sampled on the rising edge of TCK.
TCK	9	I pull-down	CMOS	TCK: JTAG Test Clock The clock for the JTAG test is input on this pin. TDI and TMS are sampled on the rising edge of TCK and TDO is updated on the falling edge of TCK. If TCK is idle at a low level, all stored-state devices contained in the test logic will indefinitely retain their state.
TDI	23	I pull-up	CMOS	TDI: JTAG Test Data Input The test data is input on this pin. It is clocked into the device on the rising edge of TCK.
TDO	21	O	CMOS	TDO: JTAG Test Data Output The test data is output on this pin. It is clocked out of the device on the falling edge of TCK. TDO pin outputs a high impedance signal except during the process of data scanning. This pin can indicate the interrupt of T0 selected input clock fail, as determined by the LOS_FLAG_ON_TDO bit (b6, 0BH). Refer to Chapter 3.8.1 Input Clock Validity for details.
Power & Ground				
VDDD1	12	Power	-	VDDDn: 3.3 V Digital Power Supply Each VDDDn should be paralleled with ground through a 0.1 μ F capacitor.
VDDD2	16			
VDDD3	13			
VDDD4	50			
VDDD5	61			
VDDD6	85			
VDDD7	86			
VDDA1	6	Power	-	VDDAn: 3.3 V Analog Power Supply Each VDDAn should be paralleled with ground through a 0.1 μ F capacitor.
VDDA2	19			
VDDA3	91			
VDD_AMI	26	Power	-	VDD_AMI: 3.3 V Power Supply for AMI I/O
VDD_DIFF1	33	Power	-	VDD_DIFF1: 3.3 V Power Supply for OUT6
VDD_DIFF2	39	Power	-	VDD_DIFF2: 3.3 V Power Supply for OUT7

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description ¹
DGND1	11	Ground	-	DGNDn: Digital Ground
DGND2	15			
DGND3	14			
DGND4	49			
DGND5	62			
DGND6	84			
DGND7	87			
AGND1	5	Ground	-	AGNDn: Analog Ground
AGND2	20			
AGND3	92			
GND_DIFF1	32	Ground	-	GND_DIFF: Ground for OUT6
GND_DIFF2	38	Ground	-	GND_DIFF: Ground for OUT7
GND_AMI	29	Ground	-	GND_AMI: Ground for AMI I/O
AGND	1	Ground	-	AGND: Analog Ground
Others				
IC1	3	-	-	IC: Internal Connected Internal Use. These pins should be left open for normal operation.
IC2	4			
IC3	17			
IC4	22			
IC5	96			
IC6	97			
IC7	98			
NC	44	-	-	NC: Not Connected
Note:				
1. All the unused input pins should be connected to ground; the output of all the unused output pins are don't-care.				
2. The contents in the brackets indicate the position of the register bit/bits.				
3. N x 8 kHz: $1 \leq N \leq 19440$.				
4. N x E1: N = 1, 2, 3, 4, 6, 8, 12, 16, 24, 32, 48, 64.				
5. N x T1: N = 1, 2, 3, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96.				
6. N x 13.0 MHz: N = 1, 2, 4.				
7. N x 3.84 MHz: N = 1, 2, 4, 8, 16, 10, 20, 40.				

3 FUNCTIONAL DESCRIPTION

3.1 RESET

The reset operation resets all registers and state machines to their default value or status.

After power on, the device must be reset for normal operation.

For a complete reset, the $\overline{\text{RST}}$ pin must be asserted low for at least 50 μs . After the $\overline{\text{RST}}$ pin is pulled high, the device will still be in reset state for 500 ms (typical). If the $\overline{\text{RST}}$ pin is held low continuously, the device remains in reset state.

3.2 MASTER CLOCK

A nominal 12.8000 MHz clock, provided by a crystal oscillator, is input on the OSC1 pin. This clock is provided for the device as a master clock. The master clock is used as a reference clock for all the internal circuits. A better active edge of the master clock is selected by the OSC_EDGE bit to improve jitter and wander performance.

In fact, an offset from the nominal frequency may input on the OSC1 pin. This offset can be compensated by setting the NOMINAL_FREQ_VALUE[23:0] bits. The calibration range is within ± 741 ppm.

The performance of the master clock should meet GR-1244-CORE, GR-253-CORE, ITU-T G.812 and G.813 criteria.

Table 2: Related Bit / Register in Chapter 3.2

Bit	Register	Address (Hex)
NOMINAL_FREQ_VALUE[23:0]	NOMINAL_FREQ[23:16]_CNFG, NOMINAL_FREQ[15:8]_CNFG, NOMINAL_FREQ[7:0]_CNFG	06, 05, 04
OSC_EDGE	DIFFERENTIAL_IN_OUT_OSC1_CNFG	0A

3.3 INPUT CLOCKS & FRAME SYNC SIGNAL

Altogether 14 clocks and 1 frame sync signal are input to the device.

3.3.1 INPUT CLOCKS

The device provides 14 input clock ports.

According to the input port technology, the input ports support the following technologies:

- AMI
- PECL/LVDS
- CMOS

According to the input clock source, the following clock sources are supported:

- T1: Recovered clock from STM-N or OC-n
- T2: PDH network synchronization timing
- T3: External synchronization reference timing

IN1 and IN2 support the AMI input signal only and the clock source is from T3. The input clock is a 64 kHz + 8 kHz or 64 kHz + 8 kHz + 0.4 kHz composite clock. The 400HZ_SEL bit should be set to match the input frequency. Any input violation that does not meet the standard composite clock structure will induce an AMI violation. The AMI violation is indicated by the AMI1_VIOL¹ / AMI2_VIOL¹ bit. If the AMI1_VIOL² / AMI2_VIOL² bit is '1', the occurrence of an AMI violation will trigger an interrupt.

IN3, IN4 and IN7 ~ IN14 support CMOS input signal only and the clock sources can be from T1, T2 or T3.

IN5 and IN6 support PECL/LVDS input signal and automatically detect whether the signal is PECL or LVDS. The clock sources can be from T1, T2 or T3.

For SDH and SONET networks, the default frequency is different. SONET / SDH frequency selection is controlled by the IN_SONET_SDH bit. During reset, the default value of the IN_SONET_SDH bit is determined by the SONET/SDH pin: high for SONET and low for SDH. After reset, the input signal on the SONET/SDH pin takes no effect.

IDT82V3280 supports single-ended input for differential input. Refer to [Chapter 9.3.3.3 Single-Ended Input for Differential Input](#).

3.3.2 FRAME SYNC INPUT SIGNALS

A 2 kHz, 4 kHz or 8 kHz frame sync signal is input on the EX_SYNC1 pin. It is a CMOS input. The input frequency should match the setting in the SYNC_FREQ[1:0] bits.

The frame sync input signal is used for frame sync output signal synchronization. Refer to [Chapter 3.13.2 Frame SYNC Output Signals](#) for details.

Table 3: Related Bit / Register in Chapter 3.3

Bit	Register	Address (Hex)
400HZ_SEL	IN1_CNFG	14
	IN2_CNFG	15
AMI1_VIOL ¹	INTERRUPT3_STS	0F
AMI2_VIOL ¹		
AMI1_VIOL ²	INTERRUPTS3_ENABLE_CNFG	12
AMI2_VIOL ²		
IN_SONET_SDH	INPUT_MODE_CNFG	09
SYNC_FREQ[1:0]		

3.4 INPUT CLOCK PRE-DIVIDER

Each input clock is assigned an internal Pre-Divider. The Pre-Divider is used to divide the clock frequency down to the DPLL's required input frequency, which is no more than 38.88 MHz.

For IN1 and IN2, the DPLL required frequency is fixed to 8 kHz (i.e., the corresponding IN_FREQ[3:0] bits are '0000'). The 8 kHz clock is extracted from the composite clock and the Pre-Divider is bypassed automatically.

For IN3 ~ IN14, the DPLL required frequency is set by the corresponding IN_FREQ[3:0] bits.

Each Pre-Divider consists of a DivN Divider and a Lock 8k Divider. IN3 and IN4 also include an HF (High Frequency) Divider. Figure 3 shows a block diagram of the pre-dividers for an input clock.

When the Lock 8k Divider is used, the input clock is divided down to 8 kHz internally; the PRE_DIVN_VALUE [14:0] bits are not required. Lock 8k Divider can be used for 1.544 MHz, 2.048 MHz, 6.48 MHz, 19.44 MHz, 25.92 MHz or 38.88 MHz input clock frequency and the corresponding IN_FREQ[3:0] bits should be set to match the input frequency. For 2 kHz, 4 kHz or 8 kHz input clock frequency only, the Pre-Divider is bypassed and the corresponding IN_FREQ[3:0] bits should be set to match the input frequency. The input clock can be inverted, as determined by the IN_2K_4K_8K_INV bit.

The HF Divider, which is only available for IN5 and IN6, should be used when the input clock is higher than (>) 155.52 MHz. The input clock can be divided by 4, 5 or can bypass the HF Divider, as determined by the IN5_DIV[1:0]/IN6_DIV[1:0] bits correspondingly.

Either the DivN Divider or the Lock 8k Divider can be used or both can be bypassed, as determined by the DIRECT_DIV bit and the LOCK_8K bit.

When the DivN Divider is used for INn ($3 \leq n \leq 14$), the division factor setting should observe the following order:

1. Select an input clock by the PRE_DIV_CH_VALUE[3:0] bits;
2. Write the lower eight bits of the division factor to the PRE_DIVN_VALUE[7:0] bits;
3. Write the higher eight bits of the division factor to the PRE_DIVN_VALUE[14:8] bits.

Once the division factor is set for the input clock selected by the PRE_DIV_CH_VALUE[3:0] bits, it is valid until a different division factor is set for the same input clock. The division factor is calculated as follows:

$$\text{Division Factor} = (\text{the frequency of the clock input to the DivN Divider} \div \text{the frequency of the DPLL required clock set by the IN_FREQ[3:0] bits}) - 1$$

The DivN Divider can only divide the input clock whose frequency is lower than (<) 155.52 MHz.

The Pre-Divider configuration and the division factor setting depend on the input clock on one of the IN3 ~ IN14 pins and the DPLL required clock. Here is an example:

The input clock on the IN6 pin is 622.08 MHz; the DPLL required clock is 6.48 MHz by programming the IN_FREQ[3:0] bits of register IN6 to '0010'. Do the following step by step to divide the input clock:

1. Use the HF Divider to divide the clock down to 155.52 MHz:
 $622.08 \div 155.52 = 4$, so set the IN6_DIV[1:0] bits to '01';
2. Use the DivN Divider to divide the clock down to 6.48 MHz:
 Set the PRE_DIV_CH_VALUE[3:0] bits to '0110';
 Set the DIRECT_DIV bit in Register IN6_CNFG to '1' and the LOCK_8K bit in Register IN6_CNFG to '0';
 $155.52 \div 6.48 = 24$; $24 - 1 = 23$, so set the PRE_DIVN_VALUE[14:0] bits to '10111'.

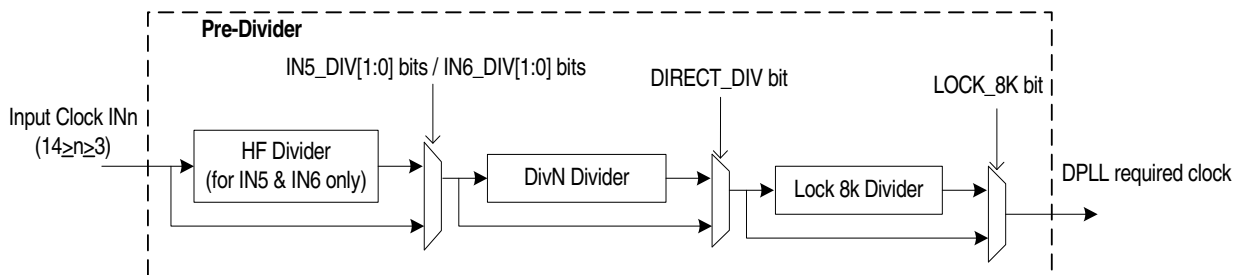


Figure 3. Pre-Divider for An Input Clock

Table 4: Related Bit / Register in Chapter 3.4

Bit	Register	Address (Hex)
IN5_DIV[1:0]	IN5_IN6_HF_DIV_CNFG	18
IN6_DIV[1:0]		
IN_FREQ[3:0]	IN1_CNFG ~ IN14_CNFG	14 ~ 17, 19 ~ 22
IN_2K_4K_8K_INV	FR_MFR_SYNC_CNFG	74
DIRECT_DIV	IN3_CNFG ~ IN14_CNFG	16, 17, 19 ~ 22
LOCK_8K		
PRE_DIV_CH_VALUE[3:0]	PRE_DIV_CH_CNFG	23
PRE_DIVN_VALUE[14:0]	PRE_DIVN[14:8]_CNFG, PRE_DIVN[7:0]_CNFG	25, 24

3.5 INPUT CLOCK QUALITY MONITORING

The qualities of all the input clocks are always monitored in the following aspects:

- LOS (loss of signal) (only for IN1 and IN2)
- Activity
- Frequency

LOS monitoring is only conducted on IN1 and IN2. Activity and frequency monitoring are conducted on all the input clocks.

The qualified clocks are available for T0/T4 DPLL selection. The T0 and T4 selected input clocks have to be monitored further. Refer to [Chapter 3.7 Selected Input Clock Monitoring](#) for details.

3.5.1 LOS MONITORING

IN1 and IN2 support the AMI input signal. LOS monitoring is conducted on IN1 and IN2. A LOS event occurs when the amplitude of the input clock falls below +0.6 Vp-p for 1 ms; the LOS event is cleared when the amplitude rises higher than +1 Vp-p.

LOS status is indicated by the AMI1_LOS¹ / AMI2_LOS¹ bit. If the AMI1_LOS² / AMI2_LOS² bit is '1', the occurrence of LOS will trigger an interrupt.

The input clock in LOS status is disqualified for clock selection for T0/T4 DPLL.

3.5.2 ACTIVITY MONITORING

Activity is monitored by using an internal leaky bucket accumulator, as shown in [Figure 4](#).

Each input clock is assigned an internal leaky bucket accumulator. The input clock is monitored for each period of 128 ms and the internal leaky bucket accumulator increases by 1 when an event is detected; it decreases by 1 if no event is detected within the period set by the decay rate. The event is that an input clock drifts outside (>) ±500 ppm with respect to the master clock within a 128 ms period.

There are four configurations (0 - 3) for a leaky bucket accumulator. The leaky bucket configuration for an input clock is selected by the corresponding BUCKET_SEL[1:0] bits. Each leaky bucket configuration consists of four elements: upper threshold, lower threshold, bucket size and decay rate.

The bucket size is the capability of the accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected. The upper threshold is a point above which a no-activity alarm is raised. The lower threshold is a point below which the no-activity alarm is cleared. The decay rate is a certain period during which the accumulator decreases by 1 if no event is detected.

The leaky bucket configuration is programmed by one of four groups of register bits: the BUCKET_SIZE_n_DATA[7:0] bits, the UPPER_THRESHOLD_n_DATA[7:0] bits, the LOWER_THRESHOLD_n_DATA[7:0] bits and the DECAY_RATE_n_DATA[1:0] bits respectively; 'n' is 0 ~ 3.

The no-activity alarm status of the input clock is indicated by the INn_NO_ACTIVITY_ALARM bit (14 ≥ n ≥ 1).

The input clock with a no-activity alarm is disqualified for clock selection for T0/T4 DPLL.

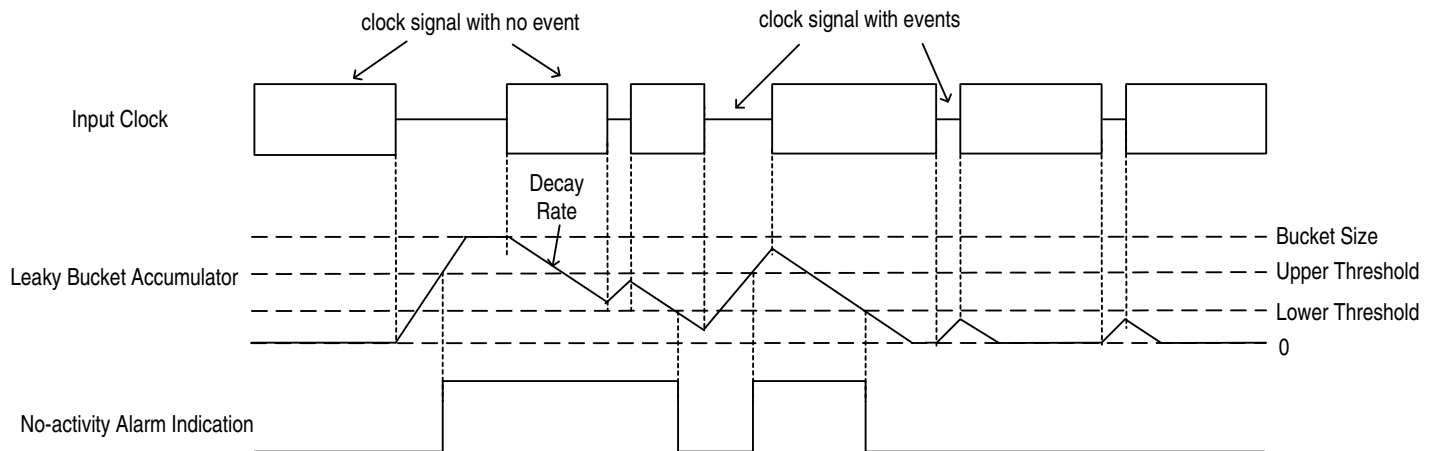


Figure 4. Input Clock Activity Monitoring

3.5.3 FREQUENCY MONITORING

Frequency is monitored by comparing the input clock with a reference clock. The reference clock can be derived from the master clock or the output of T0 DPLL, as determined by the `FREQ_MON_CLK` bit.

A frequency hard alarm threshold is set for frequency monitoring. If the `FREQ_MON_HARD_EN` bit is '1', a frequency hard alarm is raised when the frequency of the input clock with respect to the reference clock is above the threshold; the alarm is cleared when the frequency is below the threshold.

The frequency hard alarm threshold can be calculated as follows:

$$\text{Frequency Hard Alarm Threshold (ppm)} = (\text{ALL_FREQ_HARD_THRESHOLD}[3:0] + 1) \times \text{FREQ_MON_FACTOR}[3:0]$$

If the `FREQ_MON_HARD_EN` bit is '1', the frequency hard alarm status of the input clock is indicated by the `INn_FREQ_HARD_ALARM` bit ($14 \geq n \geq 1$). When the `FREQ_MON_HARD_EN` bit is '0', no frequency hard alarm is raised even if the input clock is above the frequency hard alarm threshold.

The input clock with a frequency hard alarm is disqualified for clock selection for T0/T4 DPLL.

In addition, if the input clock is 2 kHz, 4 kHz or 8 kHz, its clock edges with respect to the reference clock are monitored. If any edge drifts outside $\pm 5\%$, the input clock is disqualified for clock selection for T0/T4 DPLL. The input clock is qualified if any edge drifts inside $\pm 5\%$. This function is supported only when the `IN_NOISE_WINDOW` bit is '1'.

The frequency of each input clock with respect to the reference clock can be read by doing the following step by step:

1. Select an input clock by setting the `IN_FREQ_READ_CH[3:0]` bits;
2. Read the value in the `IN_FREQ_VALUE[7:0]` bits and calculate as follows:

$$\text{Input Clock Frequency (ppm)} = \text{IN_FREQ_VALUE}[7:0] \times \text{FREQ_MON_FACTOR}[3:0]$$

Note that the value set by the `FREQ_MON_FACTOR[3:0]` bits depends on the application.

Table 5: Related Bit / Register in Chapter 3.5

Bit	Register	Address (Hex)
<code>AMI1_LOS</code> ¹	INTERRUPTS3_STS	0F
<code>AMI2_LOS</code> ¹		
<code>AMI1_LOS</code> ²	INTERRUPTS3_ENABLE_CNFG	12
<code>AMI2_LOS</code> ²		
<code>BUCKET_SIZE_n_DATA[7:0]</code> ($3 \geq n \geq 0$)	<code>BUCKET_SIZE_0_CNFG</code> ~ <code>BUCKET_SIZE_3_CNFG</code>	33, 37, 3B, 3F
<code>UPPER_THRESHOLD_n_DATA[7:0]</code> ($3 \geq n \geq 0$)	<code>UPPER_THRESHOLD_0_CNFG</code> ~ <code>UPPER_THRESHOLD_3_CNFG</code>	31, 35, 39, 3D
<code>LOWER_THRESHOLD_n_DATA[7:0]</code> ($3 \geq n \geq 0$)	<code>LOWER_THRESHOLD_0_CNFG</code> ~ <code>LOWER_THRESHOLD_3_CNFG</code>	32, 36, 3A, 3E
<code>DECAY_RATE_n_DATA[1:0]</code> ($3 \geq n \geq 0$)	<code>DECAY_RATE_0_CNFG</code> ~ <code>DECAY_RATE_3_CNFG</code>	34, 38, 3C, 40
<code>BUCKET_SEL[1:0]</code>	<code>IN1_CNFG</code> ~ <code>IN14_CNFG</code>	14 ~ 17, 19 ~ 22
<code>INn_NO_ACTIVITY_ALARM</code> ($14 \geq n \geq 1$)	<code>IN1_IN2_STS</code> ~ <code>IN13_IN14_STS</code>	43 ~ 49
<code>INn_FREQ_HARD_ALARM</code> ($14 \geq n \geq 1$)		
<code>FREQ_MON_CLK</code>	MON_SW_PBO_CNFG	0B
<code>FREQ_MON_HARD_EN</code>		
<code>ALL_FREQ_HARD_THRESHOLD[3:0]</code>	ALL_FREQ_MON_THRESHOLD_CNFG	2F
<code>FREQ_MON_FACTOR[3:0]</code>	FREQ_MON_FACTOR_CNFG	2E
<code>IN_NOISE_WINDOW</code>	PHASE_MON_PBO_CNFG	78
<code>IN_FREQ_READ_CH[3:0]</code>	IN_FREQ_READ_CH_CNFG	41
<code>IN_FREQ_VALUE[7:0]</code>	IN_FREQ_READ_STS	42

3.6 T0 / T4 DPLL INPUT CLOCK SELECTION

An input clock is selected for T0 DPLL and for T4 DPLL respectively.

For T0 path, the EXT_SW bit and the T0_INPUT_SEL[3:0] bits determine the input clock selection, as shown in [Table 6](#):

Table 6: Input Clock Selection for T0 Path

Control Bits		Input Clock Selection
EXT_SW	T0_INPUT_SEL[3:0]	
1	don't-care	External Fast selection
0	other than 0000	Forced selection
	0000	Automatic selection

For T4 path, the T4 DPLL may lock to a T0 DPLL output or lock independently from T0 path, as determined by the T4_LOCK_T0 bit. When the T4 DPLL locks to the T0 DPLL output, the T4 selected input clock is a 77.76 MHz or 8 kHz signal from the T0 DPLL 77.76 MHz path (refer to [Chapter 3.11.5.1 T0 Path](#)), as determined by the T0_FOR_T4 bit. When the T4 path locks independently from the T0 path, the T4 DPLL input clock selection is determined by the T4_INPUT_SEL[3:0] bits. Refer to [Table 7](#):

Table 7: Input Clock Selection for T4 Path

Control Bits - T4_INPUT_SEL[3:0]	Input Clock Selection
other than 0000	Forced selection
0000	Automatic selection

External Fast selection is done between IN3/IN5 and IN4/IN6 pairs.

Forced selection is done by setting the related registers.

Table 8: External Fast Selection

Control Pin & Bits			the Selected Input Clock
FF_SRCSW (after reset)	IN3_SEL_PRIORITY[3:0]	IN4_SEL_PRIORITY[3:0]	
high	0000	don't-care	IN5
	other than 0000		IN3
low	don't-care	0000	IN6
		other than 0000	IN4

Automatic selection is done based on the results of input clocks quality monitoring and the related registers configuration.

The selected input clock is attempted to be locked in T0/T4 DPLL.

3.6.1 EXTERNAL FAST SELECTION (T0 ONLY)

The External Fast selection is supported by T0 path only. In External Fast selection, only IN3/IN5 and IN4/IN6 pairs are available for selection. Refer to [Figure 5](#). The results of input clocks quality monitoring (refer to [Chapter 3.5 Input Clock Quality Monitoring](#)) do not affect input clock selection.

The T0 input clock selection is determined by the FF_SRCSW pin after reset (this pin determines the default value of the EXT_SW bit during reset, refer to [Chapter 2 Pin Description](#)), the IN3_SEL_PRIORITY[3:0] bits and the IN4_SEL_PRIORITY[3:0] bits, as shown in [Figure 5](#) and [Table 8](#):

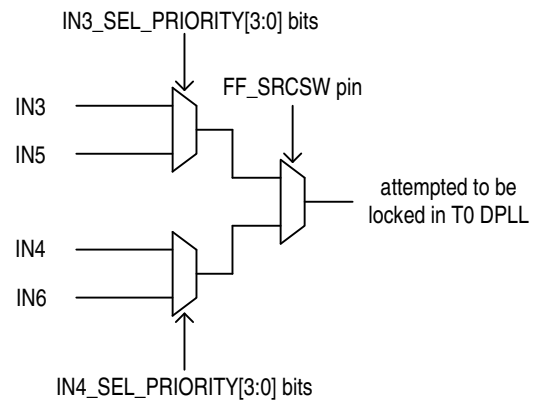


Figure 5. External Fast Selection