Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

WAN PLL

IDT82V3285A

Version -
August 7, 2009

6024 Silver Creek Valley Road, San Jose, CA 95138
Telephone: (800) 345-7015 • TWX: 910-338-2070 • FAX: (408) 284-2775

Printed in U.S.A.

Table of Contents

List of Tables

List of Figures

FEATURES

HIGHLIGHTS

- The first single PLL chip:
  - Features 0.5 mHz to 560 Hz bandwidth
  - Exceeds GR-253-CORE (OC-12) and ITU-T G.813 (STM-16/ Option I) jitter generation requirements
  - Provides node clocks for Cellular and WLL base-station (GSM and 3G networks)
  - Provides clocks for DSL access concentrators (DSLAM), especially for Japan TCM-ISDN network timing based ADSL equipments

MAIN FEATURES

- Provides an integrated single-chip solution for Synchronous Equipment Timing Source, including Stratum 2, 3E, 3, SMC, 4E and 4 clocks
- Employs DPLL and APLL to feature excellent jitter performance and minimize the number of the external components
- Integrates T0 DPLL and T4 DPLL; T4 DPLL locks independently or locks to T0 DPLL
- Supports Forced or Automatic operating mode switch controlled by an internal state machine; the primary operating modes are Free-Run, Locked and Holdover
- Supports programmable DPLL bandwidth (0.5 mHz to 560 Hz in 19 steps) and damping factor (1.2 to 20 in 5 steps)
- Supports $1.1X10^{-5}$ ppm absolute holdover accuracy and $4.4X10^{-8}$ ppm instantaneous holdover accuracy
- Supports PBO to minimize phase transients on T0 DPLL output to be no more than 0.61 ns
- Supports phase absorption when phase-time changes on T0 selected input clock are greater than a programmable limit over an interval of less than 0.1 seconds
- Supports programmable input-to-output phase offset adjustment
- Limits the phase and frequency offset of the outputs
- Supports manual and automatic selected input clock switch
- Supports automatic hitless selected input clock switch on clock failure
- Supports three types of input clock sources: recovered clock from STM-N or OC-n, PDH network synchronization timing and external synchronization reference timing
- Provides a 2 kHz, 4 kHz or 8 kHz frame sync input signal, and a 2 kHz and an 8 kHz frame sync output signals
- Provides 5 input clocks whose frequency cover from 2 kHz to 622.08 MHz
- Provides 5 output clocks whose frequency cover from 1 Hz to 622.08 MHz
- Provides output clocks for BITS, GPS, 3G, GSM, etc.
- Supports PECL/LVDS and CMOS input/output technologies
- Supports master clock calibration
- Supports Master/Slave application (two chips used together) to enable system protection against single chip failure
- Meets Telcordia GR-1244-CORE, GR-253-CORE, GR-1377-CORE, ITU-T G.812, ITU-T G.813 and ITU-T G.783 criteria

OTHER FEATURES

- Multiple microprocessor interface modes: EPROM, Multiplexed, Intel, Motorola and Serial
- IEEE 1149.1 JTAG Boundary Scan
- Single 3.3 V operation with 5 V tolerant CMOS I/Os
- 100-pin TQFP package, Green package options available

APPLICATIONS

- BITS / SSU
- SMC / SEC (SONET / SDH)
- DWDM cross-connect and transmission equipments
- Central Office Timing Source and Distribution
- Core and access IP switches / routers
- Gigabit and Terabit IP switches / routers
- IP and ATM core switches and access equipments
- Cellular and WLL base-station node clocks
- Broadband and multi-service access equipments
- Any other telecom equipments that need synchronous equipment system timing

DESCRIPTION

The IDT82V3285A is an integrated, single-chip solution for the Synchronous Equipment Timing Source for Stratum 2, 3E, 3, SMC, 4E and 4 clocks in SONET / SDH equipments, DWDM and Wireless base station, such as GSM, 3G, DSL concentrator, Router and Access Network applications.

The device supports three types of input clock sources: recovered clock from STM-N or OC-n, PDH network synchronization timing and external synchronization reference timing.

Based on ITU-T G.783 and Telcordia GR-253-CORE, the device consists of T0 and T4 paths. The T0 path is a high quality and highly configurable path to provide system clock for node timing synchronization within a SONET / SDH network. The T4 path is simpler and less configurable for equipment synchronization. The T4 path locks independently from the T0 path or locks to the T0 path.

An input clock is automatically or manually selected for T0 and T4 each for DPLL locking. Both the T0 and T4 paths support three primary operating modes: Free-Run, Locked and Holdover. In Free-Run mode, the DPLL refers to the master clock. In Locked mode, the DPLL locks to the selected input clock. In Holdover mode, the DPLL resorts to the frequency data acquired in Locked mode. Whatever the operating mode is, the DPLL gives a stable performance without being affected by operating conditions or silicon process variations.

If the DPLL outputs are processed by T0/T4 APLL, the outputs of the device will be in a better jitter/wander performance.

The device provides programmable DPLL bandwidths: 0.5 mHz to 560 Hz in 19 steps and damping factors: 1.2 to 20 in 5 steps. Different settings cover all SONET / SDH clock synchronization requirements.

A high stable input is required for the master clock in different applications. The master clock is used as a reference clock for all the internal circuits in the device. It can be calibrated within ±741 ppm.

All the read/write registers are accessed through a microprocessor interface. The device supports five microprocessor interface modes: EPROM, Multiplexed, Intel, Motorola and Serial.

In general, the device can be used in Master/Slave application. In this application, two devices should be used together to enable system protection against single chip failure. See Chapter 4 Typical Application for details.

FUNCTIONAL BLOCK DIAGRAM

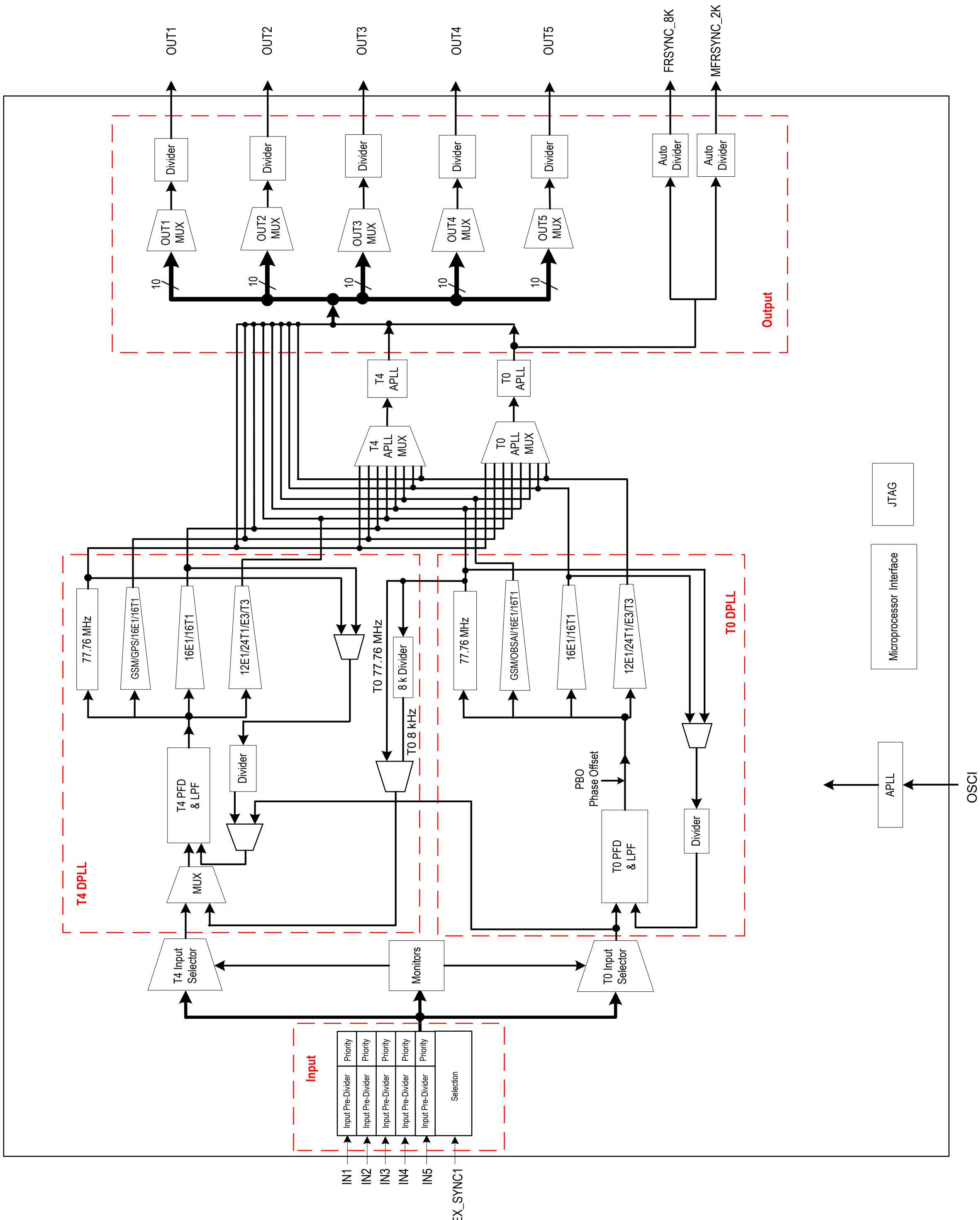

Figure 1. Functional Block Diagram

1 PIN ASSIGNMENT

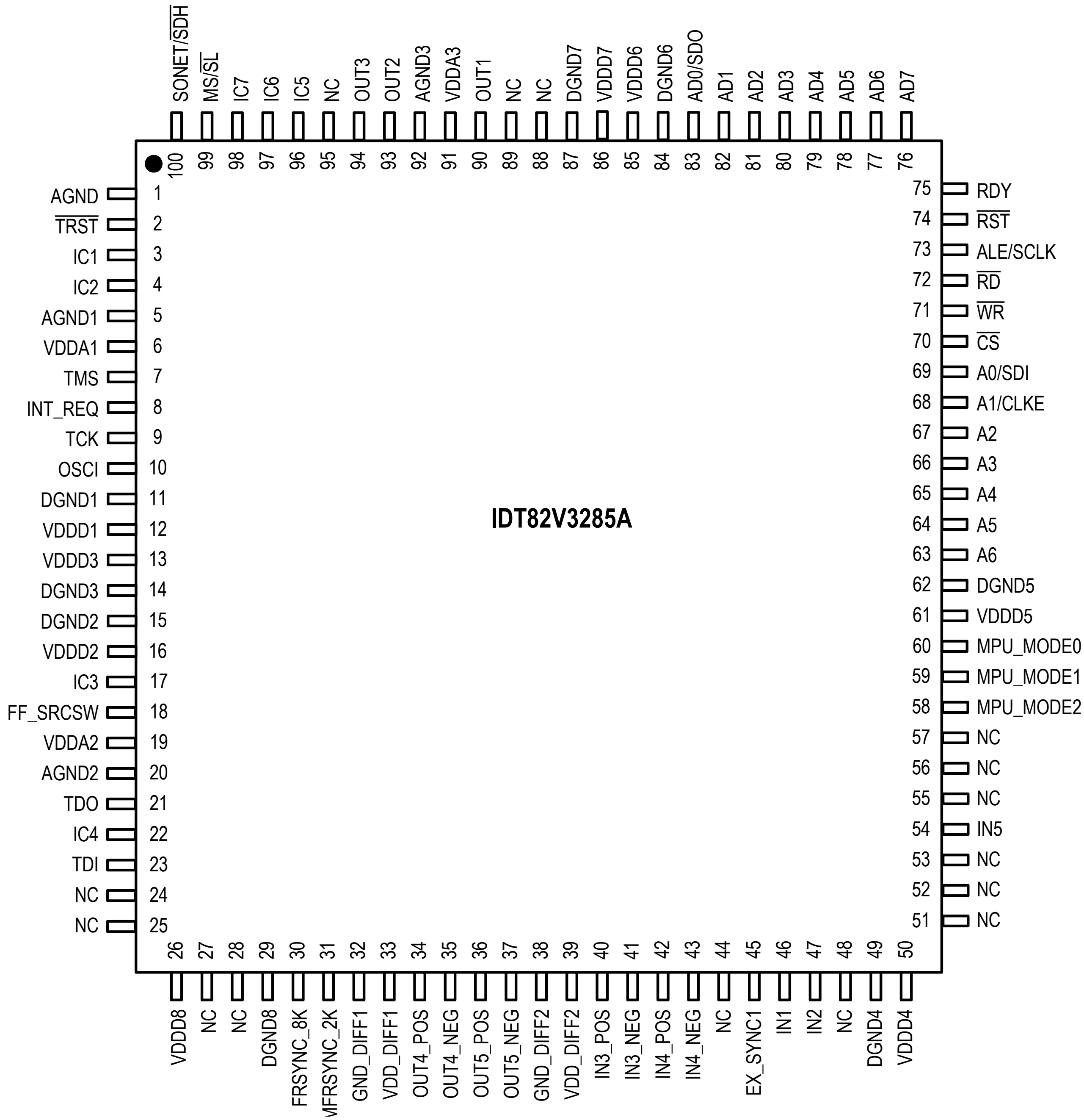

Figure 2. Pin Assignment (Top View)

2 PIN DESCRIPTION

Table 1: Pin Description

Name	Pin No.	I/O	Type	Description [1]
Global Control Signal				
OSCI	10	I	CMOS	**OSCI: Crystal Oscillator Master Clock** A nominal 12.8000 MHz clock provided by a crystal oscillator is input on this pin. It is the master clock for the device.
FF_SRCSW	18	I pull-down	CMOS	**FF_SRCSW: External Fast Selection Enable** During reset, this pin determines the default value of the EXT_SW bit (b4, 0BH) [2]. The EXT_SW bit determines whether the External Fast Selection is enabled. High: The default value of the EXT_SW bit (b4, 0BH) is ‘1’ (External Fast selection is enabled); Low: The default value of the EXT_SW bit (b4, 0BH) is ‘0’ (External Fast selection is disabled). After reset, this pin selects an input clock pair for the T0 DPLL if the External Fast selection is enabled: High: Pair IN1 / IN3 is selected. Low: Pair IN2/ IN4 is selected. After reset, the input on this pin takes no effect if the External Fast selection is disabled.
MS/$\overline{\text{SL}}$	99	I pull-up	CMOS	**MS/$\overline{\text{SL}}$: Master / Slave Selection** This pin, together with the MS_SL_CTRL bit (b0, 13H), controls whether the device is configured as the Master or as the Slave. Refer to Chapter 3.14 Master / Slave Configuration for details. The signal level on this pin is reflected by the MASTER_SLAVE bit (b1, 09H).
SONET/$\overline{\text{SDH}}$	100	I pull-down	CMOS	**SONET/$\overline{\text{SDH}}$: SONET / SDH Frequency Selection** During reset, this pin determines the default value of the IN_SONET_SDH bit (b2, 09H): High: The default value of the IN_SONET_SDH bit is ‘1’ (SONET); Low: The default value of the IN_SONET_SDH bit is ‘0’ (SDH). After reset, the value on this pin takes no effect.
$\overline{\text{RST}}$	74	I pull-up	CMOS	**$\overline{\text{RST}}$: Reset** A low pulse of at least 50 μs on this pin resets the device. After this pin is high, the device will still be held in reset state for 500 ms (typical).
Frame Synchronization Input Signal				
EX_SYNC1	45	I pull-down	CMOS	**EX_SYNC1: External Sync Input 1** A 2 kHz, 4 kHz or 8 kHz signal is input on this pin.
Input Clock				
IN1	46	I pull-down	CMOS	**IN1: Input Clock 1** A 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is input on this pin.
IN2	47	I pull-down	CMOS	**IN2: Input Clock 2** A 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is input on this pin.
IN3_POS IN3_NEG	40 41	I	PECL/LVDS	**IN3_POS / IN3_NEG: Positive / Negative Input Clock 3** A 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz or 622.08 MHz clock is differentially input on this pair of pins. Whether the clock signal is PECL or LVDS is automatically detected. Single-ended input for differential input is also supported. Refer to Chapter 9.3.2.3 Single-Ended Input for Differential Input.

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description [1]
IN4_POS IN4_NEG	42 43	I	PECL/LVDS	**IN4_POS / IN4_NEG: Positive / Negative Input Clock 4** A 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz or 622.08 MHz clock is differentially input on this pair of pins. Whether the clock signal is PECL or LVDS is automatically detected. Single-ended input for differential input is also supported. Refer to Chapter 9.3.2.3 Single-Ended Input for Differential Input.
IN5	54	I pull-down	CMOS	**IN5: Input Clock 5** A 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is input on this pin. In Slave operation, the frequency of the T0 selected input clock IN5 is recommended to be 6.48 MHz.
Output Frame Synchronization Signal				
FRSYNC_8K	30	O	CMOS	**FRSYNC_8K: 8 kHz Frame Sync Output** An 8 kHz signal is output on this pin.
MFRSYNC_2K	31	O	CMOS	**MFRSYNC_2K: 2 kHz Multiframe Sync Output** A 2 kHz signal is output on this pin.
Output Clock				
OUT1	90	O	CMOS	**OUT1: Output Clock 1** A 1 Hz, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 [4], N x T1 [5], N x 13.0 MHz [6], N x 3.84 MHz [7], 5 MHz, 10 MHz, 20 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is output on this pin.
OUT2	93	O	CMOS	**OUT2: Output Clock 2** A 1 Hz, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 [4], N x T1 [5], N x 13.0 MHz [6], N x 3.84 MHz [7], 5 MHz, 10 MHz, 20 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is output on this pin.
OUT3	94	O	CMOS	**OUT3: Output Clock 3** A 1 Hz, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 [4], N x T1 [5], N x 13.0 MHz [6], N x 3.84 MHz [7], 5 MHz, 10 MHz, 20 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is output on this pin.
OUT4_POS OUT4_NEG	34 35	O	PECL/LVDS	**OUT4_POS / OUT4_NEG: Positive / Negative Output Clock 4** A 1 Hz, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 [4], N x T1 [5], N x 13.0 MHz [6], N x 3.84 MHz [7], 5 MHz, 10 MHz, 20 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz or 622.08 MHz clock is differentially output on this pair of pins.
OUT5_POS OUT5_NEG	36 37	O	PECL/LVDS	**OUT5_POS / OUT5_NEG: Positive / Negative Output Clock 5** A 1 Hz, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 [4], N x T1 [5], N x 13.0 MHz [6], N x 3.84 MHz [7], 5 MHz, 10 MHz, 20 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz or 622.08 MHz clock is differentially output on this pair of pins.
Microprocessor Interface				
$\overline{CS}$	70	I pull-up	CMOS	**$\overline{CS}$: Chip Selection** A transition from high to low must occur on this pin for each read or write operation and this pin should remain low until the operation is over.
INT_REQ	8	O	CMOS	**INT_REQ: Interrupt Request** This pin is used as an interrupt request. The output characteristics are determined by the HZ_EN bit (b1, 0CH) and the INT_POL bit (b0, 0CH).

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description [1]
MPU_MODE0 MPU_MODE1 MPU_MODE2	60 59 58	I pull-down	CMOS	**MPU_MODE[2:0]: Microprocessor Interface Mode Selection** The device supports five microprocessor interface modes: EPROM, Multiplexed, Intel, Motorola and Serial. During reset, these pins determine the default value of the MPU_SEL_CNFG[2:0] bits (b2~0, 7FH) as follows: 001 (EPROM mode); 010 (Multiplexed mode); 011 (Intel mode); 100 (Motorola mode); 101 (Serial mode); 110 - 111 (Reserved). After reset, these pins are general purpose inputs. The microprocessor interface mode is selected by the MPU_SEL_CNFG[2:0] bits (b2~0, 7FH). The value of these pins is always reflected by the MPU_PIN_STS[2:0] bits (b2~0, 02H).
A0 / SDI A1 / CLKE A2 A3 A4 A5 A6	69 68 67 66 65 64 63	I pull-down	CMOS	**A[6:0]: Address Bus** In ERPOM, Intel and Motorola modes, these pins are the address bus of the microprocessor interface. **SDI: Serial Data Input** In Serial mode, this pin is used as the serial data input. Address and data on this pin are serially clocked into the device on the rising edge of SCLK. **CLKE: SCLK Active Edge Selection** In Serial mode, this pin selects the active edge of SCLK to update the SDO: High - The falling edge; Low - The rising edge. In Multiplexed mode, A0/SDI, A1/CLKE and A[6:2] pins should be connected to ground. In Serial mode, A[6:2] pins should be connected to ground.
AD0 / SDO AD1 AD2 AD3 AD4 AD5 AD6 AD7	83 82 81 80 79 78 77 76	I/O pull-down	CMOS	**AD[7:0]: Address / Data Bus** In EPROM, Intel and Motorola modes, these pins are the bi-directional data bus of the microprocessor interface. In Multiplexed mode, these pins are the bi-directional address/data bus of the microprocessor interface. **SDO: Serial Data Output** In Serial mode, this pin is used as the serial data output. Data on this pin is serially clocked out of the device on the active edge of SCLK. In Serial mode, AD[7:1] pins should be connected to ground.
$\overline{WR}$	71	I pull-up	CMOS	**$\overline{WR}$: Write Operation** In Multiplexed and Intel modes, this pin is asserted low to initiate a write operation. In Motorola mode, this pin is asserted low to initiate a write operation or s asserted high to initiate a read operation. In EPROM and Serial modes, this pin should be connected to ground.
$\overline{RD}$	72	I pull-up	CMOS	**$\overline{RD}$: Read Operation** In Multiplexed and Intel modes, this pin is asserted low to initiate a read operation. In EPROM, Motorola and Serial modes, this pin should be connected to ground.

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description [1]
ALE / SCLK	73	I pull-down	CMOS	**ALE: Address Latch Enable** In Multiplexed mode, the address on AD[7:0] pins is sampled into the device on the falling edge of ALE. **SCLK: Shift Clock** In Serial mode, a shift clock is input on this pin. Data on SDI is sampled by the device on the rising edge of SCLK. Data on SDO is updated on the active edge of SCLK. The active edge is determined by the CLKE. In EPROM, Intel and Motorola modes, this pin should be connected to ground.
RDY	75	O	CMOS	**RDY: Ready/Data Acknowledge** In Multiplexed and Intel modes, a high level on this pin indicates that a read/write cycle is completed. A low level on this pin indicates that wait state must be inserted. In Motorola mode, a low level on this pin indicates that valid information on the data bus is ready for a read operation or acknowledges the acceptance of the written data during a write operation. In EPROM and Serial modes, this pin should be connected to ground.
JTAG (per IEEE 1149.1)				
$\overline{TRST}$	2	I pull-down	CMOS	**$\overline{TRST}$: JTAG Test Reset (Active Low)** A low signal on this pin resets the JTAG test port. This pin should be connected to ground when JTAG is not used.
TMS	7	I pull-up	CMOS	**TMS: JTAG Test Mode Select** The signal on this pin controls the JTAG test performance and is sampled on the rising edge of TCK.
TCK	9	I pull-down	CMOS	**TCK: JTAG Test Clock** The clock for the JTAG test is input on this pin. TDI and TMS are sampled on the rising edge of TCK and TDO is updated on the falling edge of TCK. If TCK is idle at a low level, all stored-state devices contained in the test logic will indefinitely retain their state.
TDI	23	I pull-up	CMOS	**TDI: JTAG Test Data Input** The test data is input on this pin. It is clocked into the device on the rising edge of TCK.
TDO	21	O	CMOS	**TDO: JTAG Test Data Output** The test data is output on this pin. It is clocked out of the device on the falling edge of TCK. TDO pin outputs a high impedance signal except during the process of data scanning. This pin can indicate the interrupt of T0 selected input clock fail, as determined by the LOS_FLAG_ON_TDO bit (b6, 0BH). Refer to Chapter 3.8.1 Input Clock Validity for details.
Power & Ground				
VDDD1 VDDD2 VDDD3 VDDD4 VDDD5 VDDD6 VDDD7	12 16 13 50 61 85 86	Power	-	**VDDDn: 3.3 V Digital Power Supply** VDDDn connections should be connected using the recommended decoupling scheme shown in Figure 16.

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description [1]
VDDA1 VDDA2 VDDA3	6 19 91	Power	-	**VDDAn: 3.3 V Analog Power Supply** VDDAn connections should be connected using the recommended decoupling scheme shown in Figure 16.
VDDD8	26	Power	-	**VDDD8: 3.3 V Digital Power Supply**
VDD_DIFF1	33	Power	-	**VDD_DIFF1: 3.3 V Power Supply for OUT4**
VDD_DIFF2	39	Power	-	**VDD_DIFF2: 3.3 V Power Supply for OUT5**
DGND1 DGND2 DGND3 DGND4 DGND5 DGND6 DGND7	11 15 14 49 62 84 87	Ground	-	**DGNDn: Digital Ground**
AGND1 AGND2 AGND3	5 20 92	Ground	-	**AGNDn: Analog Ground**
GND_DIFF1	32	Ground	-	**GND_DIFF: Ground for OUT4**
GND_DIFF2	38	Ground	-	**GND_DIFF: Ground for OUT5**
DGND8	29	Ground	-	**DGND8: Digital Ground**
AGND	1	Ground	-	**AGND: Analog Ground**
Others				
IC1 IC2 IC3 IC4 IC5 IC6 IC7	3 4 17 22 96 97 98	-	-	**IC: Internally Connected** Internal Use. These pins should be left open for normal operation.
NC	24, 25, 27, 28, 44, 48, 51, 52, 53, 55, 56, 57, 88, 89, 95	-	-	**NC: Not Connected**

Note:
1. All the unused input pins should be connected to ground; the output of all the unused output pins are don't-care.
2. The contents in the brackets indicate the position of the register bit/bits.
3. N x 8 kHz: $1 \le N \le 19440$.
4. N x E1: N = 1, 2, 3, 4, 6, 8, 12, 16, 24, 32, 48, 64.
5. N x T1: N = 1, 2, 3, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96.
6. N x 13.0 MHz: N = 1, 2, 4.
7. N x 3.84 MHz: N = 1, 2, 4, 8, 16, 10, 20, 40.

3 FUNCTIONAL DESCRIPTION

3.1 RESET

The reset operation resets all registers and state machines to their default value or status.

After power on, the device must be reset for normal operation.

For a complete reset, the $\overline{RST}$ pin must be asserted low for at least 50 µs. After the $\overline{RST}$ pin is pulled high, the device will still be in reset state for 500 ms (typical). If the $\overline{RST}$ pin is held low continuously, the device remains in reset state.

3.2 MASTER CLOCK

A nominal 12.8000 MHz clock, provided by a crystal oscillator, is input on the OSCI pin. This clock is provided for the device as a master clock. The master clock is used as a reference clock for all the internal circuits. A better active edge of the master clock is selected by the OSC_EDGE bit to improve jitter and wander performance.

In fact, an offset from the nominal frequency may input on the OSCI pin. This offset can be compensated by setting the NOMINAL_FREQ_VALUE[23:0] bits. The calibration range is within ±741 ppm.

The performance of the master clock should meet GR-1244-CORE, GR-253-CORE, ITU-T G.812 and G.813 criteria.

Table 2: Related Bit / Register in Chapter 3.2

Bit	Register	Address (Hex)
NOMINAL_FREQ_VALUE[23:0]	NOMINAL_FREQ[23:16]_CNFG, NOMINAL_FREQ[15:8]_CNFG, NOMINAL_FREQ[7:0]_CNFG	06, 05, 04
OSC_EDGE	DIFFERENTIAL_IN_OUT_OSCI_CNFG	0A

3.3 INPUT CLOCKS & FRAME SYNC SIGNAL

Altogether 5 clocks and 1 frame sync signal are input to the device.

3.3.1 INPUT CLOCKS

The device provides 5 input clock ports.

According to the input port technology, the input ports support the following technologies:

- PECL/LVDS
- CMOS

According to the input clock source, the following clock sources are supported:

- T1: Recovered clock from STM-N or OC-n
- T2: PDH network synchronization timing
- T3: External synchronization reference timing

IN1, IN2 and IN5 support CMOS input signal and the clock sources can be from T1, T2 or T3.

IN3 and IN4 support PECL/LVDS input signal and automatically detect whether the signal is PECL or LVDS. The clock sources can be from T1, T2 or T3.

For SDH and SONET networks, the default frequency is different. SONET / SDH frequency selection is controlled by the IN_SONET_SDH bit. During reset, the default value of the IN_SONET_SDH bit is determined by the SONET/$\overline{\text{SDH}}$ pin: high for SONET and low for SDH. After reset, the input signal on the SONET/$\overline{\text{SDH}}$ pin takes no effect.

IDT82V3285A supports single-ended input for differential input. Refer to Chapter 9.3.2.3 Single-Ended Input for Differential Input.

3.3.2 FRAME SYNC INPUT SIGNALS

A 2 kHz, 4 kHz or 8 kHz frame sync signal is input on the EX_SYNC1 pin. It is a CMOS input. The input frequency should match the setting in the SYNC_FREQ[1:0] bits.

The frame sync input signal is used for frame sync output signal synchronization. Refer to Chapter 3.13.2 Frame SYNC Output Signals for details.

Table 3: Related Bit / Register in Chapter 3.3

<table>
<tr><th>Bit</th><th>Register</th><th>Address (Hex)</th></tr>
<tr><td>IN_SONET_SDH</td><td rowspan="2">INPUT_MODE_CNFG</td><td rowspan="2">09</td></tr>
<tr><td>SYNC_FREQ[1:0]</td></tr>
</table>

3.4 INPUT CLOCK PRE-DIVIDER

Each input clock is assigned an internal Pre-Divider. The Pre-Divider is used to divide the clock frequency down to the DPLL required frequency, which is no more than 38.88 MHz.

For IN1 ~ IN5, the DPLL required frequency is set by the corresponding IN_FREQ[3:0] bits.

If the input clock is of 2 kHz, 4 kHz or 8 kHz, the Pre-Divider is bypassed automatically and the corresponding IN_FREQ[3:0] bits should be set to match the input frequency; the input clock can be inverted, as determined by the IN_2K_4K_8K_INV bit.

Each Pre-Divider consists of a HF (High Frequency) Divider (only available for IN3 and IN4), a DivN Divider and a Lock 8k Divider, as shown in Figure 3.

The HF Divider, which is only available for IN3 and IN4, should be used when the input clock is higher than (>) 155.52 MHz. The input clock can be divided by 4, 5 or can bypass the HF Divider, as determined by the IN3_DIV[1:0]/IN4_DIV[1:0] bits correspondingly.

Either the DivN Divider or the Lock 8k Divider can be used or both can be bypassed, as determined by the DIRECT_DIV bit and the LOCK_8K bit.

When the DivN Divider is used for INn ($1 \le n \le 5$), the division factor setting should observe the following order:

1. *Select an input clock by the PRE_DIV_CH_VALUE[3:0] bits;*
2. *Write the lower eight bits of the division factor to the PRE_DIVN_VALUE[7:0] bits;*
3. *Write the higher eight bits of the division factor to the PRE_DIVN_VALUE[14:8] bits.*

Once the division factor is set for the input clock selected by the PRE_DIV_CH_VALUE[3:0] bits, it is valid until a different division factor is set for the same input clock. The division factor is calculated as follows:

Division Factor = (the frequency of the clock input to the DivN Divider ÷ the frequency of the DPLL required clock set by the IN_FREQ[3:0] bits) - 1

The DivN Divider can only divide the input clock whose frequency is lower than (<) 155.52 MHz.

When the Lock 8k Divider is used, the input clock is divided down to 8 kHz automatically.

The Pre-Divider configuration and the division factor setting depend on the input clock on one of the IN1 ~ IN5 pins and the DPLL required clock. Here is an example:

The input clock on the IN4 pin is 622.08 MHz; the DPLL required clock is 6.48 MHz by programming the IN_FREQ[3:0] bits of register IN4 to '0010'. Do the following step by step to divide the input clock:

1. *Use the HF Divider to divide the clock down to 155.52 MHz:*
   622.08 ÷ 155.52 = 4, so set the IN4_DIV[1:0] bits to '01';
2. *Use the DivN Divider to divide the clock down to 6.48 MHz:*
   Set the PRE_DIV_CH_VALUE[3:0] bits to '0110';
   Set the DIRECT_DIV bit in Register IN4_CNFG to '1' and the LOCK_8K bit in Register IN4_CNFG to '0';
   155.52 ÷ 6.48 = 24; 24 - 1 = 23, so set the PRE_DIVN_VALUE[14:0] bits to '10111'.

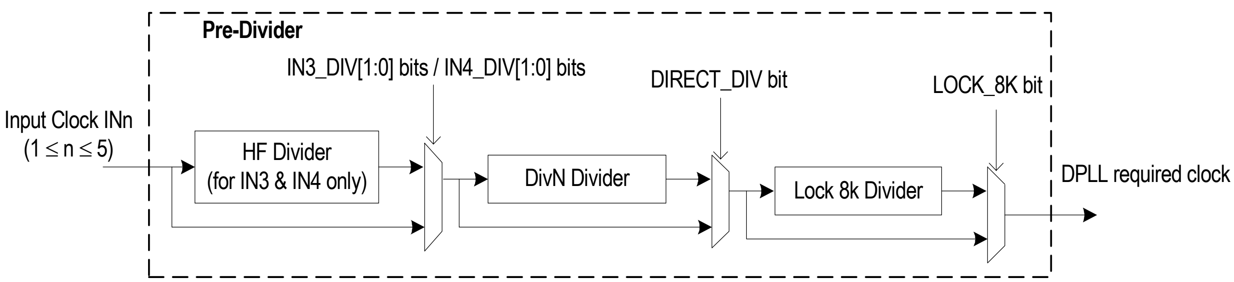

Figure 3. Pre-Divider for An Input Clock

Table 4: Related Bit / Register in Chapter 3.4

Bit	Register	Address (Hex)
IN3_DIV[1:0]	IN3_IN4_HF_DIV_CNFG	18
IN4_DIV[1:0]		
IN_FREQ[3:0]	IN1_CNFG ~ IN5_CNFG	16 ~ 17, 19 ~ 1A, 1F
IN_2K_4K_8K_INV	FR_MFR_SYNC_CNFG	74
DIRECT_DIV	IN1_CNFG ~ IN5_CNFG	16 ~ 17, 19 ~ 1A, 1F
LOCK_8K		
PRE_DIV_CH_VALUE[3:0]	PRE_DIV_CH_CNFG	23
PRE_DIVN_VALUE[14:0]	PRE_DIVN[14:8]_CNFG, PRE_DIVN[7:0]_CNFG	25, 24

3.5 INPUT CLOCK QUALITY MONITORING

The qualities of all the input clocks are always monitored in the following aspects:

- Activity
- Frequency

Activity and frequency monitoring are conducted on all the input clocks.

The qualified clocks are available for T0/T4 DPLL selection. The T0 and T4 selected input clocks have to be monitored further. Refer to Chapter 3.7 Selected Input Clock Monitoring for details.

3.5.1 ACTIVITY MONITORING

Activity is monitored by using an internal leaky bucket accumulator, as shown in Figure 4.

Each input clock is assigned an internal leaky bucket accumulator. The input clock is monitored for each period of 128 ms and the internal leaky bucket accumulator increases by 1 when an event is detected; it decreases by 1 if no event is detected within the period set by the decay rate. The event is that an input clock drifts outside (>) ±500 ppm with respect to the master clock within a 128 ms period.

There are four configurations (0 - 3) for a leaky bucket accumulator. The leaky bucket configuration for an input clock is selected by the corresponding BUCKET_SEL[1:0] bits. Each leaky bucket configuration consists of four elements: upper threshold, lower threshold, bucket size and decay rate.

The bucket size is the capability of the accumulator. If the number of the accumulated events reaches the bucket size, the accumulator will stop increasing even if further events are detected. The upper threshold is a point above which a no-activity alarm is raised. The lower threshold is a point below which the no-activity alarm is cleared. The decay rate is a certain period during which the accumulator decreases by 1 if no event is detected.

The leaky bucket configuration is programmed by one of four groups of register bits: the BUCKET_SIZE_n_DATA[7:0] bits, the UPPER_THRESHOLD_n_DATA[7:0] bits, the LOWER_THRESHOLD_n_DATA[7:0] bits and the DECAY_RATE_n_DATA[1:0] bits respectively; 'n' is 3.

The no-activity alarm status of the input clock is indicated by the INn_NO_ACTIVITY_ALARM bit ($1 \leq n \leq 5$).

The input clock with a no-activity alarm is disqualified for clock selection for T0/T4 DPLL.

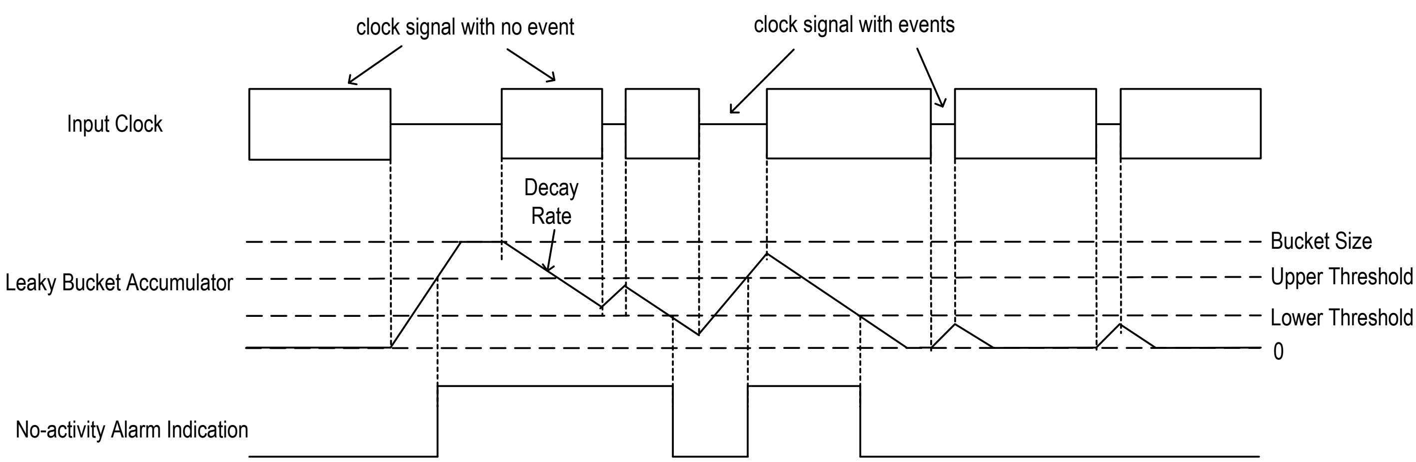

Figure 4. Input Clock Activity Monitoring

3.5.2 FREQUENCY MONITORING

Frequency is monitored by comparing the input clock with a reference clock. The reference clock can be derived from the master clock or the output of T0 DPLL, as determined by the FREQ_MON_CLK bit.

A frequency hard alarm threshold is set for frequency monitoring. If the FREQ_MON_HARD_EN bit is '1', a frequency hard alarm is raised when the frequency of the input clock with respect to the reference clock is above the threshold; the alarm is cleared when the frequency is below the threshold.

The frequency hard alarm threshold can be calculated as follows:

Frequency Hard Alarm Threshold (ppm) = (ALL_FREQ_HARD_THRESHOLD[3:0] + 1) X FREQ_MON_FACTOR[3:0]

If the FREQ_MON_HARD_EN bit is '1', the frequency hard alarm status of the input clock is indicated by the INn_FREQ_HARD_ALARM bit ($1 \leq n \leq 5$). When the FREQ_MON_HARD_EN bit is '0', no frequency hard alarm is raised even if the input clock is above the frequency hard alarm threshold.

The input clock with a frequency hard alarm is disqualified for clock selection for T0/T4 DPLL.

In addition, if the input clock is 2 kHz, 4 kHz or 8 kHz, its clock edges with respect to the reference clock are monitored. If any edge drifts outside ±5%, the input clock is disqualified for clock selection for T0/T4 DPLL. The input clock is qualified if any edge drifts inside ±5%. This function is supported only when the IN_NOISE_WINDOW bit is '1'.

The frequency of each input clock with respect to the reference clock can be read by doing the following step by step:

1. *Select an input clock by setting the IN_FREQ_READ_CH[3:0] bits;*
2. *Read the value in the IN_FREQ_VALUE[7:0] bits and calculate as follows:*

   Input Clock Frequency (ppm) = IN_FREQ_VALUE[7:0] X FREQ_MON_FACTOR[3:0]

Note that the value set by the FREQ_MON_FACTOR[3:0] bits depends on the application.

Table 5: Related Bit / Register in Chapter 3.5

Bit	Register	Address (Hex)
BUCKET_SIZE_n_DATA[7:0] (n = 3)	BUCKET_SIZE_3_CNFG	3F
UPPER_THRESHOLD_n_DATA[7:0] (n = 3)	UPPER_THRESHOLD_3_CNFG	3D
LOWER_THRESHOLD_n_DATA[7:0] (n = 3)	LOWER_THRESHOLD_3_CNFG	3E
DECAY_RATE_n_DATA[1:0] (n = 3)	DECAY_RATE_3_CNFG	40
BUCKET_SEL[1:0]	IN1_CNFG ~ IN5_CNFG	16 ~ 17, 19 ~ 1A, 1F
INn_NO_ACTIVITY_ALARM ($1 \leq n \leq 5$)	IN1_IN2_STS, IN3_IN4_STS, IN5_STS	44~ 45, 48
INn_FREQ_HARD_ALARM ($1 \leq n \leq 5$)		
FREQ_MON_CLK	MON_SW_PBO_CNFG	0B
FREQ_MON_HARD_EN		
ALL_FREQ_HARD_THRESHOLD[3:0]	ALL_FREQ_MON_THRESHOLD_CNFG	2F
FREQ_MON_FACTOR[3:0]	FREQ_MON_FACTOR_CNFG	2E
IN_NOISE_WINDOW	PHASE_MON_PBO_CNFG	78
IN_FREQ_READ_CH[3:0]	IN_FREQ_READ_CH_CNFG	41
IN_FREQ_VALUE[7:0]	IN_FREQ_READ_STS	42

3.6 T0 / T4 DPLL INPUT CLOCK SELECTION

An input clock is selected for T0 DPLL and for T4 DPLL respectively.

For T0 path, the EXT_SW bit and the T0_INPUT_SEL[3:0] bits determine the input clock selection, as shown in Table 6:

Table 6: Input Clock Selection for T0 Path

Control Bits		Input Clock Selection
EXT_SW	T0_INPUT_SEL[3:0]	
1	don't-care	External Fast selection
0	other than 0000	Forced selection
	0000	Automatic selection

For T4 path, the T4 DPLL may lock to a T0 DPLL output or lock independently from T0 path, as determined by the T4_LOCK_T0 bit. When the T4 DPLL locks to the T0 DPLL output, the T4 selected input clock is a 77.76 MHz or 8 kHz signal from the T0 DPLL 77.76 MHz path (refer to Chapter 3.11.5.1 T0 Path), as determined by the T0_FOR_T4 bit. When the T4 path locks independently from the T0 path, the T4 DPLL input clock selection is determined by the T4_INPUT_SEL[3:0] bits. Refer to Table 7:

Table 7: Input Clock Selection for T4 Path

Control Bits - T4_INPUT_SEL[3:0]	Input Clock Selection
other than 0000	Forced selection
0000	Automatic selection

External Fast selection is done between IN1/IN3 and IN2/IN4 pairs.

Forced selection is done by setting the related registers.

Automatic selection is done based on the results of input clocks quality monitoring and the related registers configuration.

The selected input clock is attempted to be locked in T0/T4 DPLL.

3.6.1 EXTERNAL FAST SELECTION (T0 ONLY)

The External Fast selection is supported by T0 path only. In External Fast selection, only IN1/IN3 and IN2/IN4 pairs are available for selection. Refer to Figure 5. The results of input clocks quality monitoring (refer to Chapter 3.5 Input Clock Quality Monitoring) do not affect input clock selection.

The T0 input clock selection is determined by the FF_SRCSW pin after reset (this pin determines the default value of the EXT_SW bit during reset, refer to Chapter 2 Pin Description), the IN1_SEL_PRIORITY[3:0] bits and the IN2_SEL_PRIORITY[3:0] bits, as shown in Figure 5 and Table 8:

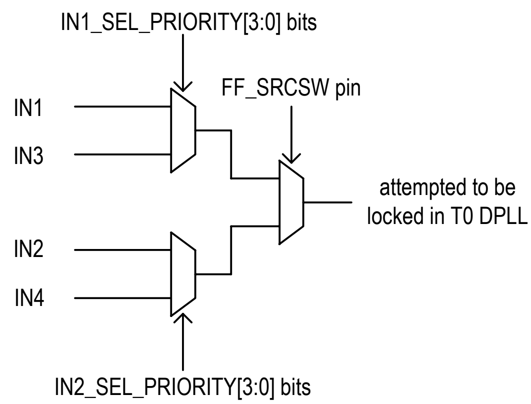

Figure 5. External Fast Selection

Table 8: External Fast Selection

Control Pin & Bits			Selected Input Clock
FF_SRCSW (after reset)	IN1_SEL_PRIORITY[3:0]	IN2_SEL_PRIORITY[3:0]	
high	0000	don't-care	IN3
	other than 0000		IN1
low	don't-care	0000	IN4
		other than 0000	IN2

3.6.2 FORCED SELECTION

In Forced selection, the selected input clock is set by the T0_INPUT_SEL[3:0] / T4_INPUT_SEL[3:0] bits. The results of input clocks quality monitoring (refer to Chapter 3.5 Input Clock Quality Monitoring) do not affect the input clock selection.

3.6.3 AUTOMATIC SELECTION

In Automatic selection, the input clock selection is determined by its validity, priority and locking allowance configuration. The validity depends on the results of input clock quality monitoring (refer to Chapter 3.5 Input Clock Quality Monitoring). Locking allowance is configured by the corresponding INn_VALID bit(1 ≤ n ≤ 5). Refer to Figure 6. In all the qualified input clocks, the one with the highest priority is selected. The priority is set by the corresponding INn_SEL_PRIORITY[3:0] bits (1 ≤ n ≤ 5). If more than one qualified input clock INn is available and has the same priority, the input clock with the smallest 'n' is selected.

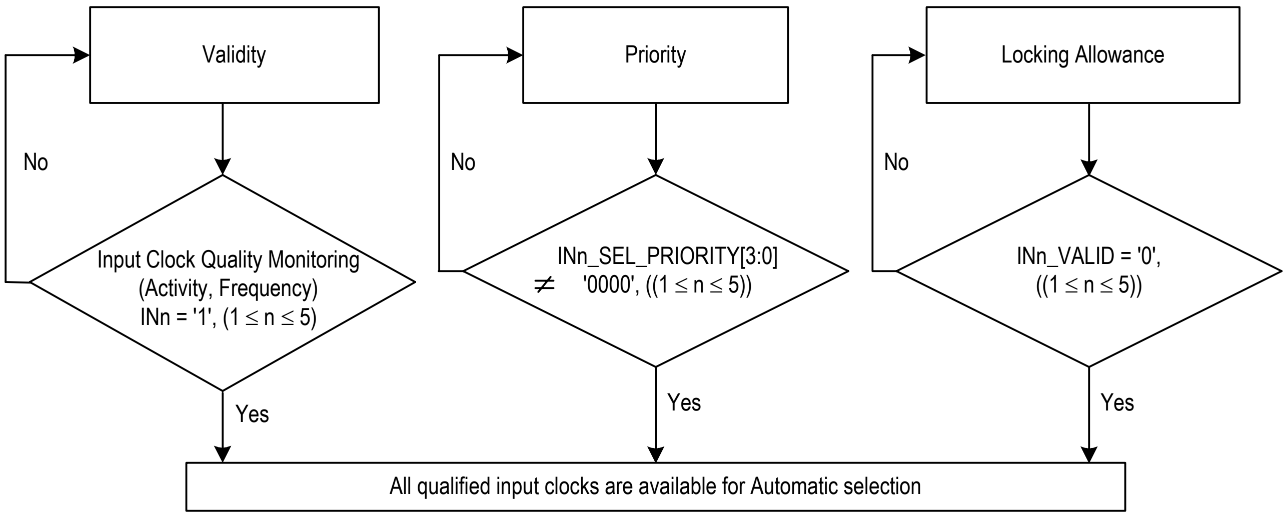

Figure 6. Qualified Input Clocks for Automatic Selection

Table 9: Related Bit / Register in Chapter 3.6

Bit	Register	Address (Hex)
EXT_SW	MON_SW_PBO_CNFG	0B
T0_INPUT_SEL[3:0]	T0_INPUT_SEL_CNFG	50
T4_LOCK_T0	T4_INPUT_SEL_CNFG	51
T0_FOR_T4		
T4_INPUT_SEL[3:0]		
INn_SEL_PRIORITY[3:0] (1 ≤ n ≤ 5)	IN1_IN2_SEL_PRIORITY_CNFG IN3_IN4_SEL_PRIORITY_CNFG IN5_SEL_PRIORITY_CNFG	27 ~ 28, 2B
INn_VALID (1 ≤ n ≤ 5)	REMOTE_INPUT_VALID1_CNFG, REMOTE_INPUT_VALID2_CNFG	4C, 4D
INn (1 ≤ n ≤ 5)	INPUT_VALID1_STS, INPUT_VALID2_STS	4A, 4B
T4_T0_SEL	T4_T0_REG_SEL_CNFG	07

Note: * The setting in the 26 ~ 2C registers is either for T0 path or for T4 path, as determined by the T4_T0_SEL bit.

3.7 SELECTED INPUT CLOCK MONITORING

The quality of the selected input clock is always monitored (refer to Chapter 3.5 Input Clock Quality Monitoring) and the DPLL locking status is always monitored.

3.7.1 T0 / T4 DPLL LOCKING DETECTION

The following events are always monitored:

- Fast Loss;
- Coarse Phase Loss;
- Fine Phase Loss;
- Hard Limit Exceeding.

3.7.1.1 Fast Loss

A fast loss is triggered when the selected input clock misses 2 consecutive clock cycles. It is cleared once an active clock edge is detected.

For T0 path, the occurrence of the fast loss will result in T0 DPLL being unlocked if the FAST_LOS_SW bit is ‘1’. For T4 path, the occurrence of the fast loss will result in T4 DPLL being unlocked regardless of the FAST_LOS_SW bit.

3.7.1.2 Coarse Phase Loss

The T0/T4 DPLL compares the selected input clock with the feedback signal. If the phase-compared result exceeds the coarse phase limit, a coarse phase loss is triggered. It is cleared once the phase-compared result is within the coarse phase limit.

When the selected input clock is of 2 kHz, 4 kHz or 8 kHz, the coarse phase limit depends on the MULTI_PH_8K_4K_2K_EN bit, the WIDE_EN bit and the PH_LOS_COARSE_LIMT[3:0] bits. Refer to Table 10. When the selected input clock is of other frequencies than 2 kHz, 4 kHz and 8 kHz, the coarse phase limit depends on the WIDE_EN bit and the PH_LOS_COARSE_LIMT[3:0] bits. Refer to Table 11.

Table 10: Coarse Phase Limit Programming (the selected input clock of 2 kHz, 4 kHz or 8 kHz)

MULTI_PH_8K_4K_2K_EN	WIDE_EN	Coarse Phase Limit
0	don’t-care	±1 UI
1	0	±1 UI
	1	set by the PH_LOS_COARSE_LIMT[3:0] bits

Table 11: Coarse Phase Limit Programming (the selected input clock of other than 2 kHz, 4 kHz and 8 kHz)

WIDE_EN	Coarse Phase Limit
0	±1 UI
1	set by the PH_LOS_COARSE_LIMT[3:0] bits

The occurrence of the coarse phase loss will result in T0/T4 DPLL being unlocked if the COARSE_PH_LOS_LIMT_EN bit is ‘1’.

3.7.1.3 Fine Phase Loss

The T0/T4 DPLL compares the selected input clock with the feedback signal. If the phase-compared result exceeds the fine phase limit programmed by the PH_LOS_FINE_LIMT[2:0] bits, a fine phase loss is triggered. It is cleared once the phase-compared result is within the fine phase limit.

The occurrence of the fine phase loss will result in T0/T4 DPLL being unlocked if the FINE_PH_LOS_LIMT_EN bit is ‘1’.

3.7.1.4 Hard Limit Exceeding

Two limits are available for this monitoring. They are DPLL soft limit and DPLL hard limit. When the frequency of the DPLL output with respect to the master clock exceeds the DPLL soft / hard limit, a DPLL soft / hard alarm will be raised; the alarm is cleared once the frequency is within the corresponding limit. The occurrence of the DPLL soft alarm does not affect the T0/T4 DPLL locking status. The DPLL soft alarm is indicated by the corresponding T0_DPLL_SOFT_FREQ_ALARM / T4_DPLL_SOFT_FREQ_ALARM bit. The occurrence of the DPLL hard alarm will result in T0/T4 DPLL being unlocked if the FREQ_LIMT_PH_LOS bit is ‘1’.

The DPLL soft limit is set by the DPLL_FREQ_SOFT_LIMT[6:0] bits and can be calculated as follows:

DPLL Soft Limit (ppm) = DPLL_FREQ_SOFT_LIMT[6:0] X 0.724

The DPLL hard limit is set by the DPLL_FREQ_HARD_LIMT[15:0] bits and can be calculated as follows:

DPLL Hard Limit (ppm) = DPLL_FREQ_HARD_LIMT[15:0] X 0.0014

3.7.2 LOCKING STATUS

The DPLL locking status depends on the locking monitoring results. The DPLL is in locked state if none of the following events is triggered during 2 seconds; otherwise, the DPLL is unlocked.

- Fast Loss (the FAST_LOS_SW bit is ‘1’);
- Coarse Phase Loss (the COARSE_PH_LOS_LIMT_EN bit is ‘1’);
- Fine Phase Loss (the FINE_PH_LOS_LIMT_EN bit is ‘1’);
- DPLL Hard Alarm (the FREQ_LIMT_PH_LOS bit is ‘1’).

If the FAST_LOS_SW bit, the COARSE_PH_LOS_LIMT_EN bit, the FINE_PH_LOS_LIMT_EN bit or the FREQ_LIMT_PH_LOS bit is ‘0’, the DPLL locking status will not be affected even if the corresponding event is triggered. If all these bits are ‘0’, the DPLL will be in locked state in 2 seconds.

The DPLL locking status is indicated by the T0_DPLL_LOCK / T4_DPLL_LOCK bit.

The T4_STS [1] bit will be set when the locking status of the T4 DPLL changes (from ‘locked’ to ‘unlocked’ or from ‘unlocked’ to ‘locked’). If the T4_STS [2] bit is ‘1’, an interrupt will be generated.