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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Low Skew, 1-to-4 LVCMOS/LVTTL Fanout Buffer

8304

8304AMLN - PDN CQ-16-01 - LAST TIME BUY EXPIRES MAY 6, 2017

DATA SHEET

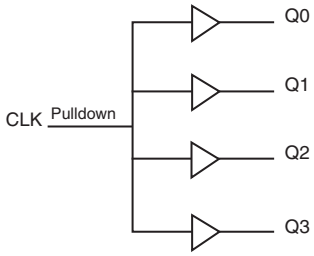
General Description

The 8304 is a low skew, 1-to-4 Fanout Buffer. The 8304 is characterized at full 3.3V for input (V_{DD}), and mixed 3.3V and 2.5V for output operating supply modes (V_{DDO}). Guaranteed output and part-to-part skew characteristics make the 8304 ideal for those clock distribution applications demanding well defined performance and repeatability.

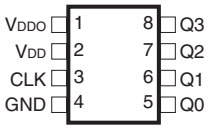
Features

- Four LVCMOS / LVTTL outputs
- LVCMOS / LVTTL clock input
- CLK can accept the following input levels: LVCMOS, LVTTL
- Maximum output frequency: 200MHz
- Additive phase jitter, RMS: 0.173ps (typical) @ 3.3V
- Output skew: 45ps (maximum) @ 3.3V
- Part-to-part skew: 500ps (maximum)
- Small 8 lead SOIC package saves board space
- 3.3V input, outputs may be either 3.3V or 2.5V supply modes
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) compliant package

Block Diagram



Pin Assignment



8304
8-Lead SOIC
3.9mm x 4.9mm, x 1.375mm package body
M Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{DDO}	Power		Output supply pin.
2	V_{DD}	Power		Positive supply pin.
3	CLK	Input	Pulldown	LVCMOS / LVTTL clock input.
4	GND	Power		Power supply ground.
5	Q0	Output		Single clock output. LVCMOS / LVTTL interface levels.
6	Q1	Output		Single clock output. LVCMOS / LVTTL interface levels.
7	Q2	Output		Single clock output. LVCMOS / LVTTL interface levels.
8	Q3	Output		Single clock output. LVCMOS / LVTTL interface levels.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDO} = 3.465V			15	pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance		5	7	12	Ω

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	112.7°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V±5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Power Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				15	mA
I_{DDO}	Output Supply Current				8	mA

Table 3B. Power Supply DC Characteristics, $V_{DD} = 3.3V±5\%$, $V_{DDO} = 2.5V±5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				15	mA
I_{DDO}	Output Supply Current				8	mA

Table 3C. LVCMOS / LVTTL DC Characteristics, $V_{DD} = V_{DDO} = 3.3V±5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		1.3	V
I_{IH}	Input High Current	$V_{DD} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5			µA
V_{OH}	Output High Voltage	Refer to NOTE 1	2.6			V
		I_{OH} = -16mA	2.9			V
		I_{OH} = -100uA	3			V
V_{OL}	Output Low Voltage	Refer to NOTE 1			0.5	V
		I_{OL} = 16mA			0.25	V
		I_{OL} = 100uA			0.15	V

NOTE 1: Outputs terminated with 50 to $V_{DDO}/2$. See Parameter Measurement Section, “3.3V Output Load Test Circuit”.

TABLE 3D. LVCMOS / LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		1.3	V
I_{IH}	Input High Current	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1		2.1			V
V_{OL}	Output Low Voltage; NOTE 1				0.5	V

NOTE 1: Outputs terminated with 50 to V_{DDO}/2. See Parameter Measurement Section, "3.3V/2.5V Output Load Test Circuit".

TABLE 4A. AC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency				200	MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1	$f \leq$ 166MHz	2.0		3.3	ns
		166MHz < f ≤ 189.5MHz	2.0		3.4	ns
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	125MHz, Integration Range: 12kHz – 20MHz		0.173		ps
tsk(o)	Output Skew; NOTE 2, 4	f = 133MHz			45	ps
tsk(pp)	Part-to-Part Skew; NOTE 3, 4				500	ps
t_R	Output Rise Time	30% to 70%	250		500	ps
t_F	Output Fall Time	30% to 70%	250		500	ps
odc	Output Duty Cycle	f ≤ 189.5MHz	40		60	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

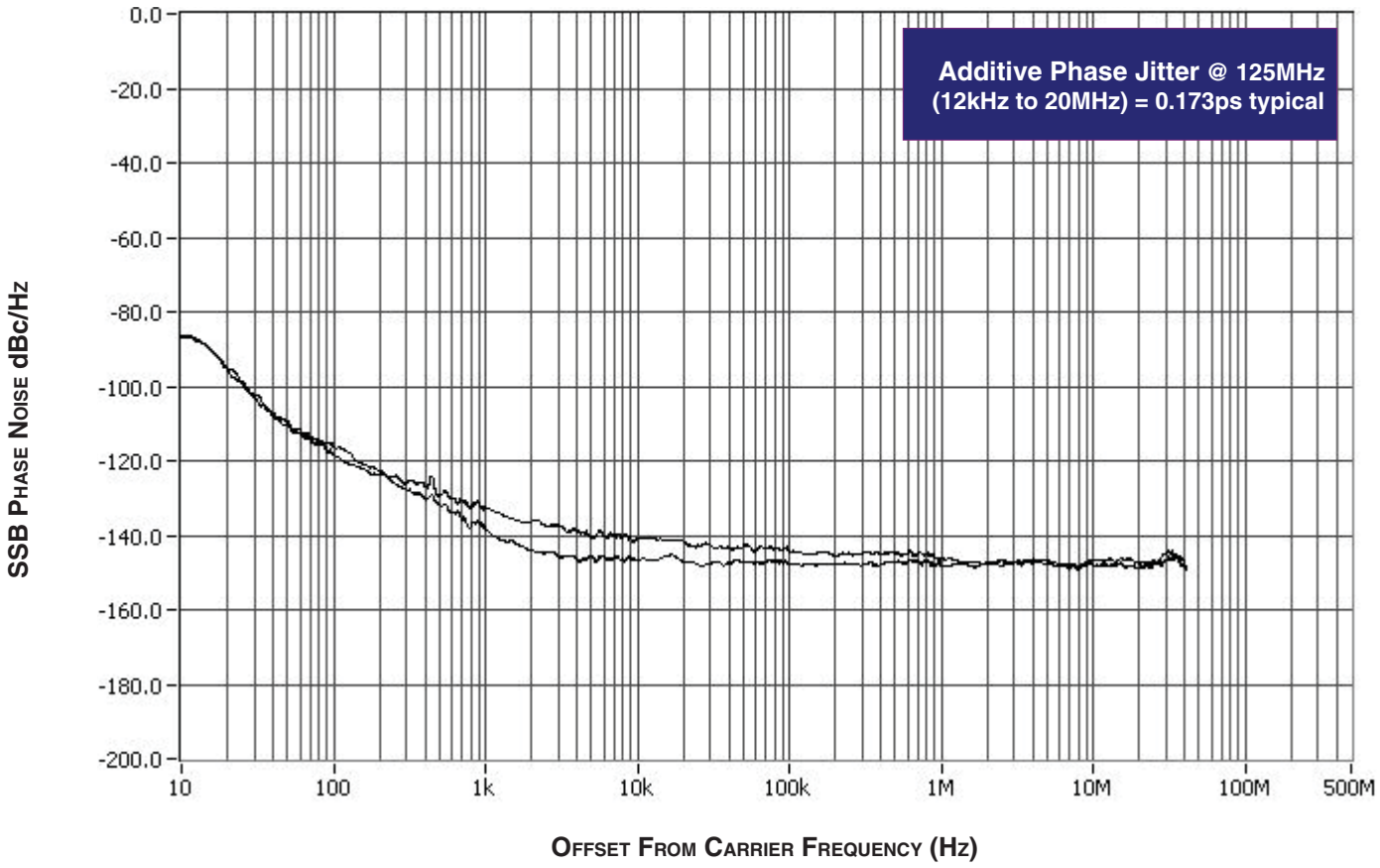
TABLE 4B. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency				189.5	MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1	$f \leq$ 166MHz	2.3		3.7	ns
		166MHz < f ≤ 189.5MHz	2.15		3.55	ns
tsk(o)	Output Skew; NOTE 2, 4	f = 133MHz			60	ps
tsk(pp)	Part-to-Part Skew; NOTE 3, 4				500	ps
t_R	Output Rise Time	30% to 70%	250		500	ps
t_F	Output Fall Time	30% to 70%	250		500	ps
odc	Output Duty Cycle	f ≤ 189.5MHz	40		60	%

For NOTES, please see above Table 4A.

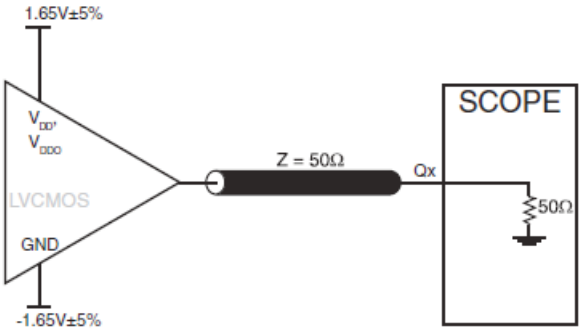
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

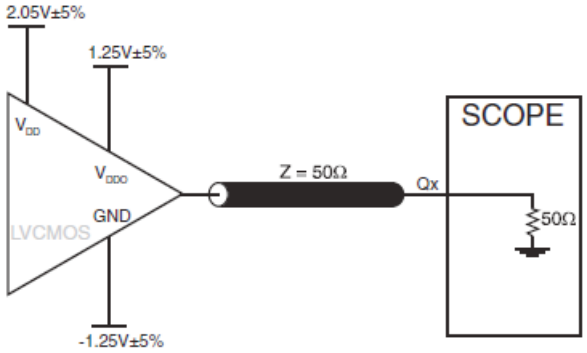


As with most timing specifications, phase noise measurements has issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

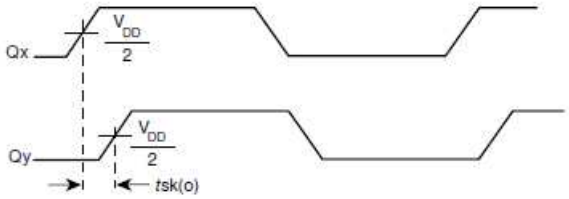
Parameter Measurement Information



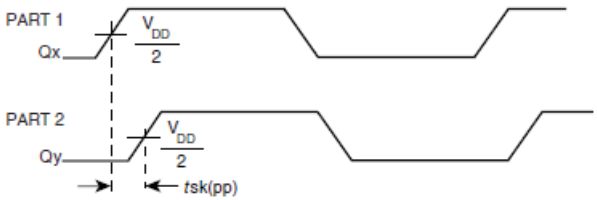
3.3V Output Load AC Test Circuit



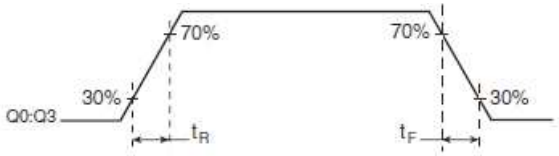
2.5V Output Load AC Test Circuit



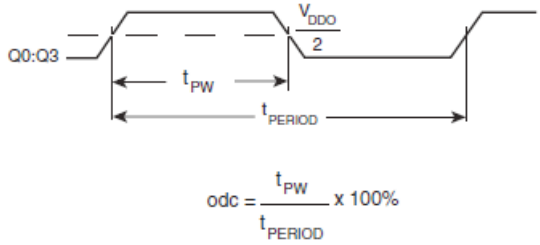
Output Skew



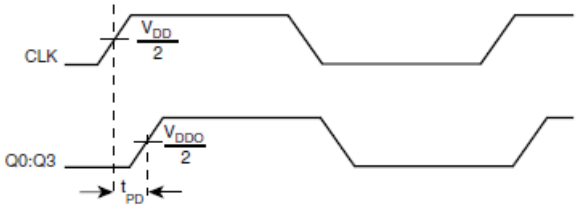
Part-to-Part Skew



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period



Propagation Delay

Application Information

Recommendations for Unused Output Pins

Outputs:

LVCMOS Output:
All unused LVCMOS output can be left floating. There should be no trace attached.

Reliability Information

Table 5. θ_{JA} vs. Air Flow Table

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for 8304 is: 416

Package Outline - Suffix M for 8 Lead SOIC

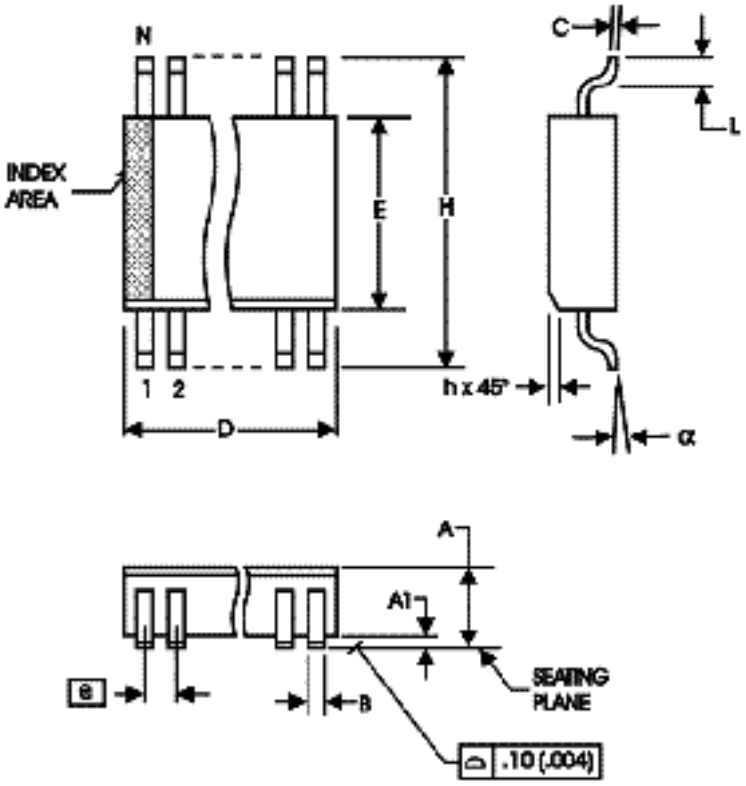


Table 6. Package Dimensions - Suffix M

SYMBOL	Millimeters	
	MINIMUN	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8304AMLF	8304AMLF	8 lead “Lead Free” SOIC	Tube	0°C to +70°C
8304AMLFT	8304AMLF	8 lead “Lead Free” SOIC	Tape and Reel	0°C to +70°C
8304AMLN	8304AMLN	8 lead SOIC, Lead Free/Annealed	Tube	0°C to +70°C
8304AMLNT	8304AMLN	8 lead SOIC, Lead Free/Annealed	Tape and Reel	0°C to +70°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T4A T4B	3 4	• Revised tp_{LH} (Propagation Delay) row from 2.3 Min. to 2 Min. • Deleted tp_{HL} row. • Revised tsk(o) (Output Skew) row from 35 Max. to 80 Max. • Revised tsk(pp) (Part-to-Part Skew) row from 200 Max. to 500 Max. • General note changed from "...measured at 166MHz..." to " ...measured at 150MHz..." • Revised tp_{LH} (Propagation Delay) row from 2.6 Min. to 2.3 Min. • Deleted tp_{HL} row. • Revised tsk(o) (Output Skew) row from 35 Max. to 85 Max. • Revised tsk(pp) (Part-to-Part Skew) row from 200 Max. to 500 Max. • General note changed from "...measured at 166MHz..." to " ...measured at 150MHz..."	12/4/01
C	T4A T4B	3 4	• In AC table, revised tsk(o) row from 80ps Max. to 45ps Max. Added f = 133MHz in Test Conditions column. • In odc row, deleted test conditions. • In notes, changed 150MHz to $f_{MAX.}$ • In AC table, revised tsk(o) row from 80ps Max. to 60ps Max. Added f = 133MHz in Test Conditions column. • In odc row, deleted test conditions • In notes, changed 150MHz to $f_{MAX.}$	12/11/01
C	T7	10	In the Ordering Information table, Marking column, revised marking to read 8304AM from 8304AM.	3/11/02
D	T3B	3	LVCMOS/LVTTL DC Characteristics Table, added I_{OH} and I_{OL} Test Conditions to V_{OH} and V_{OL} rows.	4/4/02
E	 T1 T2 T3A & T3C T7	1 2 2 3 & 4 8	• Pin Assignment - adjusted dimensions. • Pin Descriptions - changed V_{DD} description to Core supply pin. • Pin Characteristics - changed C_{IN} max 4pF to typical 4pF. Deleted R_{PULLUP} row. Added 5W min. and 12W max. to R_{OUT}. • Power Supply tables - changed V_{DD} parameter from Power to Core. • Ordering Information table - added "Lead Free/Annealed" marking. Updated format throughout the data sheet.	4/13/04
F	 T4A T4B	1 4 4	Featues section, changed Maximum output frequency bullet from 166MHz to 200MHz. 3.3V AC Table - changed 166MHz max. to 200MHz max. Added another line for Propagation Delay. Changed test conditions in Output Duty Cycle from 166MHz to 189.5MHz. 3.3V AC Table - changed 166MHz max. to 189.5MHz max. Added another line for Propagation Delay. Changed test conditions in Output Duty Cycle from 166MHz to 189.5MH	6/1/04
F	T7	8	• Ordering Information table - added "Lead Free" marking.	9/13/04
G	T4A	1 4 5 7	Features Section - added Additive Phase Jitter bullet. 3.3V AC Characteristics Table - added Additive Phase Jitter row. Added Additive Phase Jitter plot. Added Recommendations for Unused Output Pins.	6/11/07
H		1	Pin Assignment - corrected "pullup" label to "pulldown" label.	10/29/10
H	T7	9	Ordering Information - removed leaded devices. Updated data sheet format.	11/19/15
H			8304AMLN - Product Discontinuation Notice - Last time buy expires May 6, 2017. PDN CQ-16-01	5/9/16

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, California 95138

Sales
800-345-7015 or +408-284-8200
Fax: 408-284-2775
www.IDT.com

Technical Support
email: clocks@idt.com