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General Description

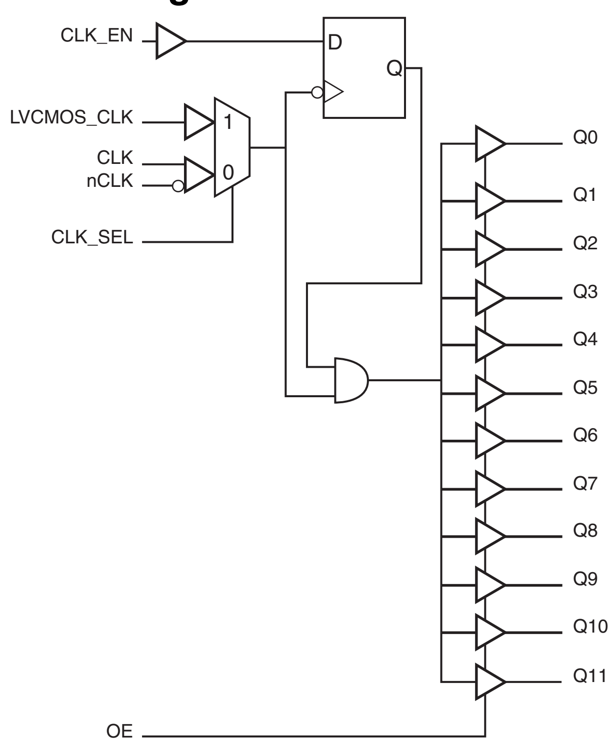
The 83948I-147 is a low skew, 1-to-12 Differential-to-LVCMOS/LVTTL Fanout Buffer. The 83948I-147 has two selectable clock inputs. The CLK, nCLK pair can accept most standard differential input levels. The LVCMOS_CLK can accept LVCMOS or LVTTL input levels. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 12 to 24 by utilizing the ability of the outputs to drive two series terminated lines.

The 83948I-147 is characterized at full 3.3V, full 2.5V or mixed 3.3V core/2.5V output operating supply modes. Guaranteed output and part-to-part skew characteristics make the 83948I-147 ideal for those clock distribution applications demanding well defined performance and repeatability.

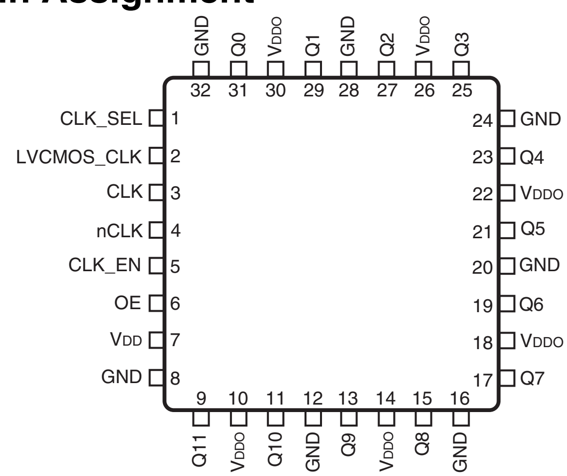
Features

- Twelve LVCMOS/LVTTL outputs
- Selectable differential CLK/nCLK or LVCMOS/LVTTL clock input
- CLK/nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- LVCMOS_CLK supports the following input types: LVCMOS, LVTTL
- Output frequency: 350MHz
- Additive phase jitter, RMS: 0.14ps (typical)
- Output skew: 100ps (maximum), 3.3V±5%
- Part-to-part skew: 1ns (maximum), 3.3V±5%
- Operating supply modes:
- Core/Output
  3.3V/3.3V
  3.3V/2.5V
  2.5V/2.5V
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

Block Diagram



Pin Assignment



83948I-147

32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

Pin Descriptions and Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1	CLK_SEL	Input	Pullup	Clock select input. When HIGH, selects LVCMOS_CLK input. When LOW, selects CLK/nCLK inputs. LVCMOS / LVTTL interface levels.
2	LVCMOS_CLK	Input	Pullup	Single-ended clock input. LVCMOS/LVTTL interface levels.
3	CLK	Input	Pullup	Non-inverting differential clock input.
4	nCLK	Input	Pulldown	Inverting differential clock input.
5	CLK_EN	Input	Pullup	Clock enable pin. LVCMOS/LVTTL interface levels.
6	OE	Input	Pullup	Output enable pin. When LOW, outputs are in an High-impedance state. when HIGH, outputs are active. LVCMOS/LVTTL interface levels.
7	V_{DD}	Power		Power supply pin.
8, 12, 16, 20, 24, 28, 32	GND	Power		Power supply ground.
9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31	Q11, Q10, Q9, Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
10, 14, 18, 22, 26, 30	V_{DDO}	Power		Output supply pins.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)			12		pF
R_{OUT}	Output Impedance		5	7	12	Ω

Function Tables

Table 3A. Clock Select Function Table

Control Input	Clock
0	CLK/nCLK inputs selected
1	LVCMOS_CLK input selected

Table 3B. Clock Input Function Table

Inputs				Outputs	Input to Output Mode	Polarity
CLK_SEL	LVCMOS_CLK	CLK	nCLK	Q[0:11]		
0	–	0	1	LOW	Differential to Single-Ended	Non-Inverting
0	–	1	0	HIGH	Differential to Single-Ended	Non-Inverting
0	–	0	Biased; NOTE 1	LOW	Single-Ended to Single-Ended	Non-Inverting
0	–	1	Biased; NOTE 1	HIGH	Single-Ended to Single-Ended	Non-Inverting
0	–	Biased; NOTE 1	0	HIGH	Single-Ended to Single-Ended	Inverting
0	–	Biased; NOTE 1	1	LOW	Single-Ended to Single-Ended	Inverting
1	0	–	–	LOW	Single-Ended to Single-Ended	Non-Inverting
1	1	–	–	HIGH	Single-Ended to Single-Ended	Non-Inverting

NOTE 1: Please refer to the Application Information Section, *Wiring the Differential Input to Accept Single-ended Levels.*

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	73.6°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40°C$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				55	mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = -40°C$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				52	mA

Table 4C. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				55	mA

Table 4D. DC Characteristics, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	LVCMOS	V_{DD} = 3.465V	2		V_{DD} + 0.3	V
		LVCMOS	V_{DD} = 2.625V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	LVCMOS	V_{DD} = 3.465V	-0.3		0.8	V
		LVCMOS	V_{DD} = 2.625V	-0.3		0.7	V
I_{IN}	Input Current		V_{IN} = V_{DD} or V_{IN} = 3.465V or 2.625V			300	µA
V_{OH}	Output High Voltage; NOTE 1		V_{DDO} = 3.3V ± 5% I_{OH} = -24mA	2.4			V
			V_{DDO} = 2.5V ± 5% I_{OH} = -15mA	1.8			V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDO} = 3.3V ± 5% I_{OL} = 24mA			0.55	V
			V_{DDO} = 3.3V ± 5% I_{OL} = 12mA			0.30	V
			V_{DDO} = 2.5V ± 5% I_{OL} = 15mA			0.6	V
V_{PP}	Peak-to-Peak Input Voltage; NOTE 2	CLK/nCLK	V_{DD} = 3.465V or 2.625V	0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 2, 3	CLK/nCLK	V_{DD} = 3.465V or 2.625V	GND + 0.5		V_{DD} – 0.85	V

NOTE 1: Outputs capable of driving 50Ω transmission lines terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement section, *Output Load AC Test Circuit diagrams.*
NOTE 2: V_{IL} should not be less than -0.3V.
NOTE 3: Common mode voltage is defined as V_{IH}.

AC Electrical Characteristics

Table 5A. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40°C$ to $85°C$

Parameter	Symbol		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					350	MHz
t_{PD}	Propagation Delay	CLK/nCLK; NOTE 1	$f \le 350MHz$	2		4	ns
		LVCMOS_CLK; NOTE 2	$f \le 350MHz$	2		4	ns
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section		155.52MHz, Integration Range: 12kHz – 20MHz		0.14	1	ps
*t*sk(o)	Output Skew; NOTE 3, 7		Measured on the Rising Edge @ $V_{DDO}/2$			100	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 7		Measured on the Rising Edge @ $V_{DDO}/2$			1	ns
t_R / t_F	Output Rise/Fall Time		0.8V to 2V	0.2		1.0	ns
odc	Output Duty Cycle		$f \le 150MHz$, Ref = CLK/nCLK	45	50	55	%
t_{PZL}, t_{PZH}	Output Enable Time; NOTE 5					5	ns
t_{PLZ}, t_{PHZ}	Output Disable Time; NOTE 5					5	ns
t_S	Clock Enable Setup Time; NOTE 6	CLK_EN to CLK/nCLK		1			ns
		CLK_EN to LVCMOS_CLK		0			ns
t_H	Clock Enable Hold Time; NOTE 6	CLK/nCLK to CLK_EN		0			ns
		LVCMOS_CLK to CLK_EN		1			ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to $V_{DDO}/2$ of the output.
NOTE 2: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: Setup and Hold times are relative to the rising edge of the input clock.
NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

Table 5B. AC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = -40°C$ to $85°C$

Parameter	Symbol		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					350	MHz
t_{PD}	Propagation Delay	CLK/nCLK; NOTE 1	$f \le 350MHz$	1.5		4.2	ns
		LVCMOS_CLK; NOTE 2	$f \le 350MHz$	1.7		4.4	ns
$t$jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section		155.52MHz, Integration Range: 12kHz – 20MHz		0.14	1	ps
$t$sk(o)	Output Skew; NOTE 3, 7		Measured on the Rising Edge @ $V_{DDO}/2$			160	ps
$t$sk(pp)	Part-to-Part Skew; NOTE 4, 7		Measured on the Rising Edge @ $V_{DDO}/2$			2	ns
t_R / t_F	Output Rise/Fall Time		0.6V to 1.8V	0.1		1.0	ns
odc	Output Duty Cycle		$f \le 150MHz$, Ref = CLK/nCLK	40		60	%
t_{PZL}, t_{PZH}	Output Enable Time; NOTE 5					5	ns
t_{PLZ}, t_{PHZ}	Output Disable Time; NOTE 5					5	ns
t_S	Clock Enable Setup Time; NOTE 6	CLK_EN to CLK/nCLK		1			ns
		CLK_EN to LVCMOS_CLK		0			ns
t_H	Clock Enable Hold Time; NOTE 6	CLK/nCLK to CLK_EN		0			ns
		LVCMOS_CLK to CLK_EN		1			ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to $V_{DDO}/2$ of the output.
NOTE 2: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: Setup and Hold times are relative to the rising edge of the input clock.
NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

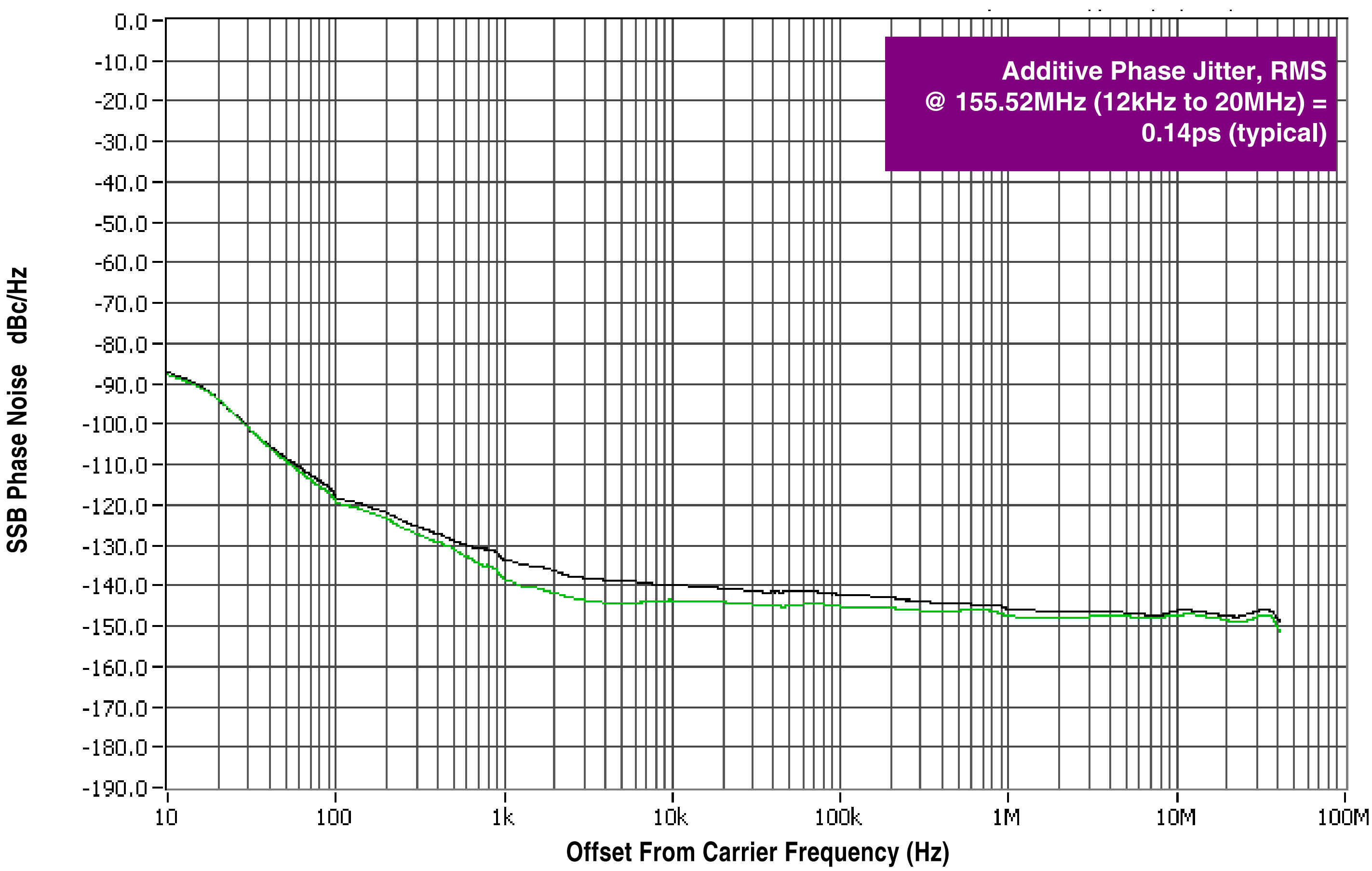
Table 5C. AC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 2.5V ± 5%, T_A = -40°C to 85°C

Parameter	Symbol		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					350	MHz
t_{PD}	Propagation Delay	CLK/nCLK; NOTE 1	$f \leq$ 350MHz	2		4	ns
		LVCMOS_CLK; NOTE 2	$f \leq$ 350MHz	2		4	ns
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section		155.52MHz, Integration Range: 12kHz – 20MHz		0.14	1	ps
*t*sk(o)	Output Skew; NOTE 3, 7		Measured on the Rising Edge @ $V_{DDO}/2$			100	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 7		Measured on the Rising Edge @ $V_{DDO}/2$			1	ns
t_R / t_F	Output Rise/Fall Time		0.8V to 2V	0.1		1.0	ns
odc	Output Duty Cycle		$f \leq$ 200MHz, Ref = CLK/nCLK	45		55	%
t_{PZL}, t_{PZH}	Output Enable Time; NOTE 5					5	ns
t_{PLZ}, t_{PHZ}	Output Disable Time; NOTE 5					5	ns
t_S	Clock Enable Setup Time; NOTE 6	CLK_EN to CLK/nCLK		1			ns
		CLK_EN to LVCMOS_CLK		0			ns
t_H	Clock Enable Hold Time; NOTE 6	CLK/nCLK to CLK_EN		0			ns
		LVCMOS_CLK to CLK_EN		1			ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to $V_{DDO}/2$ of the output.
NOTE 2: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: Setup and Hold times are relative to the rising edge of the input clock.
NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

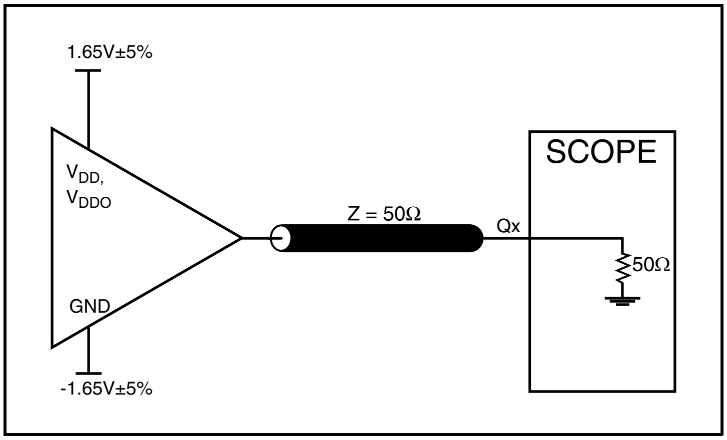
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

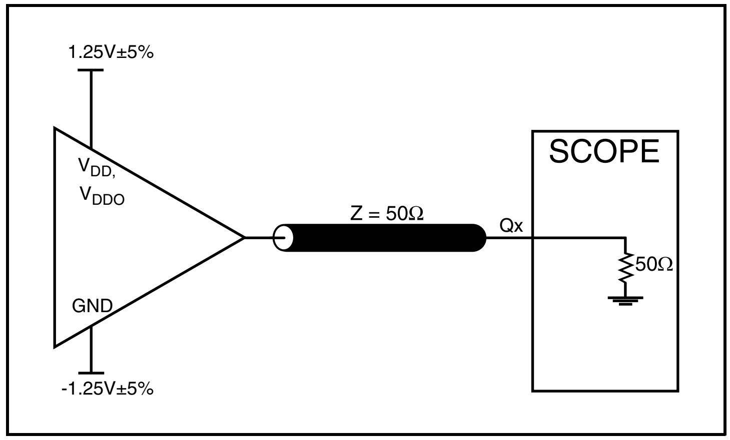


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

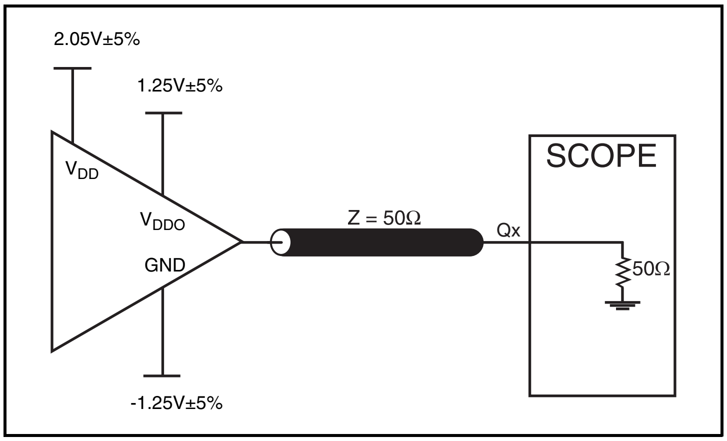
Parameter Measurement Information



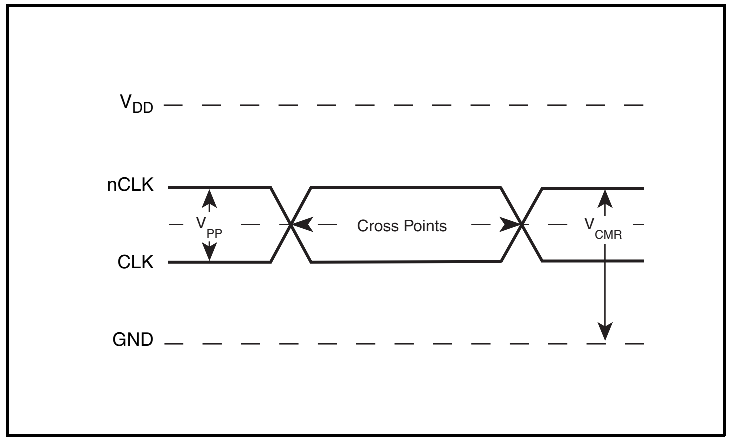
3.3V Core/3.3V LVCMOS Output Load AC Test Circuit



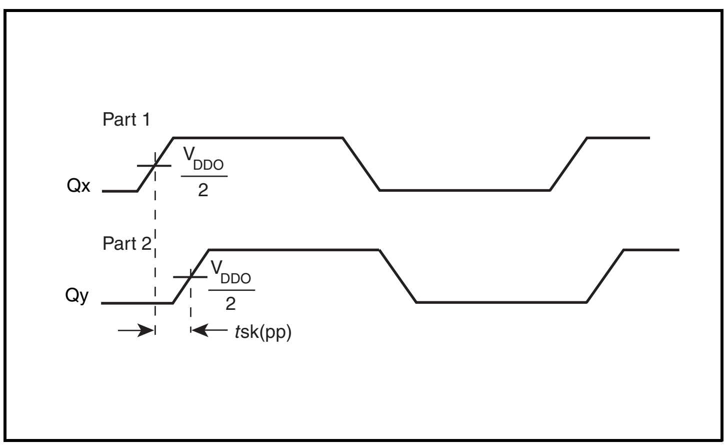
2.5V Core/2.5V LVCMOS Output Load AC Test Circuit



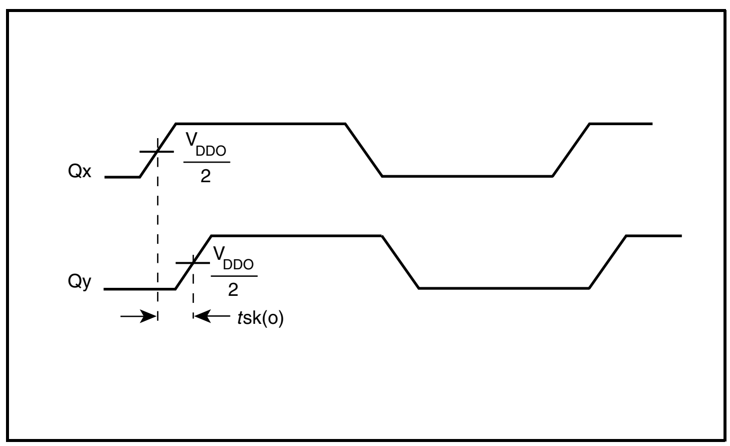
3.3V Core/2.5V LVCMOS Output Load AC Test Circuit



Differential Input Level

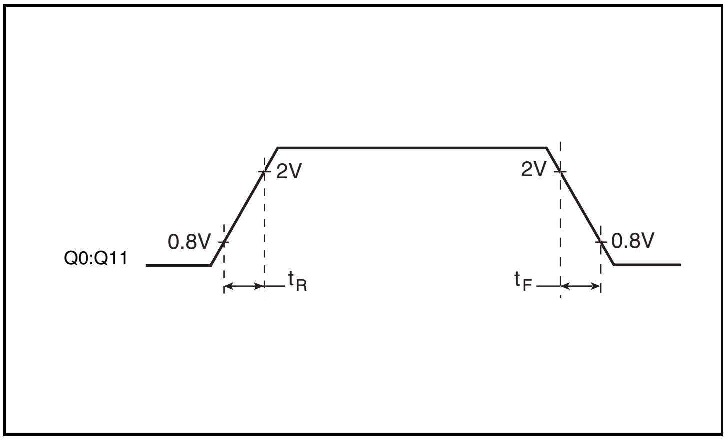


Part-to-Part Skew

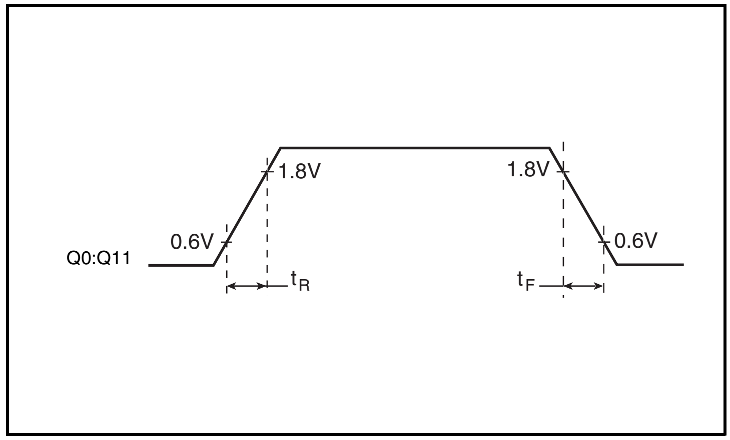


Output Skew

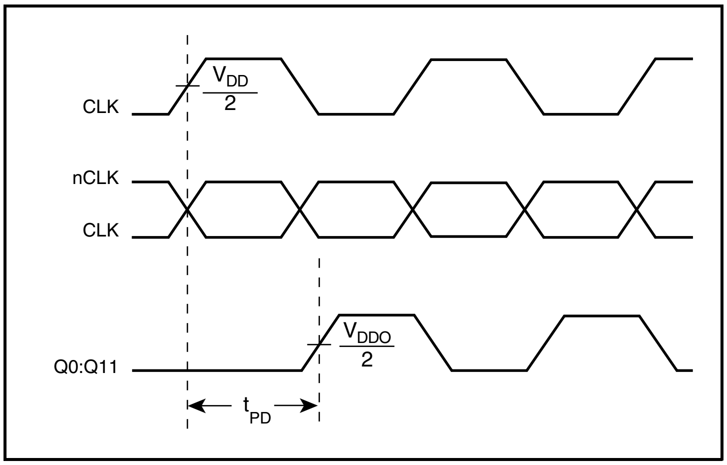
Parameter Measurement Information, continued



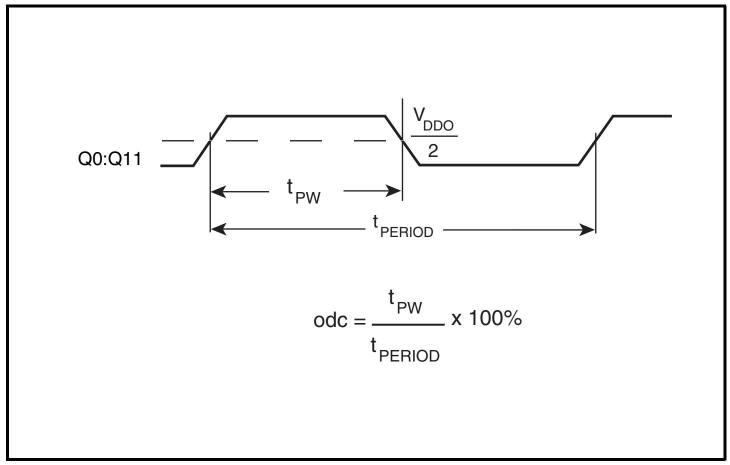
3.3V Output Rise/Fall Time



2.5V Output Rise/Fall Time



Propagation Delay



Output Duty Cycle/Pulse Width/Period

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = $V_{DD}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

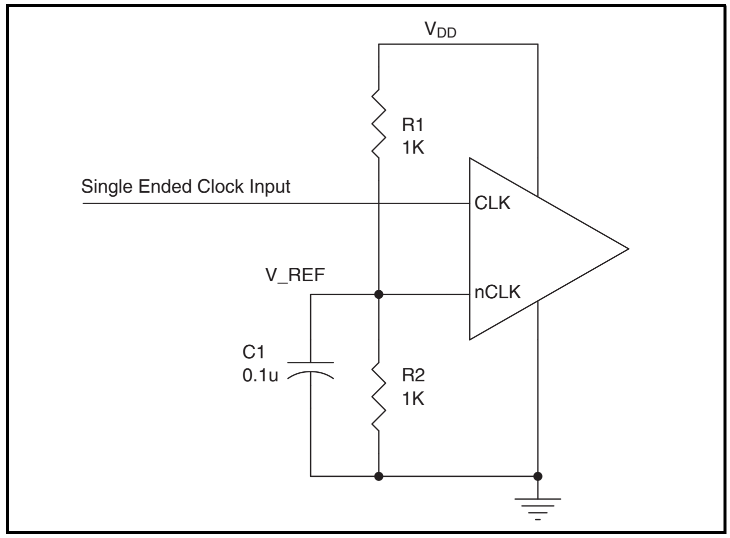


Figure 1. Single-Ended Signal Driving Differential Input

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

CLK Input

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2F* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

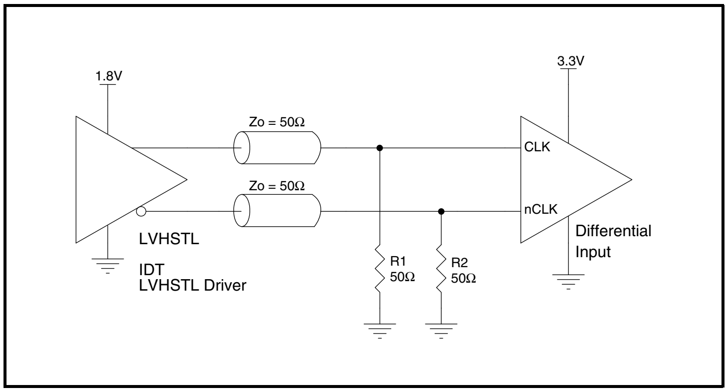


Figure 2A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

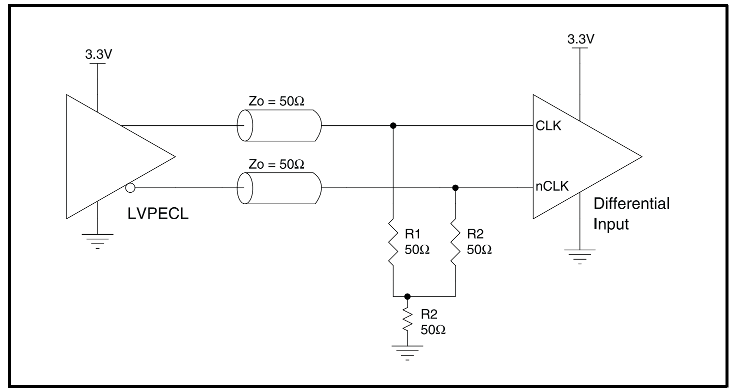


Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

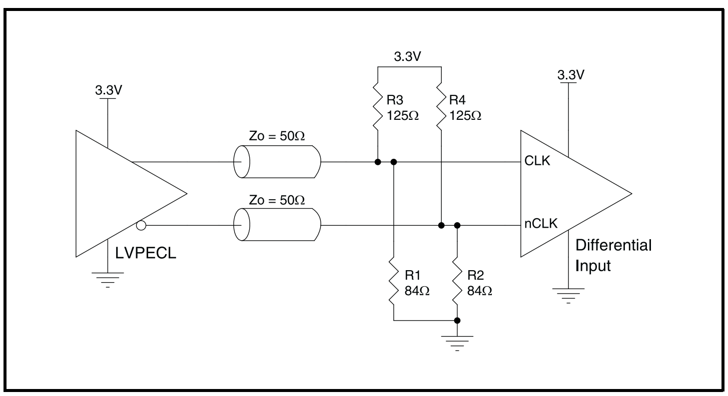


Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

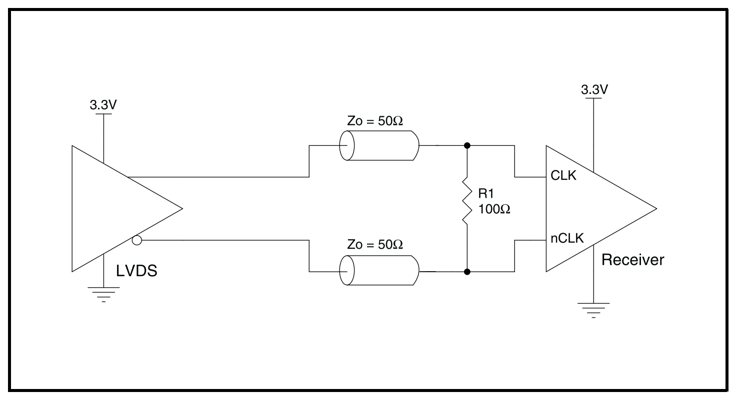


Figure 2D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

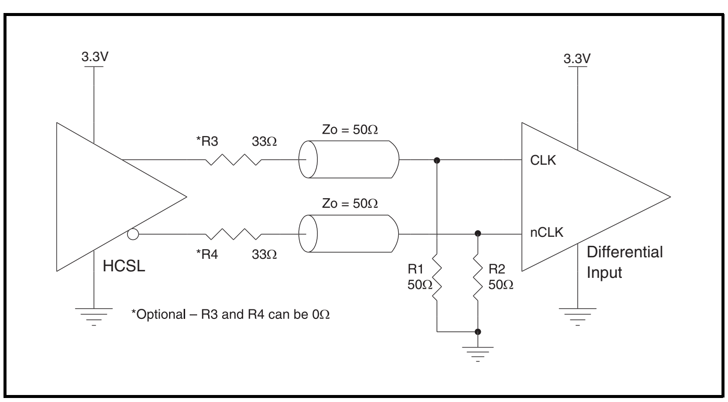


Figure 2E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

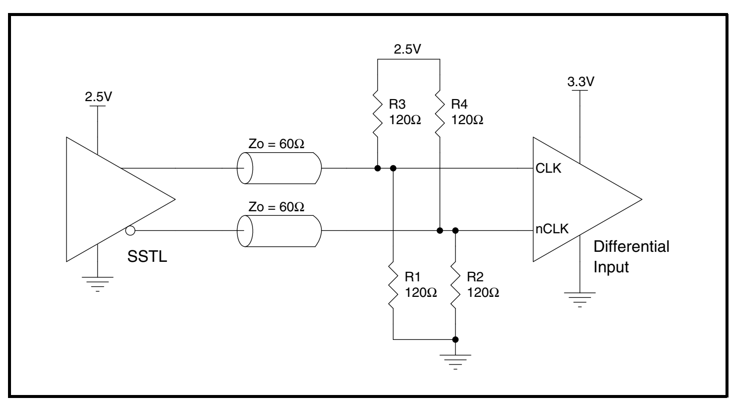


Figure 2F. CLK/nCLK Input Driven by a 2.5V SSTL Driver

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 32-Lead LQFP

θ_{JA} **vs. Air Flow**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	73.6°C/W	63.9°C/W	60.3°C/W

Transistor Count

The transistor count for 83948I-147 is: 1040
Pin compatible with the MPC9448

Package Outline and Package Dimension

Package Outline - Y Suffix for 32-Lead LQFP

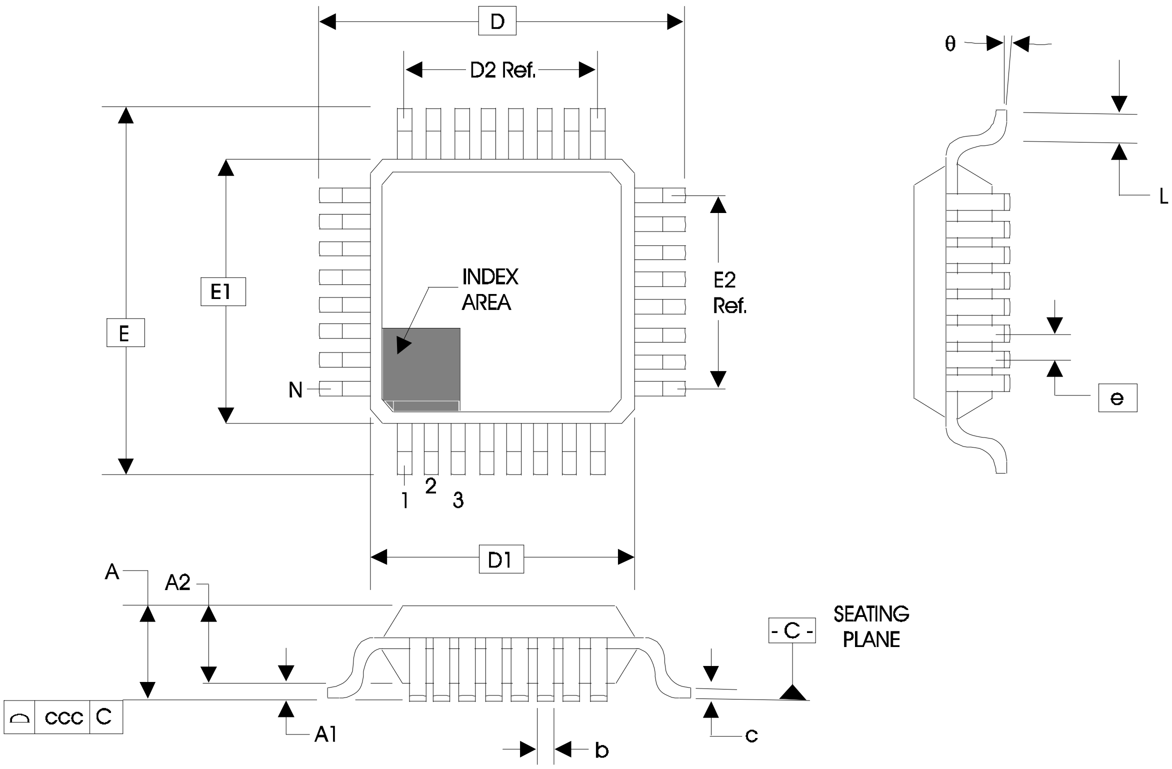


Table 7. Package Dimensions for 32-Lead LQFP

JEDEC Variation: ABC - HD All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A			1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D & E		9.00 Basic	
D1 & E1		7.00 Basic	
D2 & E2		5.60 Ref.	
e		0.80 Basic	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
83948AYI-147LF	ICS948AI147L	"Lead-Free" 32-Lead LQFP	Tray	-40°C to 85°C
83948AYI-147LFT	ICS948AI147L	"Lead-Free" 32-Lead LQFP	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	 T2 T8	1 2 7 10	Features Section - added Lead-Free bullet. Pin Characteristics Table - changed C_{IN} from 4pF max. to 4pF typical; and added 5Ω min. and 12Ω max to R_{OUT}. Updated *Single Ended Signal Driving Differential Input diagram.* Added *Recommendations for Unused Input and Output Pins.* Ordering Information Table - added lead-free part number, marking, and note.	11/21/05
C	 T5A T5B T6	1 5 6 7 11 12	Features Section - added *Additive Phase Jitter bullet.* 3.3V AC Characteristics Table - added *Additive Phase Jitter.* 3.3V AC Characteristics Table - added *Additive Phase Jitter.* Added *Additive Phase Jitter section.* Updated *Differential Input Clock Interface section.* Updated *Reliability Information.* Updated format throughout the datasheet.	1/15/08
D	 T4C T5C T8	1 4 7 9 15	Features Section - added mix voltage to supply voltage bullet. Added Mix DC Characteristics Power Supply Table. Added Mix AC Characteristics Table. Parameter Measurement Information Section - added *3.3V/2.5V LVCMOS Output Load AC Test Circuit* diagram. Ordering Information Table - deleted ICS prefix from Part/Order Number column.	4/1/09
D	T1	2	Output supply pins, Changed V_{DD} to V_{DDO}	11/1/12
D	T8	15	Removed leaded orderable parts from Ordering Information table	11/14/12
D	T8	15 17	Fixed typo: removed extra “I” from orderable part number. Updated Headers and Footers. Updated Contact information.	7/17/14
D			Removed ICS from part number where needed. Updated data sheet header and footer.	3/30/16

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