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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



## 843441-150 PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES MAY 6, 2017

### General Description

The 843441 is a low jitter, high performance clock generator. The 843441 is designed for use in applications using the SAS and SATA interconnect. The 843441 uses an external, 25MHz, parallel resonant crystal to generate four selectable output frequencies: 75MHz, 100MHz, 150MHz, and 300MHz. This silicon based approach provides excellent frequency stability and reliability. The 843441 features down and center spread spectrum (SSC) clocking techniques.

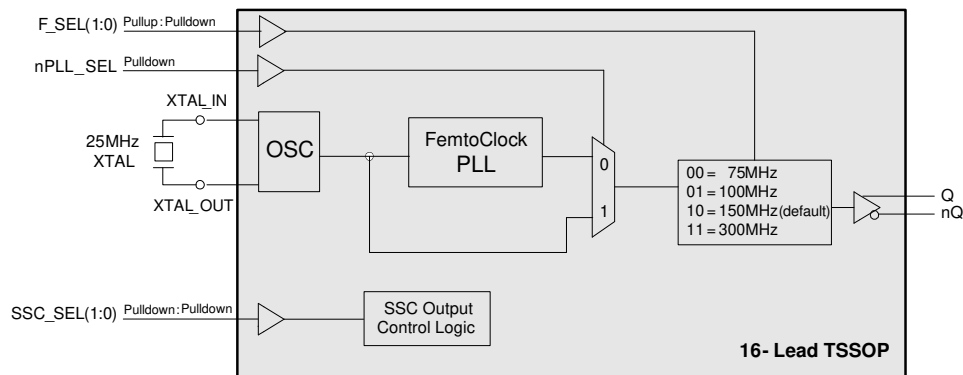
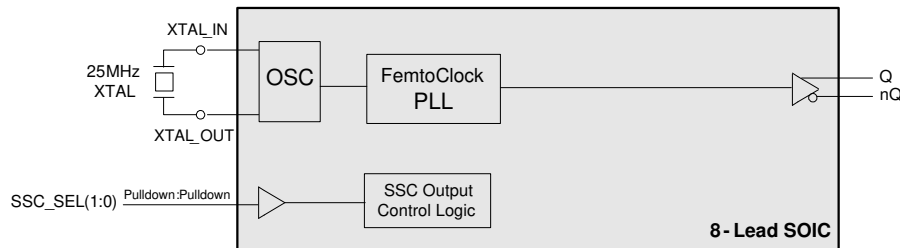
### Additional Ordering Information

| Part/Order Number | Package  | Output Frequency (MHz) |
|-------------------|----------|------------------------|
| 843441AG          | 16 TSSOP | 75, 100, 150, 300      |
| 843441AM-75       | 8 SOIC   | 75                     |
| 843441AM-100      | 8 SOIC   | 100                    |
| 843441AM-150      | 8 SOIC   | 150                    |
| 843441AM-300      | 8 SOIC   | 300                    |

### Features

- Designed for use in SAS, SAS-2, and SATA systems
- Center ( $\pm 0.33\%$ ) Spread Spectrum Clocking (SSC)
- Down ( $-0.30\%$  or  $-0.60\%$ ) SSC
- Better frequency stability than SAW oscillators
- One differential 3.3V LVPECL output
- Crystal oscillator interface designed for 25MHz ( $C_L = 18\text{pF}$ ) frequency
- External fundamental crystal frequency ensures high reliability and low aging
- Selectable output frequencies: 75MHz, 100MHz, 150MHz, 300MHz
- Output frequency is tunable with external capacitors
- RMS phase jitter: 1.33ps (typical)
- 3.3V operating supply
- $0^\circ\text{C}$  to  $70^\circ\text{C}$  ambient operating temperature
- Industrial temperature available upon request
- Available in lead-free (RoHS 6) package
- 843441-150 Functional replacement part use 8T49N242i

### Block Diagrams

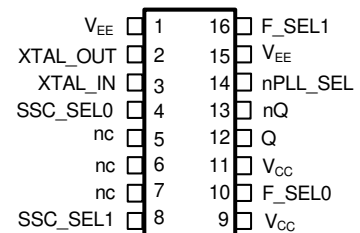


### Pin Assignments



**843441**

**8-Lead SOIC, 150 Mil**  
**3.90mm x 4.90mm x 1.375mm package body**  
**M Package**  
**Top View**



**843441**

**16-Lead TSSOP**  
**4.4mm x 5.0mm x 0.925mm package body**  
**G Package**  
**Top View**

**Table 1A. Pin Descriptions (SOIC Package)**

| Number  | Name                  | Type   |          | Description   |
|---------|-----------------------|--------|----------|---|
| 1,<br>2 | XTAL_OUT,<br>XTAL_IN  | Input  | Pullup   | Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output. |
| 3,<br>4 | SSC_SEL0,<br>SSC_SEL1 | Input  | Pulldown | SSC select pins. See Table 3A. LVCMOS/LVTTL interface levels.               |
| 5       | V <sub>CC</sub>       | Power  |          | Power supply pin.   |
| 6, 7    | Q, nQ                 | Output |          | Differential clock outputs. LVPECL interface levels.                        |
| 8       | V <sub>EE</sub>       | Power  |          | Negative supply pin.  |

NOTE: Pullup/Pulldown refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 1B. Pin Descriptions (TSSOP Package)**

| Number  | Name                  | Type   |          | Description   |
|---------|-----------------------|--------|----------|---|
| 1, 15   | V <sub>EE</sub>       | Power  |          | Negative supply pins.   |
| 2,<br>3 | XTAL_OUT,<br>XTAL_IN  | Input  | Pullup   | Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output. |
| 4,<br>8 | SSC_SEL0,<br>SSC_SEL1 | Input  | Pulldown | SSC select pins. See Table 3A. LVCMOS/LVTTL interface levels.               |
| 5, 6, 7 | nc                    | Unused |          | No connect pins.  |
| 9, 11   | V <sub>CC</sub>       | Power  |          | Power supply pins.  |
| 10      | F_SEL0                | Input  | Pulldown | Output frequency select pin. See Table 3B. LVCMOS/LVTTL interface levels.   |
| 12, 13  | Q, nQ                 | Output |          | Differential clock outputs. LVPECL interface levels.                        |
| 14      | nPLL_SEL              | Input  | Pulldown | PLL Bypass pin. LVCMOS/LVTTL interface levels.                              |
| 16      | F_SEL1                | Input  | Pullup   | Output frequency select pin. See Table 3B. LVCMOS/LVTTL interface levels.   |

NOTE: Pullup/Pulldown refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

| Symbol                | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance       |                 |         | 4       |         | pF    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor |                 |         | 51      |         | kΩ    |
| R <sub>PULLUP</sub>   | Input Pullup Resistor   |                 |         | 51      |         | kΩ    |

## Function Tables

**Table 3A. SSC\_SEL[1:0] Function Table**

| Inputs      |             | Mode                |
|-------------|-------------|---------------------|
| SSC_SEL1    | SSC_SEL0    |                     |
| 0 (default) | 0 (default) | SSC Off             |
| 0           | 1           | 0.60% Down-spread   |
| 1           | 0           | 0.30% Down-spread   |
| 1           | 1           | 0.33% Center-spread |

**Table 3B. F\_SEL[1:0] Function Table**

| Inputs      |             | Output Frequency (MHz) |
|-------------|-------------|------------------------|
| F_SEL1      | F_SEL0      |                        |
| 0           | 0           | 75                     |
| 0           | 1           | 100                    |
| 1 (default) | 0 (default) | 150                    |
| 1           | 1           | 300                    |

Table 3B applicable only for 16 Lead TSSOP package.



## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item   | Rating                                     |
|--|--|
| Supply Voltage, $V_{CC}$   | 4.6V                                       |
| Inputs, $V_I$ , (LVCMOS)<br>XTAL_IN<br>Other Inputs                      | 0V to $V_{CC}$<br>-0.5V to $V_{CC} + 0.5V$ |
| Outputs, $I_O$<br>Continuous Current<br>Surge Current                    | 50mA<br>100mA                              |
| Package Thermal Impedance, $\theta_{JA}$<br>16 Lead TSSOP<br>8 Lead SOIC | 81.2°C/W (0 mps)<br>96.0°C/W (0 lfpm)      |
| Storage Temperature, $T_{STG}$   | -65°C to 150°C                             |

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

| Symbol   | Parameter            | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|----------------------|-----------------|---------|---------|---------|-------|
| $V_{CC}$ | Power Supply Voltage |                 | 3.135   | 3.3     | 3.465   | V     |
| $I_{EE}$ | Power Supply Current |                 |         |         | 66      | mA    |

**Table 4B. LVCMOS/LVTTL DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

| Symbol   | Parameter          | Test Conditions                   | Minimum                        | Typical | Maximum        | Units   |
|----------|--------------------|-----------------------------------|--------------------------------|---------|----------------|---------|
| $V_{IH}$ | Input High Voltage |                                   | 2                              |         | $V_{DD} + 0.3$ | V       |
| $V_{IL}$ | Input Low Voltage  |                                   | -0.3                           |         | 0.8            | V       |
| $I_{IH}$ | Input High Current | F_SEL1                            | $V_{CC} = V_{IN} = 3.465V$     |         | 5              | $\mu A$ |
|          |                    | SSC_SEL[0:1],<br>F_SEL0, nPLL_SEL | $V_{CC} = V_{IN} = 3.465V$     |         | 150            | $\mu A$ |
| $I_{IL}$ | Input Low Current  | F_SEL1                            | $V_{CC} = 3.465V, V_{IN} = 0V$ | -150    |                | $\mu A$ |
|          |                    | SSC_SEL[0:1],<br>F_SEL0, nPLL_SEL | $V_{CC} = 3.465V, V_{IN} = 0V$ | -5      |                | $\mu A$ |

**Table 4C. LVPECL DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

| Symbol      | Parameter                         | Test Conditions | Minimum        | Typical | Maximum        | Units |
|-------------|-----------------------------------|-----------------|----------------|---------|----------------|-------|
| $V_{OH}$    | Output High Voltage; NOTE 1       |                 | $V_{CC} - 1.4$ |         | $V_{CC} - 0.9$ | V     |
| $V_{OL}$    | Output Low Voltage; NOTE 1        |                 | $V_{CC} - 2.0$ |         | $V_{CC} - 1.7$ | V     |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing |                 | 0.6            |         | 0.9            | V     |

NOTE 1: Output termination with  $50\Omega$  to  $V_{CC} - 2V$ .

## AC Electrical Characteristics

**Table 5. AC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

| Symbol               | Parameter                         | Test Conditions                             | Minimum | Typical | Maximum | Units |
|----------------------|-----------------------------------|---|---------|---------|---------|-------|
| $f_{OUT}$            | Output Frequency                  | F_SEL(1:0) = 00                             |         | 75      |         | MHz   |
|                      |                                   | F_SEL(1:0) = 01                             |         | 100     |         | MHz   |
|                      |                                   | F_SEL(1:0) = 10                             |         | 150     |         | MHz   |
|                      |                                   | F_SEL(1:0) = 11                             |         | 300     |         | MHz   |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter (Random); NOTE 1 | 75MHz,<br>Integration Range: 12kHz – 20 MHz |         | 1.33    |         | ps    |
|                      |                                   | 100MHz,<br>Integration Range: 12kHz – 20MHz |         | 1.39    |         | ps    |
|                      |                                   | 150MHz,<br>Integration Range: 12kHz – 20MHz |         | 1.36    |         | ps    |
|                      |                                   | 300MHz,<br>Integration Range: 12kHz – 20MHz |         | 1.37    |         | ps    |
| $f_{jit}(per)$       | Period Jitter, RMS; NOTE 2, 3     | 75MHz, SSC Off                              |         | 4.15    |         | ps    |
|                      |                                   | 100MHz, SSC Off                             |         | 4.05    |         | ps    |
|                      |                                   | 150MHz, SSC Off                             |         | 4.15    |         | ps    |
|                      |                                   | 300MHz, SSC Off                             |         | 4.25    |         | ps    |
| $f_{jit}(cc)$        | Cycle-to-Cycle Jitter: NOTE 3     | 75MHz, SSC Off                              |         |         | 31      | ps    |
|                      |                                   | 100MHz, SSC Off                             |         |         | 31      | ps    |
|                      |                                   | 150MHz, SSC Off                             |         |         | 31      | ps    |
|                      |                                   | 300MHz, SSC Off                             |         |         | 31      | ps    |
| $t_R / t_F$          | Output Rise/Fall Time             | 20% to 80%                                  | 200     |         | 700     | ps    |
| odc                  | Output Duty Cycle                 |   | 45      |         | 55      | %     |

NOTE: Using a 25MHz, 18pF quartz crystal.

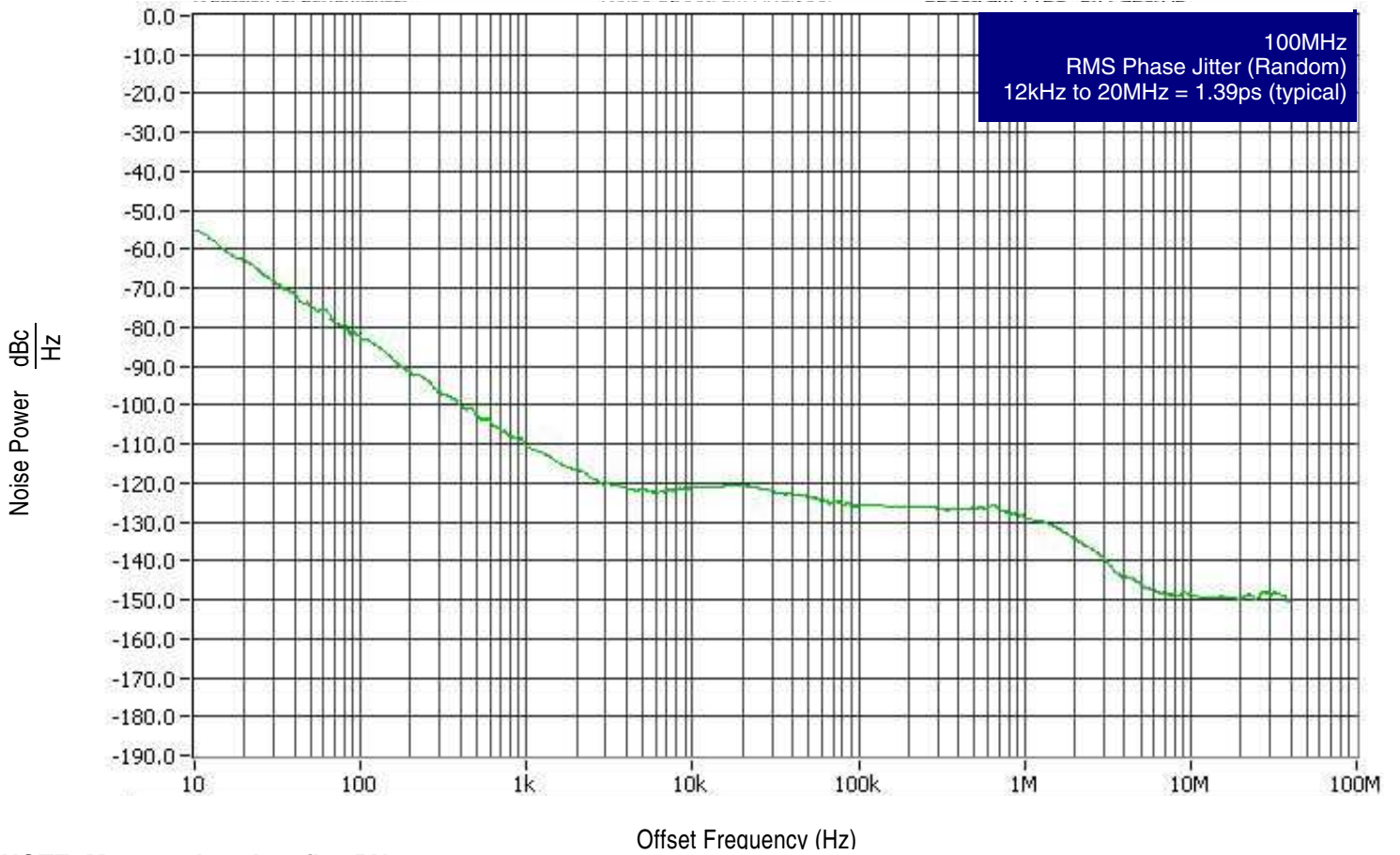
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Please refer to the Phase Noise plots.

NOTE 2: Refer to Application Section for peak-to-peak jitter calculations.

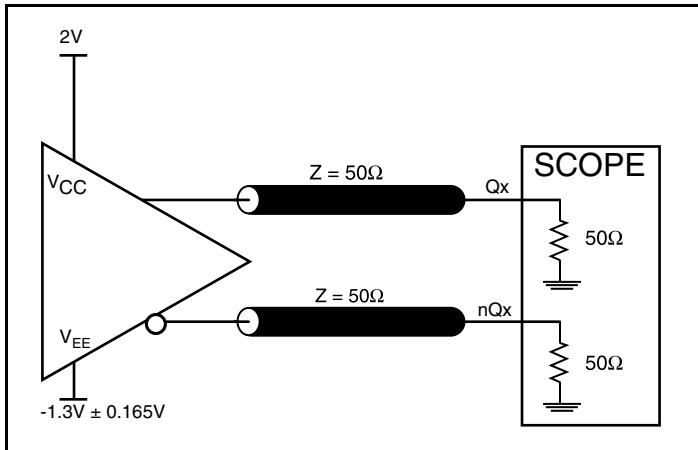
NOTE 3: Tested per JEDEC 65B.

### Typical Phase Noise at 100MHz

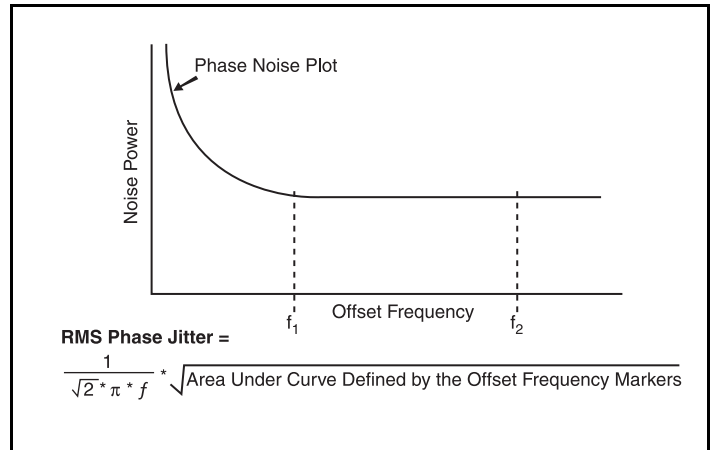


**NOTE: Measured on Aeroflex PN9000**

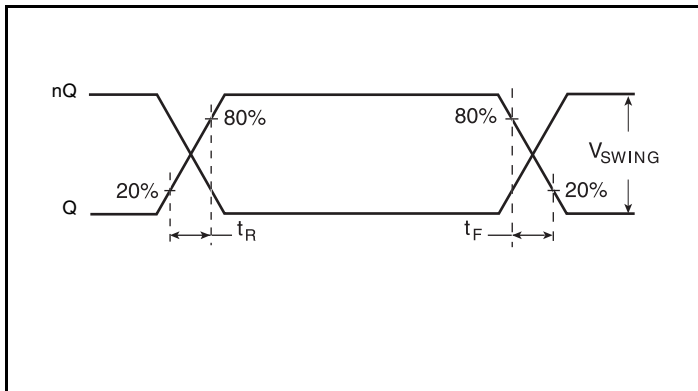
### Parameter Measurement Information



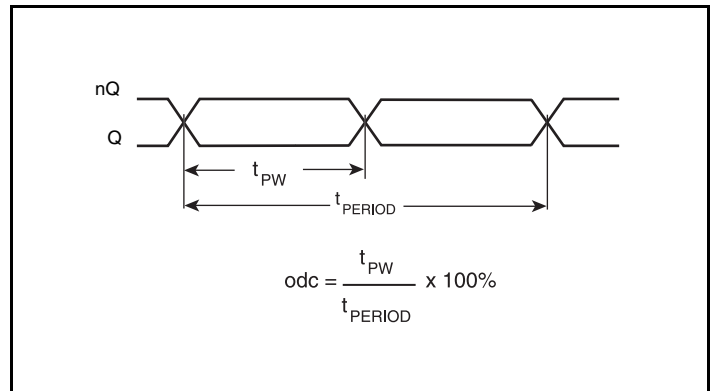
3.3V LVPECL Output Load AC Test Circuit



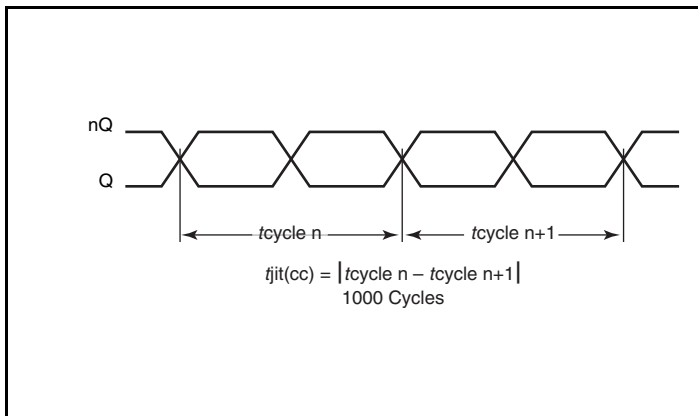
RMS Phase Jitter



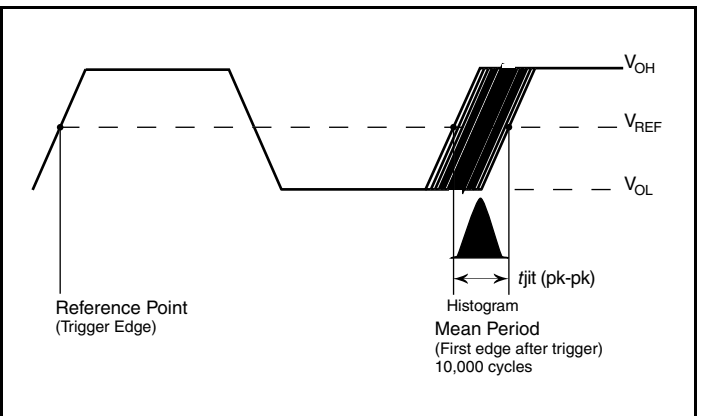
Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period



Cycle-to-Cycle Jitter



RMS Period Jitter, Peak-to-Peak



## Applications Information

### Recommendations for Unused Input Pins

#### Inputs:

##### LVC MOS Control Pins

All control pins have internal pullups and pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### Overdriving the XTAL Interface

The XTAL\_IN input can accept a single-ended LVC MOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 1A*. The XTAL\_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission line impedance. In addition,

matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most 50Ω applications,  $R_1$  and  $R_2$  can be 100Ω. This can also be accomplished by removing  $R_1$  and making  $R_2$  50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

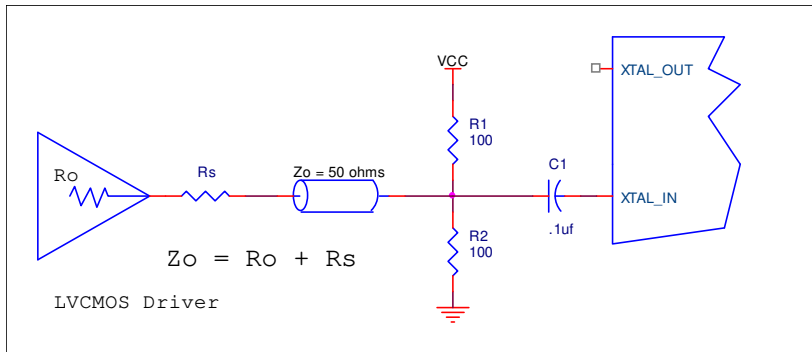
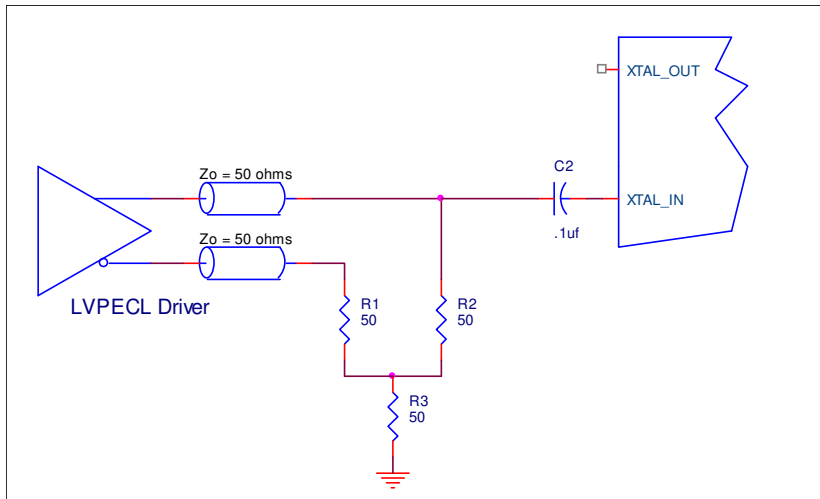


Figure 1A. General Diagram for LVC MOS Driver to XTAL Input Interface



**Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface**

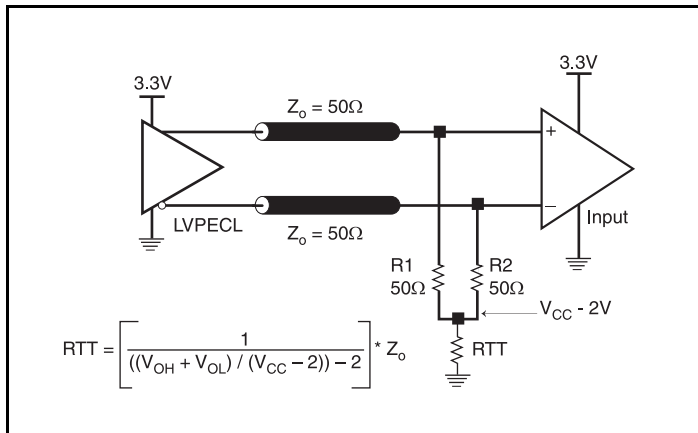
**Termination for 3.3V LVPECL Outputs**

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

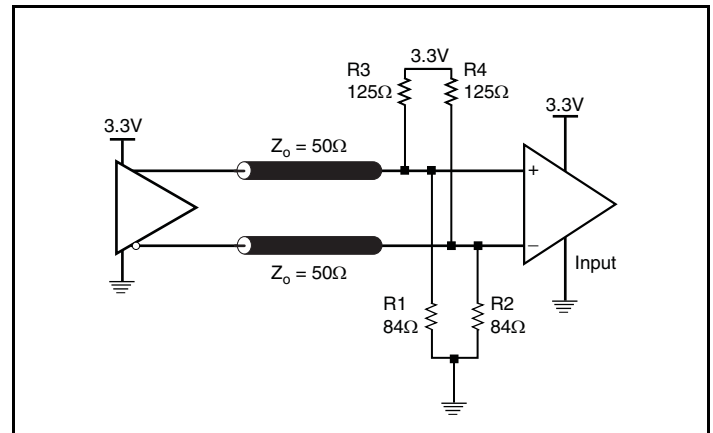
The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.

*Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.



**Figure 2A. 3.3V LVPECL Output Termination**



**Figure 2B. 3.3V LVPECL Output Termination**

### Schematic Example

Figure 3 shows an example of 843441 application schematic. In this example, the device is operated at  $V_{CC} = 3.3V$ . An 18pF parallel resonant 25MHz crystal is used. The load capacitance  $C1 = 27pF$  and  $C2 = 27pF$  are recommended for frequency accuracy. Depending on the parasitics of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will required adjusting C1 and C2.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 843441 provides separate power supplies to isolate noise from coupling into the internal PLL. In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1μF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on

the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitances in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

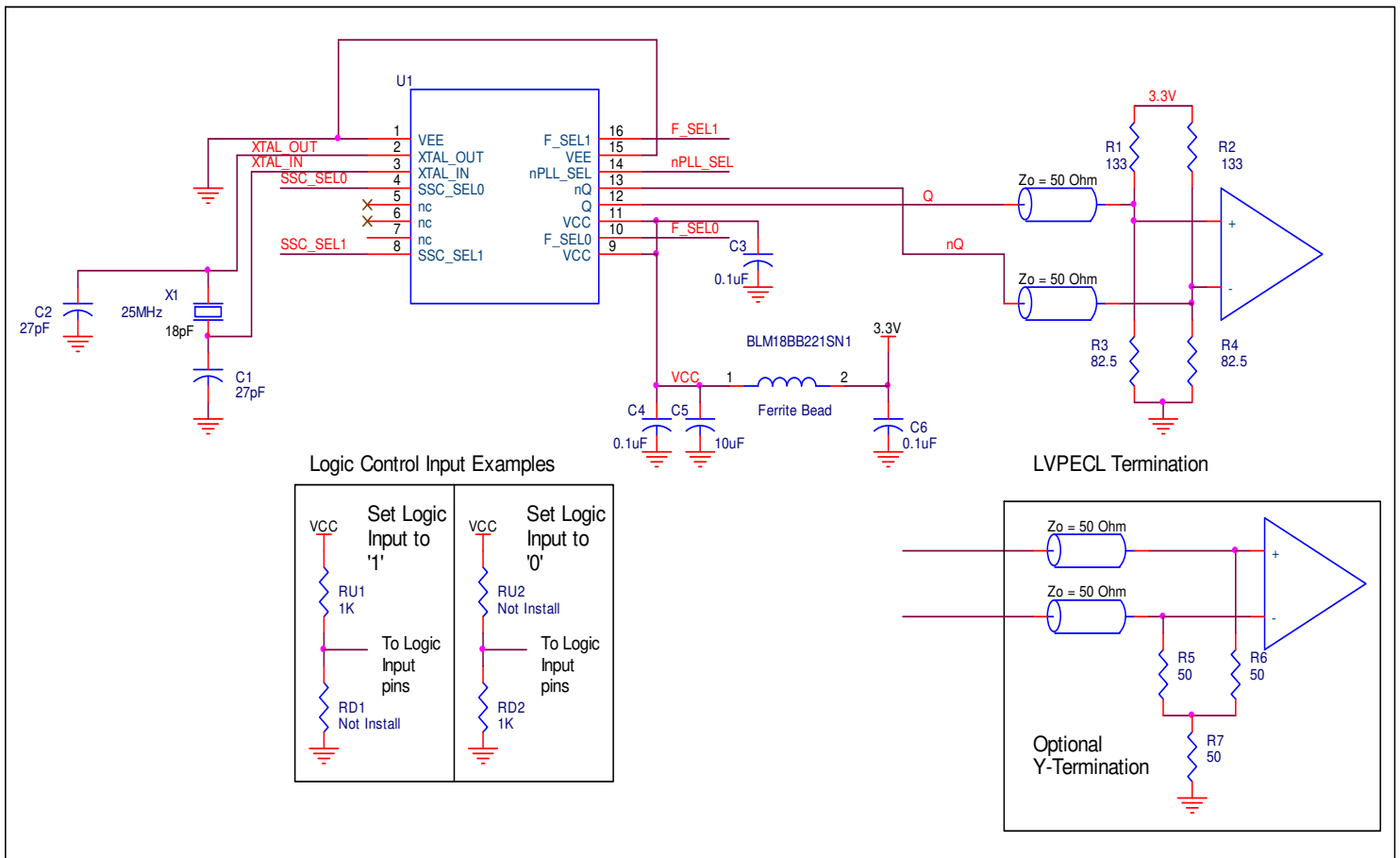


Figure 3. 843441 Schematic Example

## Peak-to-Peak Jitter Calculations

A standard deviation of a statistical population or data set is the square root of its variance. A standard deviation is used to calculate the probability of an anomaly or to predict a failure. Many times, the term "root mean square" (RMS) is used synonymously for standard deviation. This is accurate when referring to the square root of the mean squared deviation of a signal from a given baseline and the data set contains a Gaussian distribution with no deterministic components. A low standard deviation indicates that the data set tends to be close to the mean with little variation. A large standard deviation indicates that the data set is spread out and has a large variation from the mean.

A standard deviation is required when calculating peak-to-peak jitter. Since true peak-to-peak jitter is random and unbounded, it is important to always associate a bit error ratio (BER) when specifying a peak-to-peak jitter limit. Without it, the specification is meaningless. Given that a BER is application specific, many frequency timing devices specify jitter as an RMS. This allows the peak-to-peak jitter to be calculated for the specific application and

BER requirement. Because a standard deviation is the variation from the mean of the data set, it is important to always calculate the peak-to-peak jitter using the typical RMS value.

The table shows the BER with its appropriate RMS Multiplier. Once the BER is chosen, the peak to peak jitter can be calculated by simply multiplying the RMS multiplier with the typical RMS datasheet specification. For example, if a  $10^{-12}$  BER is required, multiply 14.260 times the typical jitter specification.

Jitter (peak-to-peak) = RMS Multiplier x RMS (typical)

This calculation is not specific to one type of Jitter classification. It can be used to calculate BER on various types of RMS jitter. It is important that the user understands their jitter requirement to ensure they are calculating the correct BER for their jitter requirement.

| BER        | RMS Multiplier |
|------------|----------------|
| $10^{-3}$  | 6.582          |
| $10^{-4}$  | 7.782          |
| $10^{-5}$  | 8.834          |
| $10^{-6}$  | 9.784          |
| $10^{-7}$  | 10.654         |
| $10^{-8}$  | 11.462         |
| $10^{-9}$  | 12.218         |
| $10^{-10}$ | 12.934         |
| $10^{-11}$ | 13.614         |
| $10^{-12}$ | 14.260         |
| $10^{-13}$ | 14.882         |
| $10^{-14}$ | 15.478         |
| $10^{-15}$ | 16.028         |

## Power Considerations

This section provides information on power dissipation and junction temperature for the 843441. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 843441 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 66mA = \mathbf{228.69mW}$
- Power (outputs)<sub>MAX</sub> = **30mW/Loaded Output pair**

**Total Power<sub>MAX</sub>** (3.465V, with all outputs switching) = 228.69mW + 30mW = **258.69mW**

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 96°C/W per Table 6B below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$70^\circ C + 0.259W * 96^\circ C/W = 94.864^\circ C$ . This is below the limit of 125°C.

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 6A. Thermal Resistance  $\theta_{JA}$  for 16 Lead TSSOP, Forced Convection**

| $\theta_{JA}$ vs. Air Flow                  |          |          |          |
|---|----------|----------|----------|
| Meters per Second                           | 0        | 1        | 2.5      |
| Multi-Layer PCB, JEDEC Standard Test Boards | 81.2°C/W | 73.9°C/W | 70.2°C/W |

**Table 6B. Thermal Resistance  $\theta_{JA}$  for 8 Lead SOIC, Forced Convection**

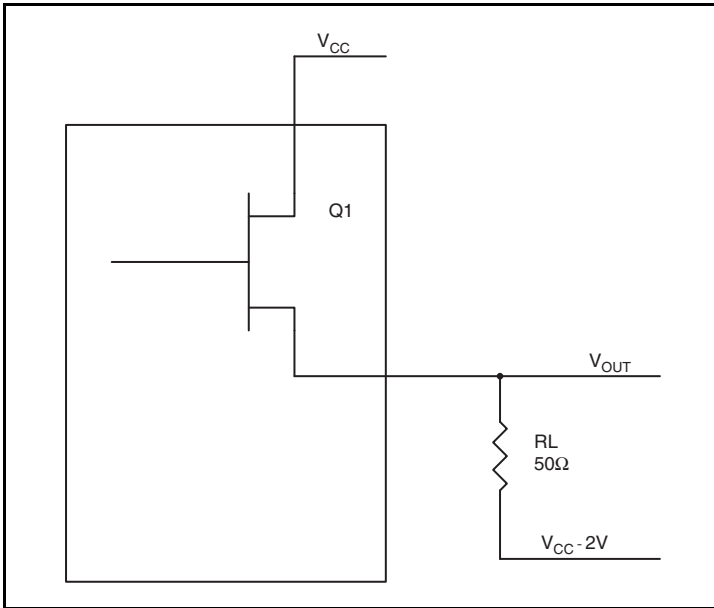
| $\theta_{JA}$ vs. Air Flow                  |        |        |        |
|---|--------|--------|--------|
| Linear Feet per Second                      | 0      | 200    | 500    |
| Multi-Layer PCB, JEDEC Standard Test Boards | 96°C/W | 87°C/W | 82°C/W |



### 3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 4*.



**Figure 4. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V<sub>CC</sub> - 2V.

- For logic high, V<sub>OUT</sub> = V<sub>OH\_MAX</sub> = V<sub>CC\_MAX</sub> - 0.9V  
(V<sub>CC\_MAX</sub> - V<sub>OH\_MAX</sub>) = **0.9V**
- For logic low, V<sub>OUT</sub> = V<sub>OL\_MAX</sub> = V<sub>CC\_MAX</sub> - 1.7V  
(V<sub>CC\_MAX</sub> - V<sub>OL\_MAX</sub>) = **1.7V**

Pd<sub>H</sub> is power dissipation when the output drives high.

Pd<sub>L</sub> is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$$

$$Pd_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$$

Total Power Dissipation per output pair = Pd<sub>H</sub> + Pd<sub>L</sub> = **30mW**

## Reliability Information

**Table 7A.  $\theta_{JA}$  vs. Air Flow Table for a 16 Lead TSSOP**

| $\theta_{JA}$ vs. Air Flow                  |          |          |          |
|---|----------|----------|----------|
| Meters per Second                           | 0        | 1        | 2.5      |
| Multi-Layer PCB, JEDEC Standard Test Boards | 81.2°C/W | 73.9°C/W | 70.2°C/W |

**Table 7B.  $\theta_{JA}$  vs. Air Flow Table for a 8 Lead SOIC**

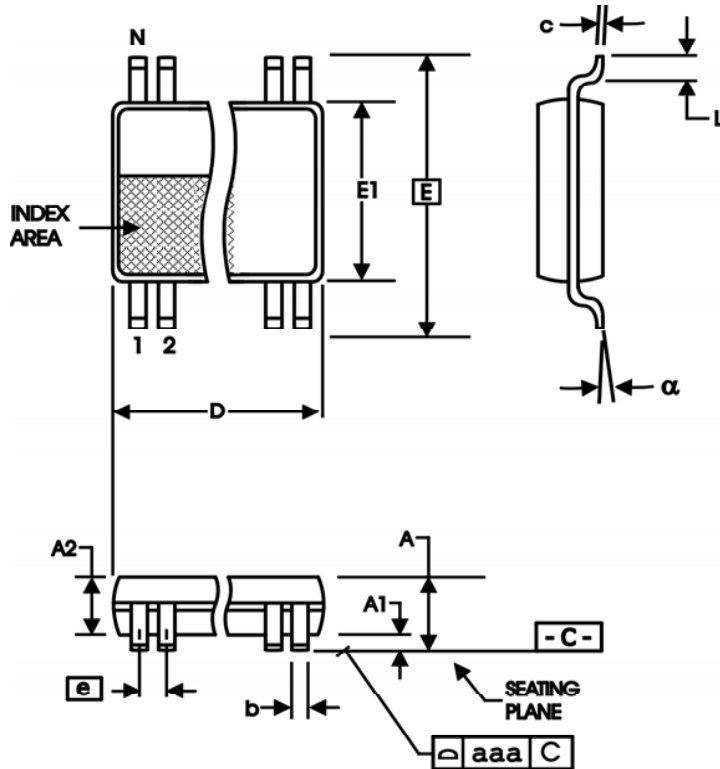
| $\theta_{JA}$ vs. Air Flow                  |        |        |        |
|---|--------|--------|--------|
| Linear Feet per Second                      | 0      | 200    | 500    |
| Multi-Layer PCB, JEDEC Standard Test Boards | 96°C/W | 87°C/W | 82°C/W |

## Transistor Count

The transistor count for 843441 is: 6303

## Package Outline and Package Dimensions

Package Outline - G Suffix for 16-Lead TSSOP



Package Outline - M Suffix for 8 Lead SOIC

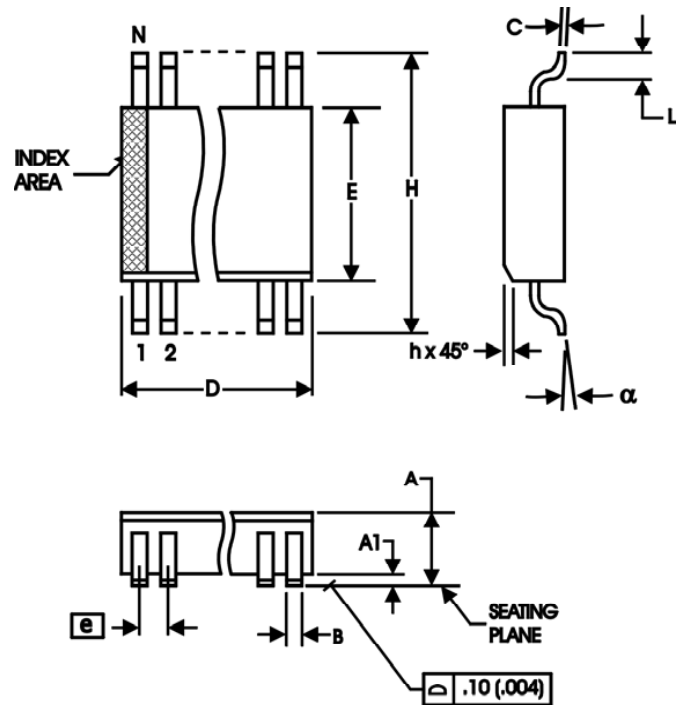


Table 8A. Package Dimensions for 16 Lead TSSOP

| All Dimensions in Millimeters |            |         |
|-------------------------------|------------|---------|
| Symbol                        | Minimum    | Maximum |
| N                             | 16         |         |
| A                             |            | 1.20    |
| A1                            | 0.05       | 0.15    |
| A2                            | 0.80       | 1.05    |
| b                             | 0.19       | 0.30    |
| c                             | 0.09       | 0.20    |
| D                             | 4.90       | 5.10    |
| E                             | 6.40 Basic |         |
| E1                            | 4.30       | 4.50    |
| e                             | 0.65 Basic |         |
| L                             | 0.45       | 0.75    |
| α                             | 0°         | 8°      |
| aaa                           |            | 0.10    |

Reference Document: JEDEC Publication 95, MO-153

Table 8B. Package Dimensions for 8 Lead SOIC

| All Dimensions in Millimeters |            |         |
|-------------------------------|------------|---------|
| Symbol                        | Minimum    | Maximum |
| N                             | 8          |         |
| A                             | 1.35       | 1.75    |
| A1                            | 0.10       | 0.25    |
| B                             | 0.33       | 0.51    |
| C                             | 0.19       | 0.25    |
| D                             | 4.80       | 5.00    |
| E                             | 3.80       | 4.00    |
| e                             | 1.27 Basic |         |
| H                             | 5.80       | 6.20    |
| h                             | 0.25       | 0.50    |
| L                             | 0.40       | 1.27    |
| α                             | 0°         | 8°      |

Reference Document: JEDEC Publication 95, MS-012

## Ordering Information

Table 9. Ordering Information

| Part/Order Number | Marking  | Package                   | Shipping Packaging | Temperature |
|-------------------|----------|---------------------------|--------------------|-------------|
| 843441AGLF        | 843441AL | 16 Lead "Lead-Free" TSSOP | Tube               | 0°C to 70°C |
| 843441AGLFT       | 843441AL | 16 Lead "Lead-Free" TSSOP | Tape & Reel        | 0°C to 70°C |
| 843441AM-75LF     | 3441A75L | 8 Lead "Lead-Free" SOIC   | Tube               | 0°C to 70°C |
| 843441AM-75LFT    | 3441A75L | 8 Lead "Lead-Free" SOIC   | Tape & Reel        | 0°C to 70°C |
| 843441AM-100LF    | 441A100L | 8 Lead "Lead-Free" SOIC   | Tube               | 0°C to 70°C |
| 843441AM-100LFT   | 441A100L | 8 Lead "Lead-Free" SOIC   | Tape & Reel        | 0°C to 70°C |
| 843441AM-150LF    | 441A150L | 8 Lead "Lead-Free" SOIC   | Tube               | 0°C to 70°C |
| 843441AM-150LFT   | 441A150L | 8 Lead "Lead-Free" SOIC   | Tape & Reel        | 0°C to 70°C |
| 843441AM-300LF    | 441A300L | 8 Lead "Lead-Free" SOIC   | Tube               | 0°C to 70°C |
| 843441AM-300LFT   | 441A300L | 8 Lead "Lead-Free" SOIC   | Tape & Reel        | 0°C to 70°C |

## Revision History Sheet

| Rev | Table | Page | Description of Change  | Date    |
|-----|-------|------|--|---------|
| A   | T3A   | 3    | SSC_SEL Function Table - updated Mode column.  | 5/18/11 |
| A   | T9    | 16   | Ordering Information - Removed quantity in tape and reel. Deleted LF note below table.<br>Removed ICS from part number where needed.<br>Product Discontinuation Notice - Last time buy expires May 6, 2017.<br>PDN CQ-16-01<br>Updated header and footer | 6/30/16 |



**Corporate Headquarters**

6024 Silver Creek Valley Road  
San Jose, CA 95138 USA  
[www.IDT.com](http://www.IDT.com)

**Sales**

1-800-345-7015 or 408-284-8200  
Fax: 408-284-2775  
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