Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

LOW SKEW, 1-TO-2, DIFFERENTIAL-TO-3.3V, 5V LVPECL FANOUT BUFFER

ICS853016

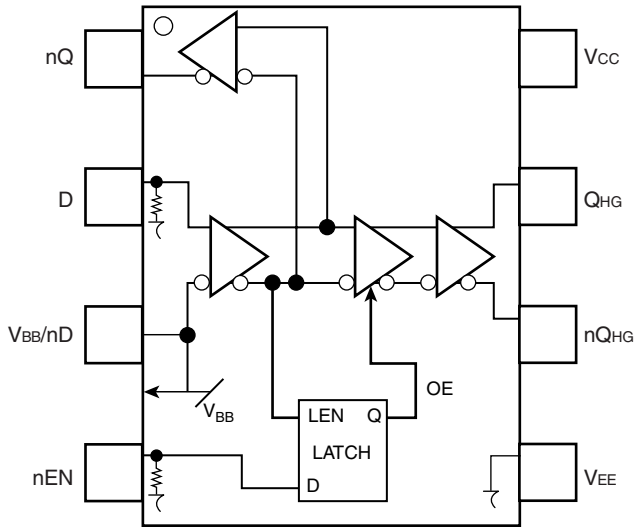
General Description

The ICS853016 is a low skew, high performance 1-to-2 Differential-to-3.3V, 5V LVPECL/ECL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS853016 is characterized to operate from either a 3.3V or a 5V power supply. Guaranteed duty cycle skew characteristic makes the ICS853016 ideal for those clock distribution applications demanding well defined performance and repeatability.

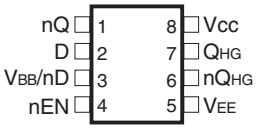
Features

- One differential 3.3V, 5V LVPECL / ECL output pair and One single-ended 3.3V, 5V LVPECL / ECL output
- One differential D, nD input pair
- D, nD pair can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Output frequency: >3GHz (typical)
- Translates any single ended input signal to 3.3V to 5V LVPECL levels with resistor bias on nD input
- Duty cycle skew: 10ps (typical)
- Propagation delay: 400ps (typical)
- LVPECL mode operating voltage supply range: V_{CC} = 3.0V to 5.5V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -5.5V to -3.0V
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS853016
8-Lead SOIC
3.90mm x 4.90mm x 1.37mm package body
M Package
Top View

ICS853016
8-Lead TSSOP, 118mil
3mm x 3mm x 0.95mm package body
G Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	nQ	Output		Single-ended clock output. LVPECL interface levels.
2	D	Input	Pulldown	Non-inverting differential clock input. LVPECL interface levels.
3	V_{BB}/nD	Input		Reference voltage output/Inverting differential clock input. LVPECL interface levels.
4	nEN	Input	Pulldown	Enable input. Default LOW when left open. LVCMOS/LVTTL interface levels.
5	V_{EE}	Power		Negative supply pin.
6, 7	nQ_{HG}, Q_{HG}	Output		Differential clock outputs. LVPECL interface levels.
8	V_{CC}	Power		Positive supply pin.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Input Pulldown Resistor			75		kΩ

Absolute Maximum Ratings

Supply Voltage, V_{CC}	6V (LVPECL mode, V_{EE} = 0)
Negative Supply Voltage, V_{EE}	-6V (ECL mode, V_{CC} = 0)
Inputs, V_I (LVPECL mode)	-0.5V to V_{CC} + 0.5 V
Inputs, V_I (ECL mode)	0.5V to V_{EE} - 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
V_{BB} Sink/Source, I_{BB}	± 0.5mA
Operating Temperature Range, T_A	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient) for 8 Lead SOIC	112.7°C/W (0 lfpm)
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient) for 8 Lead TSSOP	101.7°C/W (0 m/s)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3A. Power Supply DC Characteristics, V_{CC} = 3.0V to 5.5V; V_{EE} = 0V

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.0	3.3	5.5	V
I_{EE}	Power Supply Current			30		mA

Table 3B. LVPECL DC Characteristics, V_{CC} = 3.3V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		2.175	2.275	2.38	2.225	2.295	2.37	2.295	2.33	2.365	V
V_{OL}	Output Low Voltage; NOTE 1		1.405	1.545	1.68	1.425	1.52	1.615	1.44	1.535	1.63	V
V_{IH}	Input High Voltage (Single-Ended)		2.075		2.36	2.075		2.36	2.075		2.36	V
V_{IL}	Input Low Voltage (Single-Ended)		1.43		1.765	1.43		1.765	1.43		1.765	V
V_{BB}	Output Voltage Reference; NOTE 2		1.86		1.98	1.86		1.98	1.86		1.98	V
V_{PP}	Peak-to-Peak Input Voltage		150	800	1200	150	800	1200	150	800	1200	mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3, 4		1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input High Current	D			200			200			200	µA
I_{IL}	Input Low Current	D	-10			-10			-10			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.
NOTE 2: Single-ended input operation is limited. $V_{CC} \geq$ 3V in LVPECL mode.
NOTE 3: Common mode voltage is defined as V_{IH}.
NOTE 4: For single-ended applications, the maximum input voltage for D is V_{CC} + 0.3V.

TABLE 3C. LVPECL DC CHARACTERISTICS, V_{CC} = 5.0V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		3.875	3.975	4.08	3.925	3.995	4.07	3.995	4.03	4.065	V
V_{OL}	Output Low Voltage; NOTE 1		3.105	3.245	3.38	3.125	3.22	3.315	3.14	3.235	3.33	V
V_{IH}	Input High Voltage (Single-Ended)		3.775		4.06	3.775		4.06	3.775		4.06	V
V_{IL}	Input Low Voltage (Single-Ended)		3.13		3.465	3.13		3.465	3.13		3.465	V
V_{BB}	Output Voltage Reference; NOTE 2		3.56		3.68	3.56		3.68	3.56		3.68	V
V_{PP}	Peak-to-Peak Input Voltage		150	800	1200	150	800	1200	150	800	1200	mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3, 4		1.2		5	1.2		5	1.2		5	V
I_{IH}	Input High Current	D			200			200			200	µA
I_{IL}	Input Low Current	D	-200			-200			-200			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.
NOTE 2: Single-ended input operation is limited. $V_{CC} \geq$ 3V in LVPECL mode.
NOTE 3: Common mode voltage is defined as V_{IH}.
NOTE 4: For single-ended applications, the maximum input voltage for D is V_{CC} + 0.3V.

TABLE 3D. ECL DC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -5.5V TO -3.0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		-1.125	-1.025	-0.92	-1.075	-1.005	-0.93	-1.005	-0.97	-0.935	V
V_{OL}	Output Low Voltage; NOTE 1		-1.895	-1.755	-1.62	-1.875	-1.78	-1.685	-1.86	-1.765	-1.67	V
V_{IH}	Input High Voltage(Single-Ended)		-1.225		-0.94	-1.225		-0.94	-1.225		-0.94	V
V_{IL}	Input Low Voltage(Single-Ended)		-1.87		-1.535	-1.87		-1.535	-1.87		-1.535	V
V_{BB}	Output Voltage Reference; NOTE 2		-1.44		-1.32	-1.44		-1.32	-1.44		-1.32	V
V_{PP}	Peak-to-Peak Input Voltage		150	800	1200	150	800	1200	150	800	1200	mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3, 4		V_{EE}+1.2V		0	V_{EE}+1.2V		0	V_{EE}+1.2V		0	V
I_{IH}	Input High Current	D			200			200			200	µA
I_{IL}	Input Low Current	D	-200			-200			-200			µA

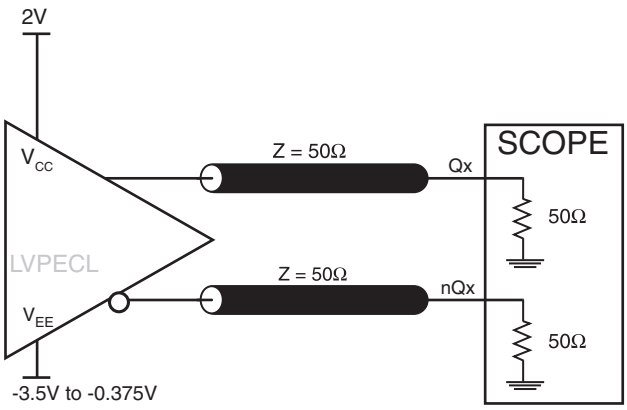
Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.
NOTE 2: Single-ended input operation is limited. $V_{CC} \geq$ 3V in LVPECL mode.
NOTE 3: Common mode voltage is defined as V_{IH}.
NOTE 4: For single-ended applications, the maximum input voltage for D is V_{CC} + 0.3V.

TABLE 4. AC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -5.5V TO -3.0V OR V_{CC} = 3.0V TO 5.5V; V_{EE} = 0V

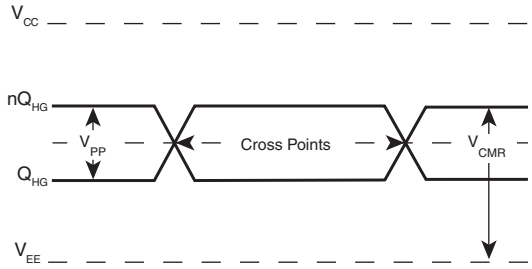
Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Output Frequency			TBD			>3			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay; NOTE 1	(Differential) nQ		TBD			350			TBD		ps
		(Differential) Q_{HG}, nQ_{HG}		TBD			400			TBD		ps
		(Single-Ended) nQ		TBD			400			TBD		ps
		(Single-Ended) Q_{HG}, nQ_{HG}		TBD			450			TBD		ps
*t*sk(odc)	Duty Cycle Skew; NOTE 2, 3			TBD			10			TBD		ps
t_R/t_F	Output Rise/ Fall Time 20% to 80%	nQ		TBD			300			TBD		ps
		Q_{HG}, nQ_{HG}		TBD			150			TBD		ps

All parameters are measured at f ≤ 1.7GHz, unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured for only differential operation from the cross point of the inputs to the cross point of the outputs.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

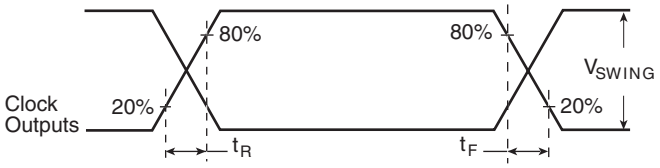
PARAMETER MEASUREMENT INFORMATION



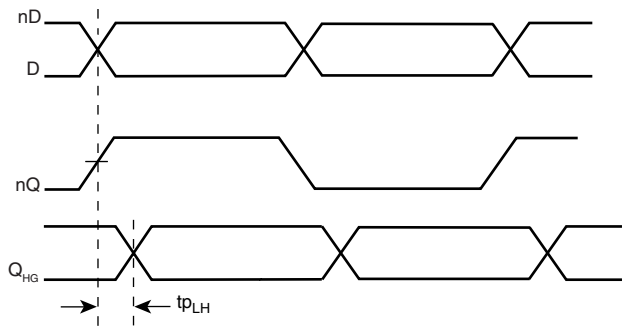
OUTPUT LOAD AC TEST CIRCUIT



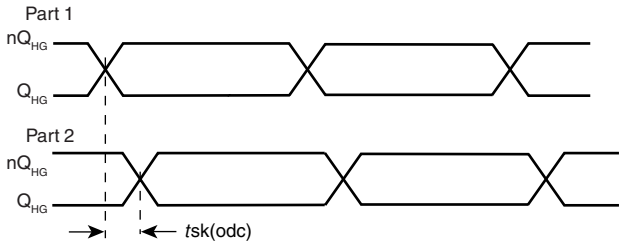
DIFFERENTIAL INPUT LEVEL



OUTPUT RISE/FALL TIME



PROPAGATION DELAY



DUTY CYCLE SKEW

APPLICATION INFORMATION

WIRING THE INPUT TO ACCEPT SINGLE ENDED LVPECL LEVELS

Figure 1 shows an example of the input that can be wired to accept single ended LVPECL levels.

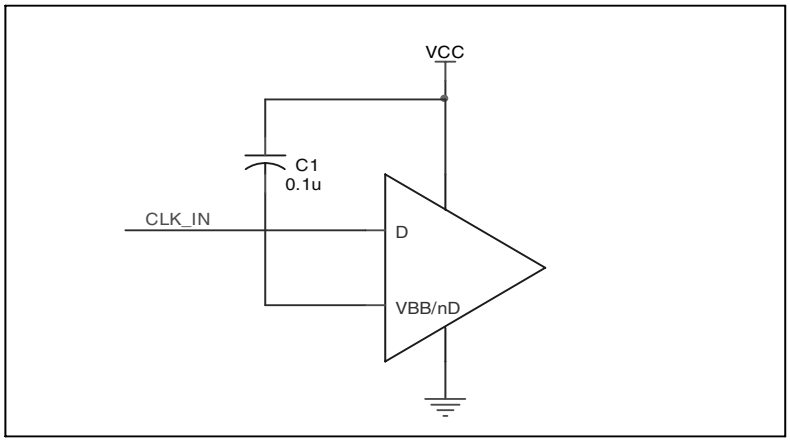


FIGURE 1. SINGLE ENDED LVPECL SIGNAL DRIVING DIFFERENTIAL INPUT

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

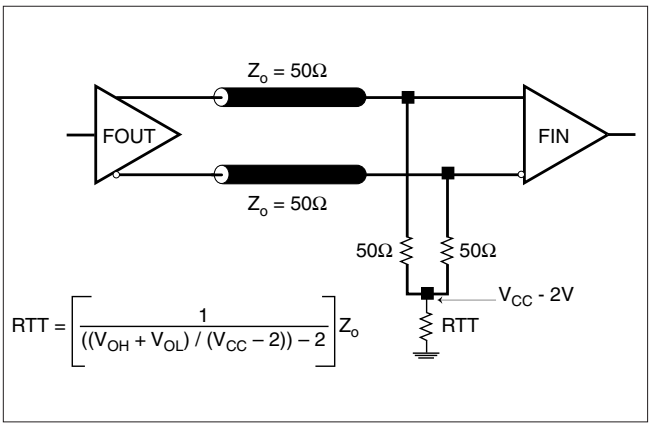


FIGURE 2A. LVPECL OUTPUT TERMINATION

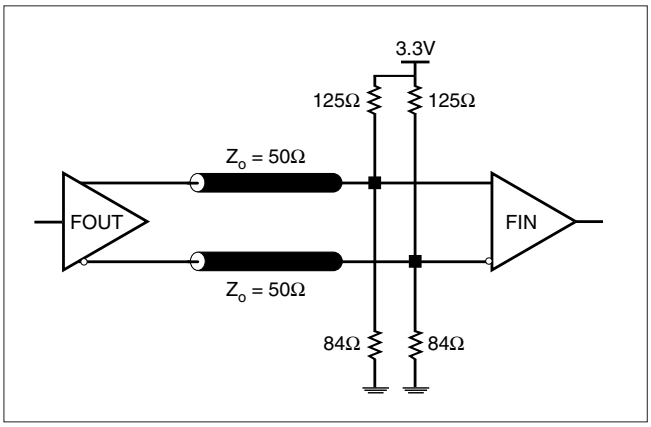


FIGURE 2B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 5V LVPECL OUTPUT

This section shows examples of 5V LVPECL output termination. *Figure 3A* shows standard termination for 5V LVPECL. The termination requires matched load of 50Ω resistors pull down to V_{CC} - 2V = 3V at the receiver. *Figure 3B* shows Thevenin equivalence of Figure 3A. In actual application where the 3V DC power supply is not available, this approached is normally used.

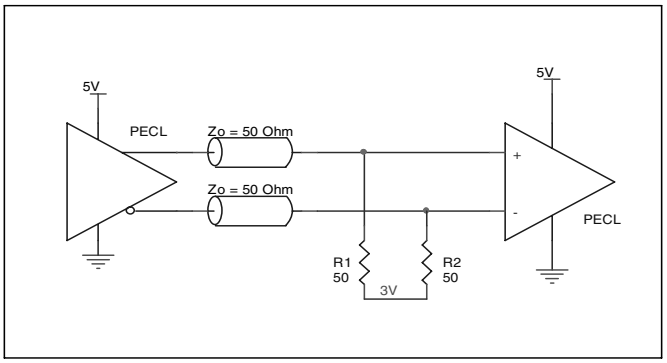


FIGURE 3A. STANDARD 5V LVPECL OUTPUT TERMINATION

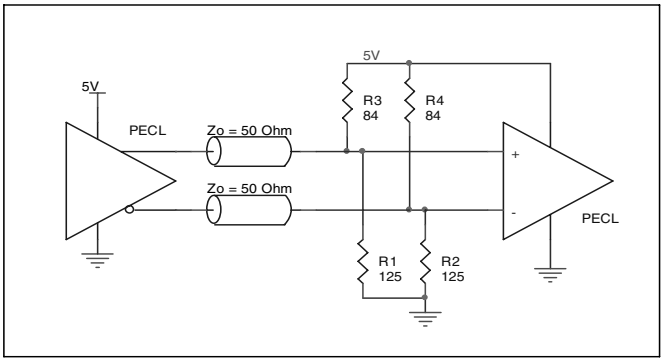


FIGURE 3B. 5V LVPECL OUTPUT TERMINATION EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS853016.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS853016 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 5.5V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 5.5V * 30mA = **165mW**
- Power $(outputs)_{MAX}$ = **30.94mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 30.94mW = **61.88mW**

Total Power$_{\_MAX}$ (5.5V, with all outputs switching) = 165mW + 61.88mW = **226.88mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 112.7°C/W per Table 5A below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.227W * 112.7°C/W = 110.6°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 5A. THERMAL RESISTANCE θ_{JA} FOR 8-PIN SOIC, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TABLE 5B. THERMAL RESISTANCE θ_{JA} FOR 8-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

3. Calculations and Equations.

LVPECL output driver circuit and termination are shown in Figure 4.

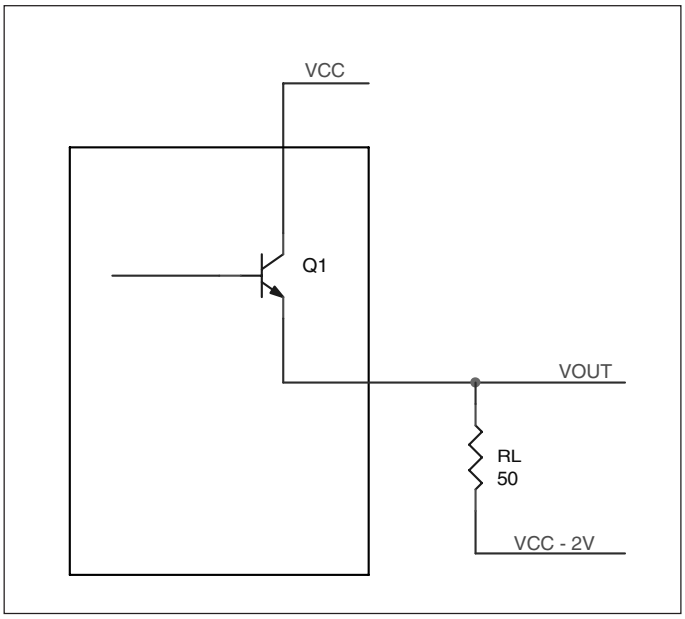


FIGURE 4. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} – 0.935V$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = 0.935V$

- For logic low, $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} – 1.67V$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = 1.67V$

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.935V)/50\Omega] * 0.935V = 19.92mW$

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.67V)/50\Omega] * 1.67V = 11.02mW$

Total Power Dissipation per output pair = Pd_H + Pd_L = 30.94mW

RELIABILITY INFORMATION

TABLE 6A. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

TABLE 6B. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD SOIC

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

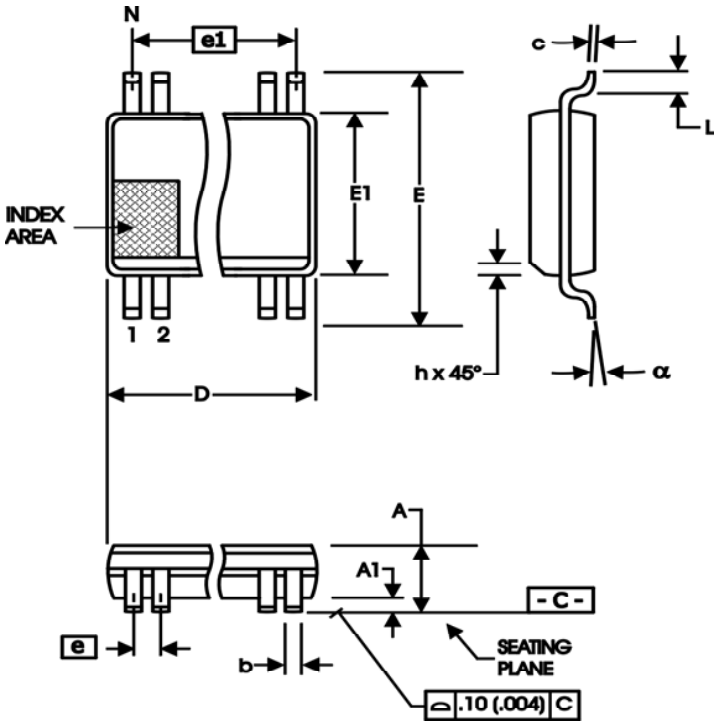
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS853016 is: 163

Pin compatible with MC100EP16VCD and MC100EP16VCDT

Package Outline - G Suffix for 8 Lead TSSOP



Package Outline - M Suffix for 8 Lead SOIC

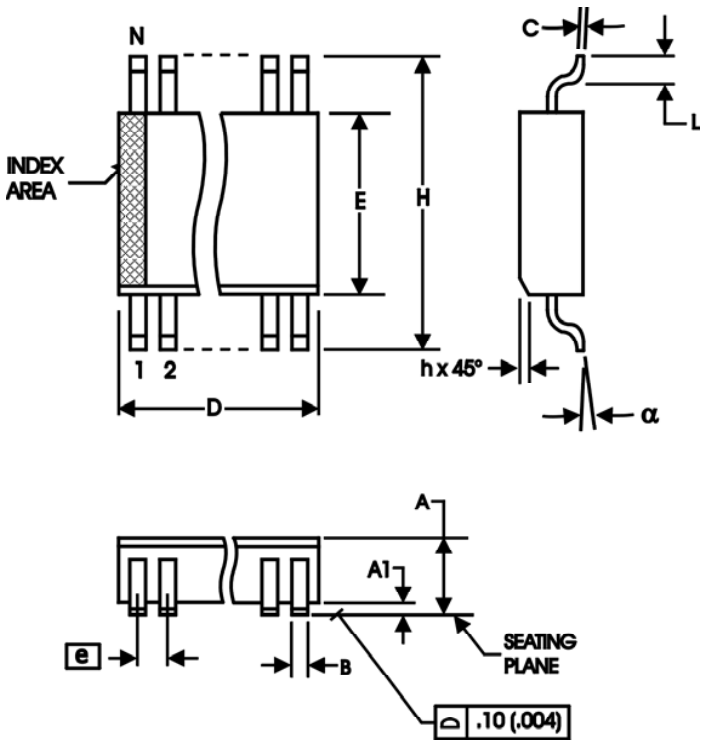


Table 8A. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.10
A1	0	0.15
A2	0.79	0.97
b	0.22	0.38
c	0.08	0.23
D	3.00 BASIC	
E	4.90 BASIC	
E1	3.00 BASIC	
e	0.65 BASIC	
e1	1.95 BASIC	
L	0.40	0.80
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-187

Table 8B. Package Dimensions

SYMBOL	Millimeters	
	MINIMUN	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS853016AM	853016A	8 lead SOIC	tube	-40°C to 85°C
ICS853016AMT	853016A	8 lead SOIC	2500 tape & reel	-40°C to 85°C
ICS853016AMLF	TBD	Lead-Free, 8 lead SOIC	tube	-40°C to 85°C
ICS853016AMLFT	TBD	Lead-Free, 8 lead SOIC	2500 tape & reel	-40°C to 85°C
ICS853016AG	016A	8 lead TSSOP	tube	-40°C to 85°C
ICS853016AGT	016A	8 lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS853016AGLF	16AL	Lead-Free, 8 lead TSSOP	tube	-40°C to 85°C
ICS853016AGLFT	16AL	Lead-Free, 8 lead TSSOP	2500 tape & reel	-40°C to 85°C

Parts that are ordered with an ""LF"" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales
800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support
netcom@idt.com
480-763-2056

Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Asia Pacific and Japan
Integrated Device Technology
Singapore (1997) Pte. Ltd.
Reg. No. 199707558G
435 Orchard Road
#20-03 Wisma Atria
Singapore 238877
+65 6 887 5505

Europe
IDT Europe, Limited
321 Kingston Road
Leatherhead, Surrey
KT22 7TU
England
+44 (0) 1372 363 339
Fax: +44 (0) 1372 378851

www.IDT.com