Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!


## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# Low Skew, 1-to-5 Differential-to-2.5V, 3.3V LVPECL Fanout Buffer

# ICS85314I-11

**DATA SHEET**

## General Description

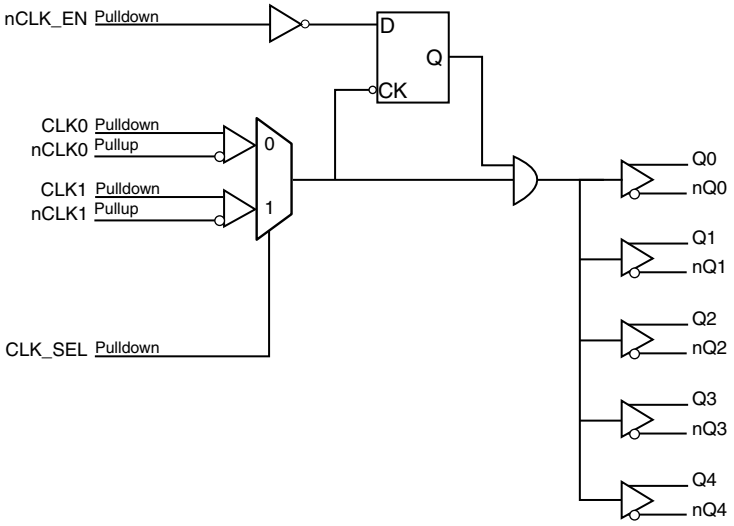
The ICS85314I-11 is a low skew, high performance 1-to-5 Differential-to-2.5V, 3.3V LVPECL fanout buffer. The ICS85314I-11 has two selectable differential clock inputs. The CLK0, nCLK0 and CLK1, nCLK1 pairs can accept most standard differential input levels. The clock enable is internally synchronized to eliminate runt clock pulses on the outputs during asynchronous assertion/ deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS85314I-11 ideal for those applications demanding well defined performance and repeatability.

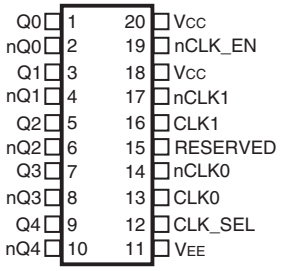
## Features

- Five differential 2.5V/3.3V LVPECL outputs
- Selectable differential CLKx, nCLKx inputs
- CLK0, nCLK0 and CLK1, nCLK1 pairs can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Maximum output frequency: 700MHz
- Translates any single-ended input signal to 3.3V LVPECL levels with resistor bias on nCLK input
- Output skew: 30ps (maximum)
- Propagation delay: 1.8ns (maximum)
- LVPECL mode operating voltage supply range: $V_{CC}$ = 2.375V to 3.8V, $V_{EE}$ = 0V
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

## Block Diagram




## Pin Assignment




**ICS85314I-11**

**20-Lead TSSOP**
**6.5mm x 4.4mm x 0.92mm package body**
**G Package**
**Top View**

**ICS85314I-11**

**20-Lead SOIC**
**7.5mm x 12.8mm x 2.3mm package body**
**M Package**
**Top View**

## Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1, 2 | Q0, nQ0 | Output | | Differential output pair. LVPECL interface levels. |
| 3, 4 | Q1, nQ1 | Output | | Differential output pair. LVPECL interface levels. |
| 5, 6 | Q2, nQ2 | Output | | Differential output pair. LVPECL interface levels. |
| 7, 8 | Q3, nQ3 | Output | | Differential output pair. LVPECL interface levels. |
| 9, 10 | Q4, nQ4 | Output | | Differential output pair. LVPECL interface levels. |
| 11 | $V_{EE}$ | Power | | Negative supply pin. |
| 12 | CLK_SEL | Input | Pulldown | Clock select input. When HIGH, selects CLK1, nCLK1 inputs. When LOW, selects CLK0, nCLK0 inputs. LVTTL / LVCMOS interface levels. |
| 13 | CLK0 | Input | Pulldown | Non-inverting differential clock input. |
| 14 | nCLK0 | Input | Pullup | Inverting differential clock input. |
| 15 | RESERVED | Reserve | | Reserved pin. |
| 16 | CLK1 | Input | Pulldown | Non-inverting differential clock input. |
| 17 | nCLK1 | Input | Pullup | Inverting differential clock input. |
| 18, 20 | $V_{CC}$ | Power | | Positive supply pins. |
| 19 | nCLK_EN | Input | Pulldown | Synchronizing clock enable. When LOW, clock outputs follow clock input. When HIGH, Q outputs are forced low, nQ outputs are forced high. LVTTL / LVCMOS interface levels. |

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

## Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | kΩ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | kΩ |

# Function Tables

### Table 3A. Control Input Function Table

| Inputs | | | Outputs | |
|---|---|---|---|---|
| **nCLK_EN** | **CLK_SEL** | **Selected Source** | **Q[0:4]** | **nQ[0:4]** |
| 0 | 0 | CLK0, nCLK0 | Enabled | Enabled |
| 0 | 1 | CLK1, nCLK1 | Enabled | Enabled |
| 1 | 0 | CLK0, nCLK0 | Disabled; LOW | Disabled; HIGH |
| 1 | 1 | CLK1, nCLK1 | Disabled; LOW | Disabled; HIGH |

After nCLK_EN switches, the clock outputs are disabled or enabled following a falling input clock edge as shown in *Figure 1.* In the active mode, the state of the outputs are a function of the CLK0, nCLK0 and CLK1, nCLK1 inputs as described in *Table 3B.*

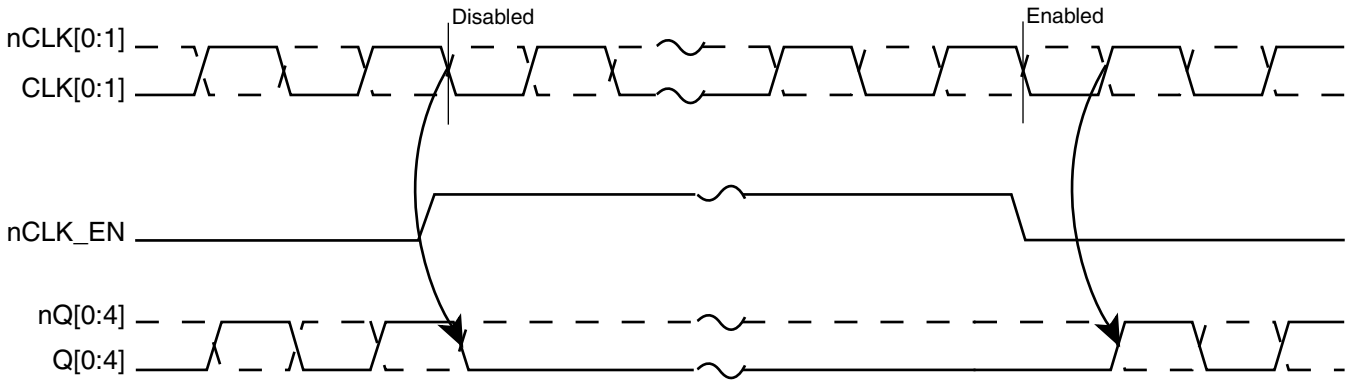



**Figure 1. nCLK_EN Timing Diagram**

### Table 3B. Clock Input Function Table

| Inputs | | Outputs | | | |
|---|---|---|---|---|---|
| **CLK0 or CLK1** | **nCLK0 or nCLK1** | **Q[0:4]** | **nQ[0:4]** | **Input to Output Mode** | **Polarity** |
| 0 | 1 | LOW | HIGH | Differential-to-Differential | Non-Inverting |
| 1 | 0 | HIGH | LOW | Differential-to-Differential | Non-Inverting |

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|---|
| Supply Voltage, $V_{CC}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{CC}$ + 0.5V |
| Outputs, $I_O$<br>Continuos Current<br>Surge Current | <br>50mA<br>100mA |
| Package Thermal Impedance, $\theta_{JA}$<br>20 Lead SOIC<br>20 Lead TSSOP | <br>46.2°C/W (0 lfpm)<br>73.2°C/W (0 lfpm) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,** $V_{CC}$ = 2.375V to 3.8V; $V_{EE}$ = 0V, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Positive Supply Voltage | | 2.375 | 3.3 | 3.8 | V |
| $I_{EE}$ | Power Supply Current | | | | 80 | mA |

**Table 4B. LVCMOS/LVTTL DC Characteristics,** $V_{CC}$ = 2.375V to 3.8V; $V_{EE}$ = 0V, $T_A$ = -40°C to 85°**C**

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | 2 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | | -0.3 | | 0.8 | V |
| $I_{IH}$ | Input High Current | nCLK_EN, CLK_SEL | $V_{CC}$ = $V_{IN}$ = 3.8V | | | 150 | µA |
| $I_{IL}$ | Input Low Current | nCLK_EN, CLK_SEL | $V_{CC}$ = 3.8V, $V_{IN}$ = 0V | -5 | | | µA |

**Table 4C. Differential DC Characteristics,** $V_{CC}$ = 2.375V to 3.8V; $V_{EE}$ = 0V, $T_A$ = -40°C to 85°**C**

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | CLK0, CLK1 | $V_{CC}$ = $V_{IN}$ = 3.8V | | | 150 | µA |
| | | nCLK0, nCLK1 | $V_{CC}$ = $V_{IN}$ = 3.8V | | | 5 | µA |
| $I_{IL}$ | Input Low Current | CLK0, CLK1 | $V_{CC}$ = 3.8V, $V_{IN}$ = 0V | -5 | | | µA |
| | | nCLK0, nCLK1 | $V_{CC}$ = 3.8V, $V_{IN}$ = 0V | -150 | | | µA |
| $V_{PP}$ | Peak-to-Peak Voltage; NOTE 1 | | | 0.15 | | 1.3 | V |
| $V_{CMR}$ | Common Mode Range; NOTE 1, 2 | | | 0.5 | | $V_{CC}$ – 0.85 | V |

NOTE 1: $V_{IL}$ should not be less than -0.3V
NOTE 2: Common mode voltage is defined as $V_{IH}$.

**Table 4D. LVPECL DC Characteristics,** $V_{CC}$ = 2.375V to 3.8V; $V_{EE}$ = 0V, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage; NOTE 1 | | $V_{CC}$ – 1.4 | | $V_{CC}$ – 0.9 | V |
| $V_{OL}$ | Output Low Voltage; NOTE 1 | | $V_{CC}$ – 2.0 | | $V_{CC}$ – 1.7 | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1: Outputs termination with 50Ω to $V_{CC}$ – 2V.

# AC Electrical Characteristics

**Table 5. AC Characteristics,** $V_{CC}$ = 2.375V to 3.8V; $V_{EE}$ = 0V, $T_A$ = -40°C to 85°C

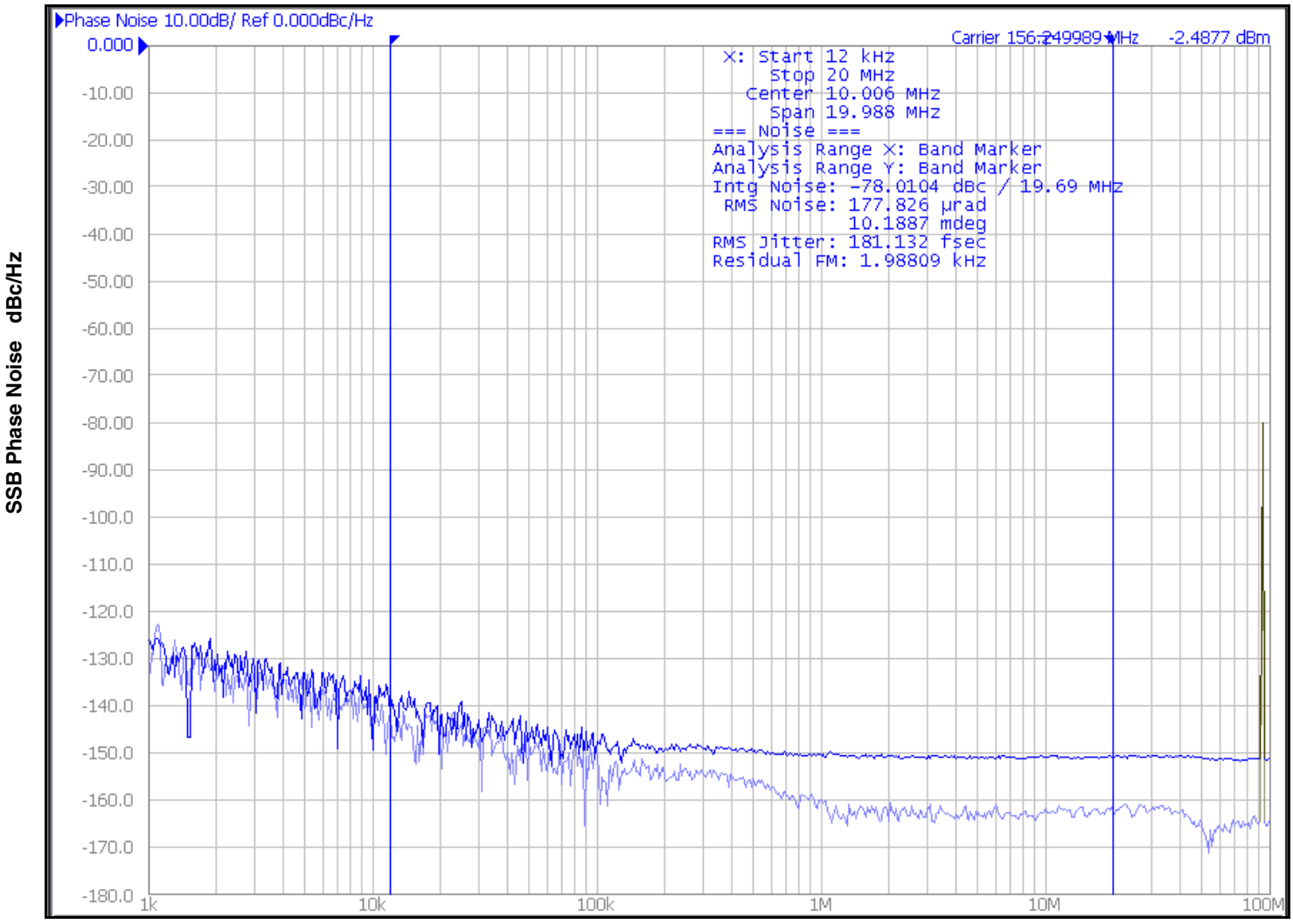
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | | | | 700 | MHz |
| $tp_{LH}$ | Propagation Delay, Low to High; NOTE 1 | $f \leq$ 700MHz | 1.0 | 1.4 | 1.8 | ns |
| *t*sk(o) | Output Skew; NOTE 2, 3 | | | | 30 | ps |
| *t*jit | Buffer Additive Phase Jitter, RMS | 156.25MHz, Integration Range: 12kHz - 20MHz | | 0.170 | 0.200 | ps |
| | | 644.53125MHz, Integration Range: 12kHz - 20MHz | | 0.060 | 0.200 | ps |
| *t*sk(pp) | Part-to-Part Skew; NOTE 3, 4 | | | | 350 | ps |
| $t_S$ | Setup Time | nCLK_EN to CLK | 50 | | | ps |
| $t_H$ | Hold Time | nCLK_EN to CLK | 50 | | | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 200 | | 700 | ps |
| odc | Output Duty Cycle Skew | $f \leq$ 700MHz | 45 | | 55 | % |

NOTE: All parameters measured at $f_{OUT}$ unless otherwise noted.
NOTE: The cycle-to-cycle jitter on the input will equal the jitter on the output. The part does not add jitter.
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

## 156.25MHz Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



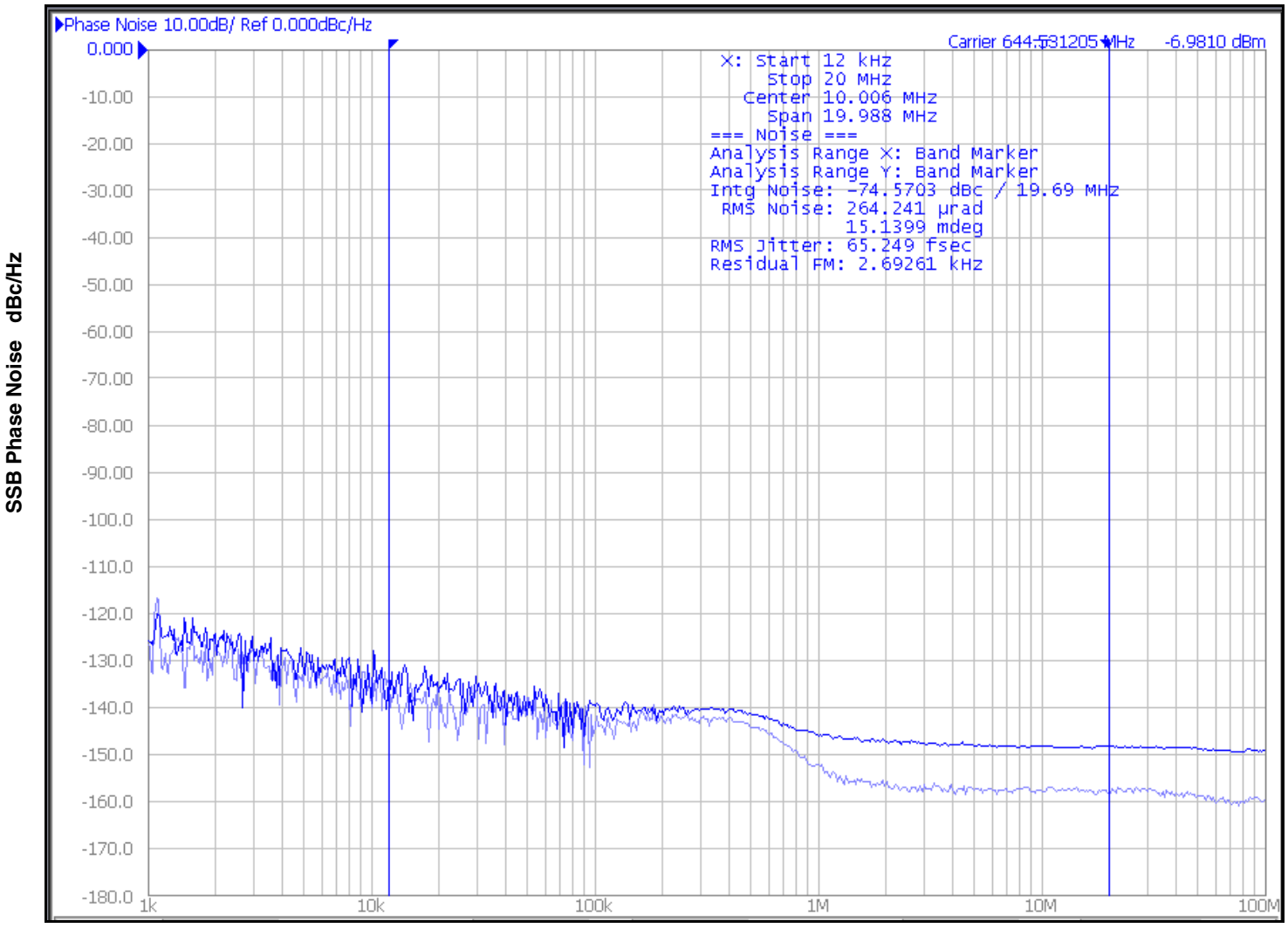

As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

Measured using a Rohde & Schwarz SMA100 as the input source.

## 644.53125MHz Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

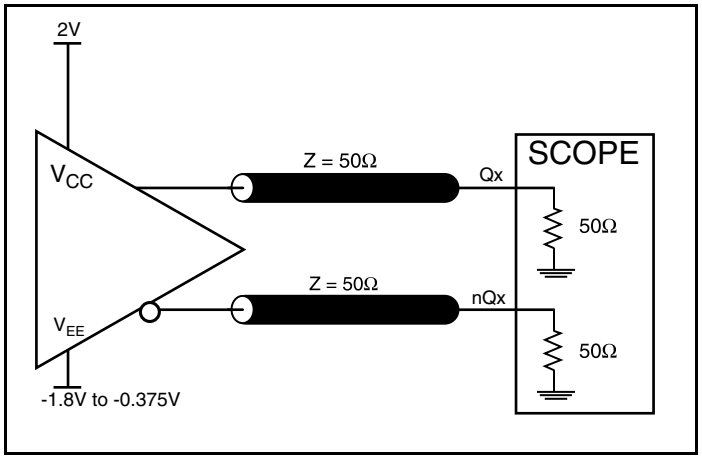



As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

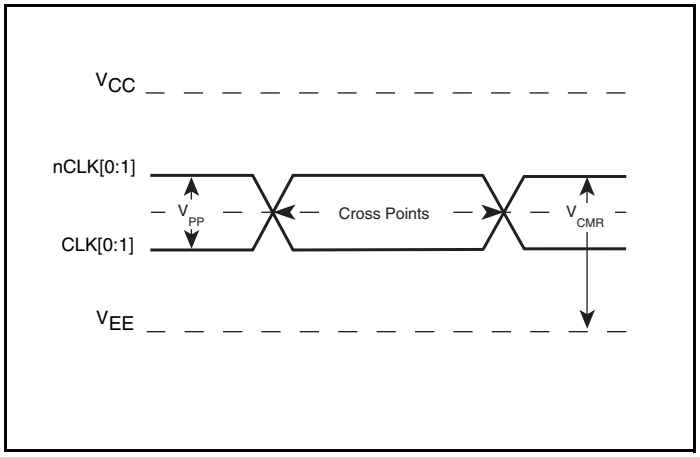
Measured using a Rohde & Schwarz SMA100 as the input source.

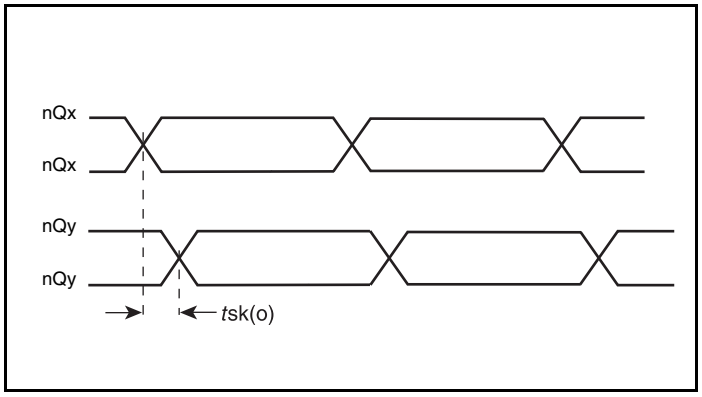
# Parameter Measurement Information



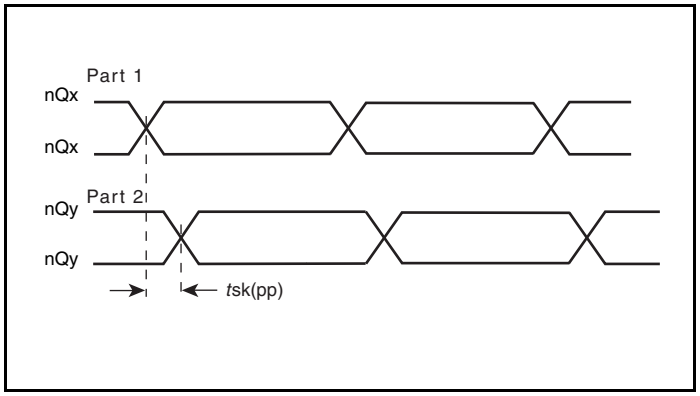

**LVPECL Output Load Test Circuit**



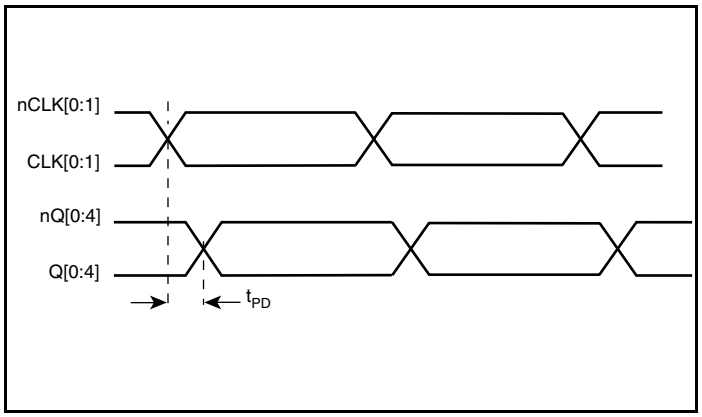

**Differential Input Level**



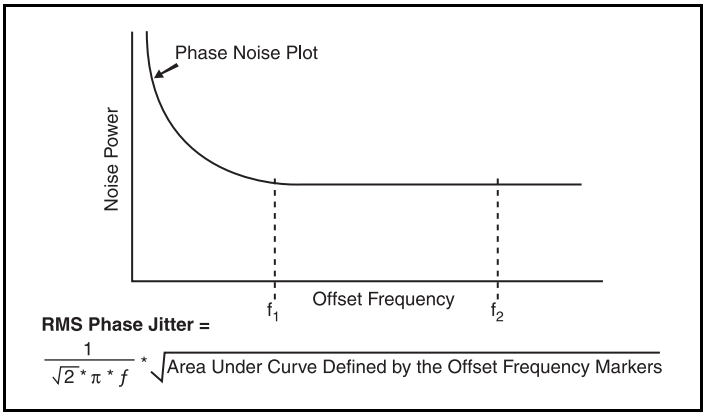

**Output Skew**




**Part-to-Part Skew**



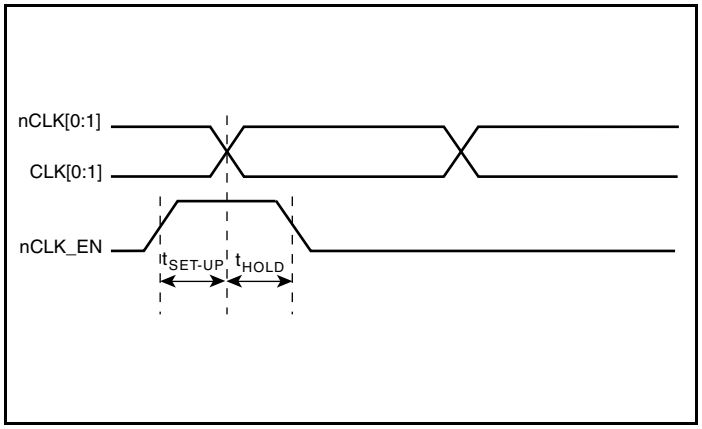

**Propagation Delay**



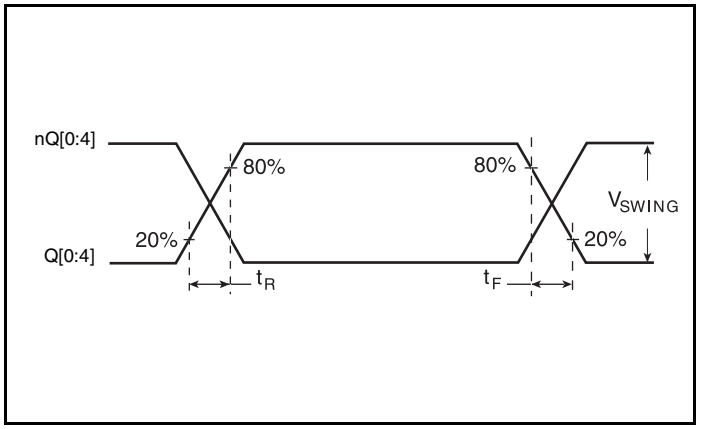

**RMS Phase Jitter**

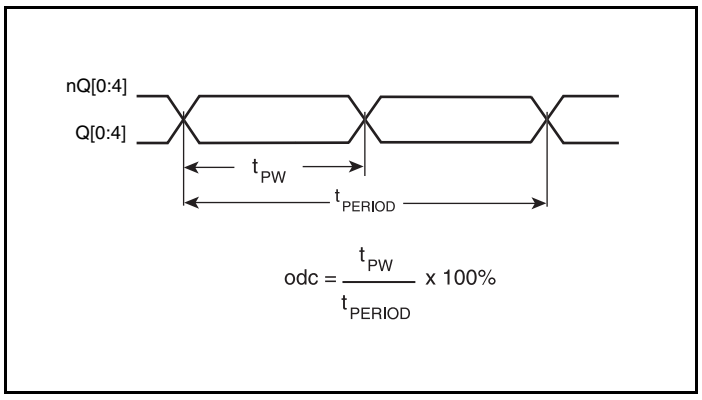
# Parameter Measurement Information, continued




**Setup & Hold Time**




**Output Rise/Fall Time**




**Output Duty Cycle**

# Application Information

## Wiring the Differential Input to Accept Single-Ended Levels

*Figure 2* shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the $V_1$ in the center of the input voltage swing. For example, if the input clock swing is 2.5V and $V_{CC}$ = 3.3V, R1 and R2 value should be adjusted to set $V_1$ at 1.25V. The values below are for when both the single ended swing and $V_{CC}$ are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however $V_{IL}$ cannot be less than -0.3V and $V_{IH}$ cannot be more than $V_{CC}$ + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

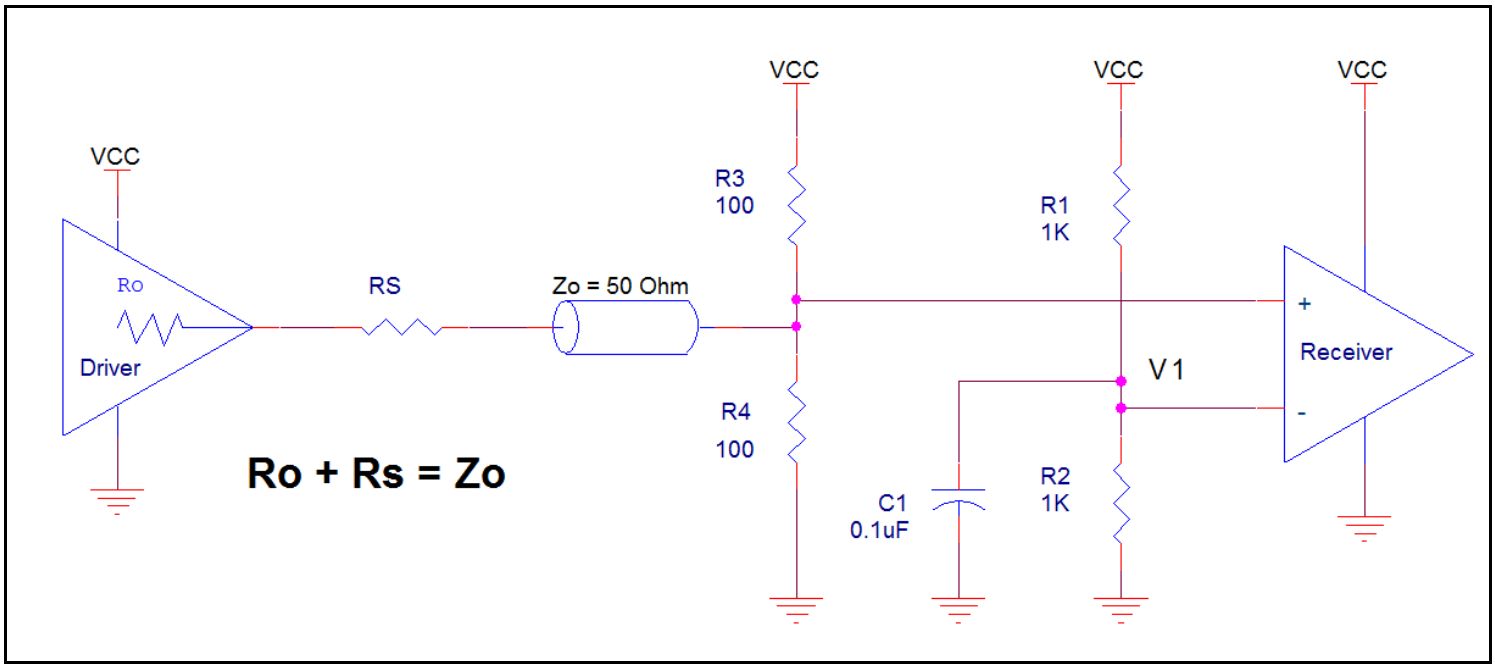



**Figure 2. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels**

## Recommendations for Unused Input and Output Pins

### Inputs:

#### CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

#### Control Pins

All control pins have internal pulldown resistors; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### Outputs:

#### LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

## 3.3V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both $V_{SWING}$ and $V_{OH}$ must meet the $V_{PP}$ and $V_{CMR}$ input requirements. Figures 3A to 3F show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A,* the input termination applies for IDT LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

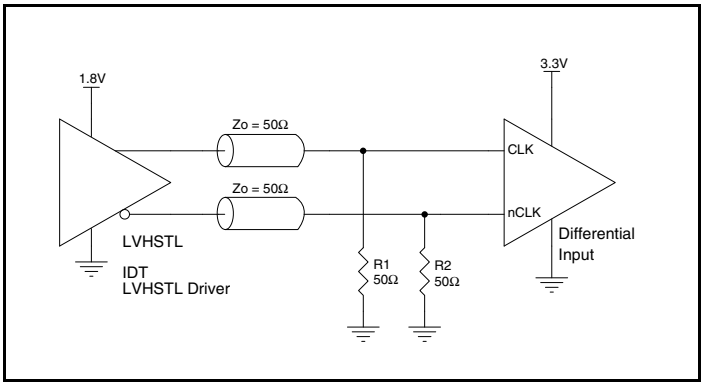



**Figure 3A. CLK/nCLK Input Driven by an IDT LVHSTL Driver**

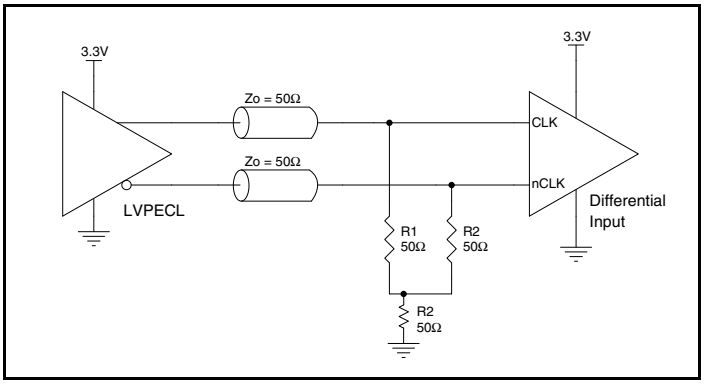



**Figure 3B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**

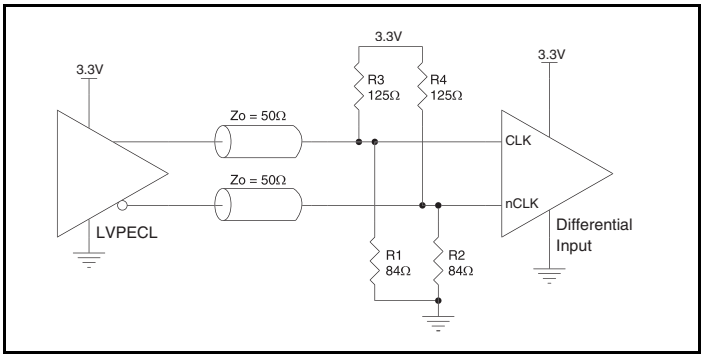



**Figure 3C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**

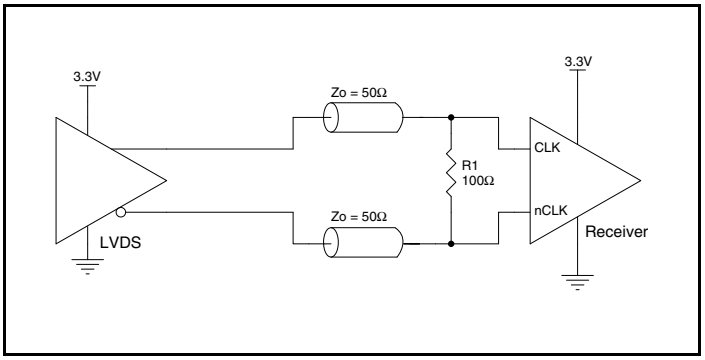



**Figure 3D. CLK/nCLK Input Driven by a 3.3V LVDS Driver**

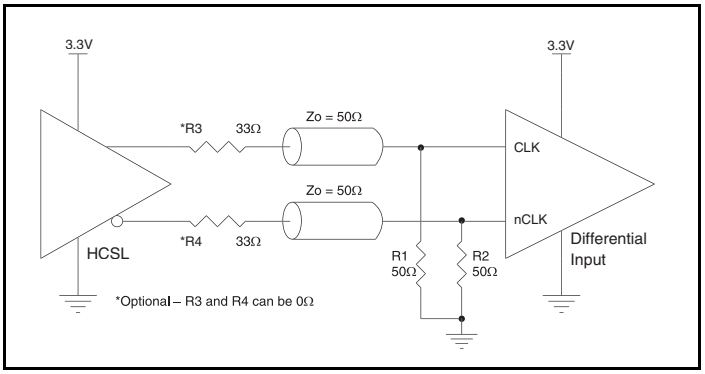



**Figure 3E. CLK/nCLK Input Driven by a 3.3V HCSL Driver**

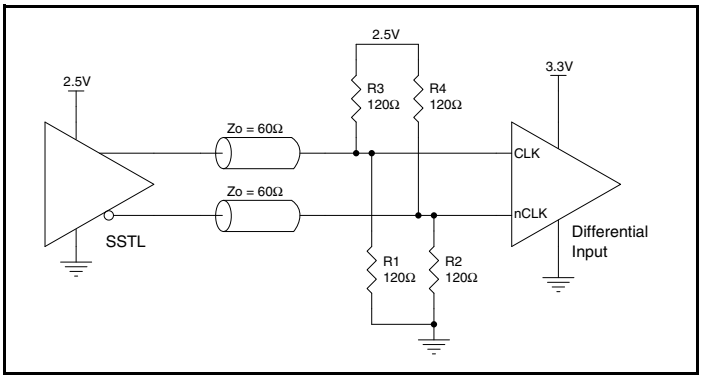



**Figure 3F. CLK/nCLK Input Driven by a 2.5V SSTL Driver**

## 2.5V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both $V_{SWING}$ and $V_{OH}$ must meet the $V_{PP}$ and $V_{CMR}$ input requirements. Figures 3A to 3F show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A,* the input termination applies for IDT LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

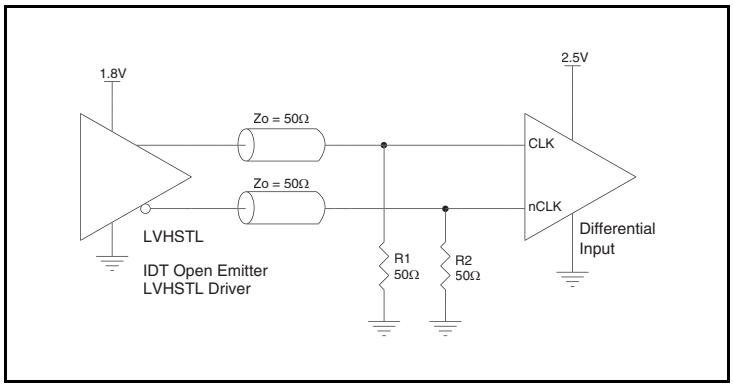



**Figure 3A. CLK/nCLK Input Driven by an IDT LVHSTL Driver**

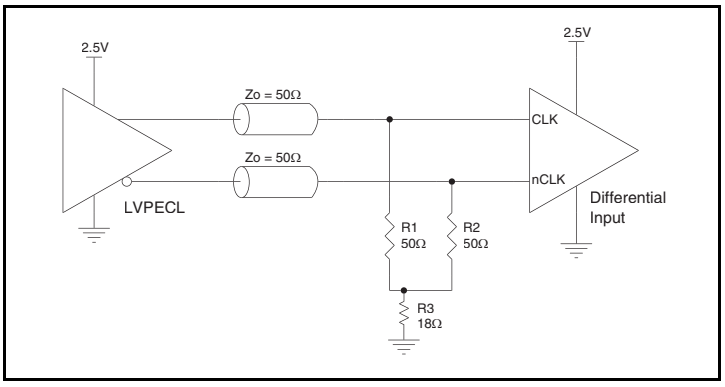



**Figure 3B. CLK/nCLK Input Driven by a 2.5V LVPECL Driver**

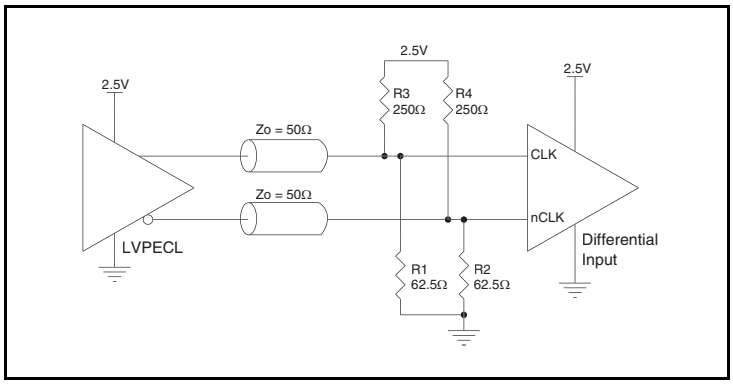



**Figure 3C. CLK/nCLK Input Driven by a 2.5V LVPECL Driver**

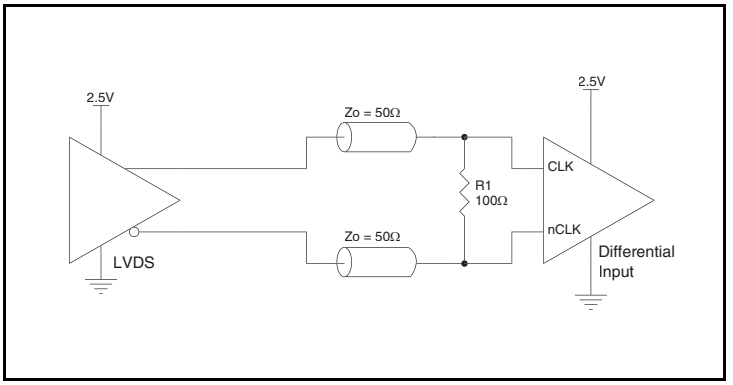



**Figure 3D. CLK/nCLK Input Driven by a 2.5V LVDS Driver**

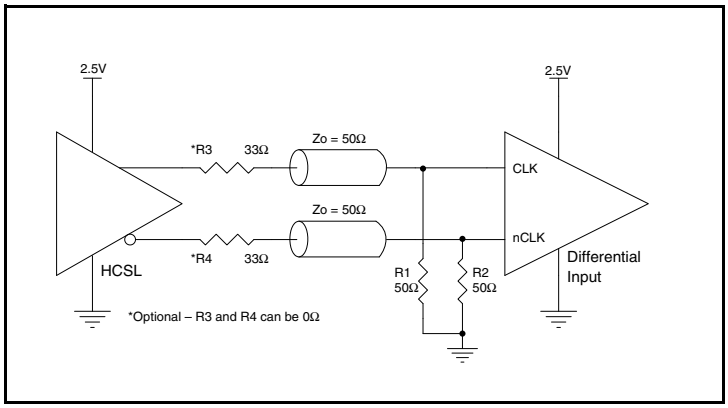



**Figure 3E. CLK/nCLK Input Driven by a 2.5V HCSL Driver**

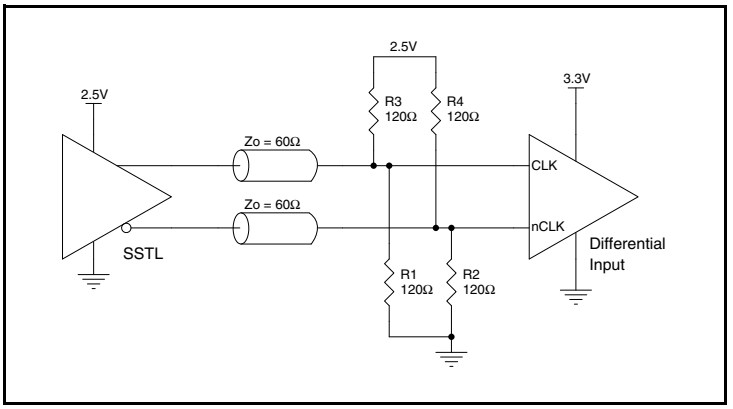



**Figure 3F. CLK/nCLK Input Driven by a 2.5V SSTL Driver**

## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

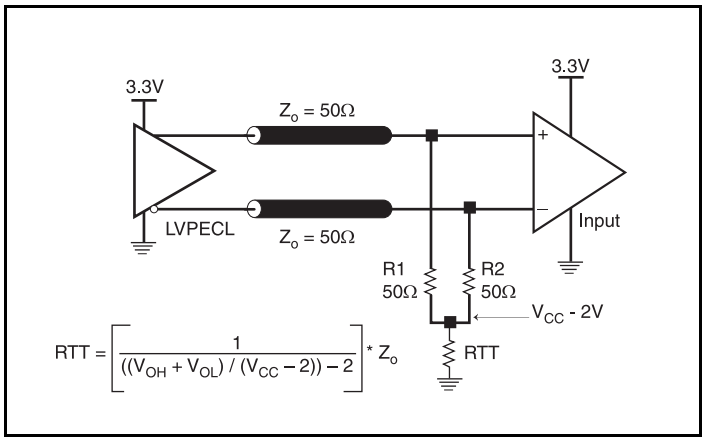



**Figure 5A. 3.3V LVPECL Output Termination**

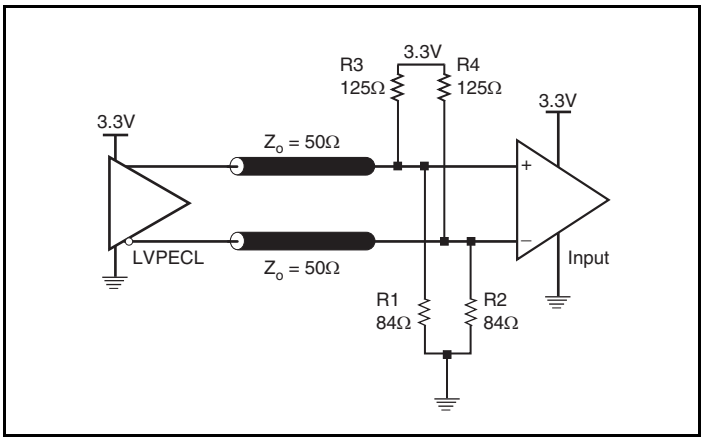



**Figure 5B. 3.3V LVPECL Output Termination**

## Termination for 2.5V LVPECL Outputs

*Figure 6A* and *Figure 6B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{CC}$ – 2V. For $V_{CC}$ = 2.5V, the $V_{CC}$ – 2V is very close to ground level. The R3 in Figure 6B can be eliminated and the termination is shown in *Figure 6C.*

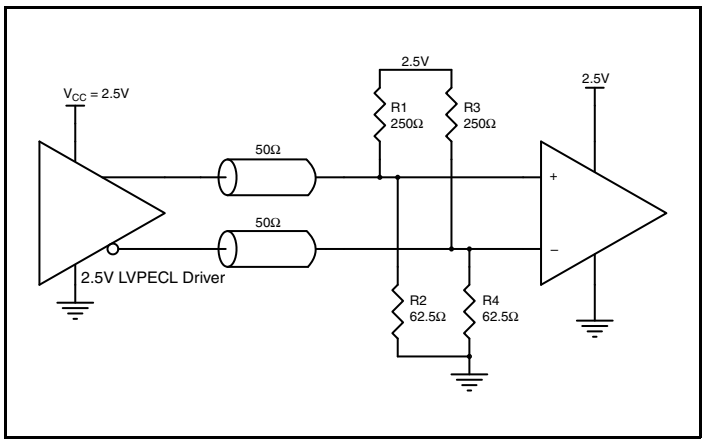



**Figure 6A. 2.5V LVPECL Driver Termination Example**

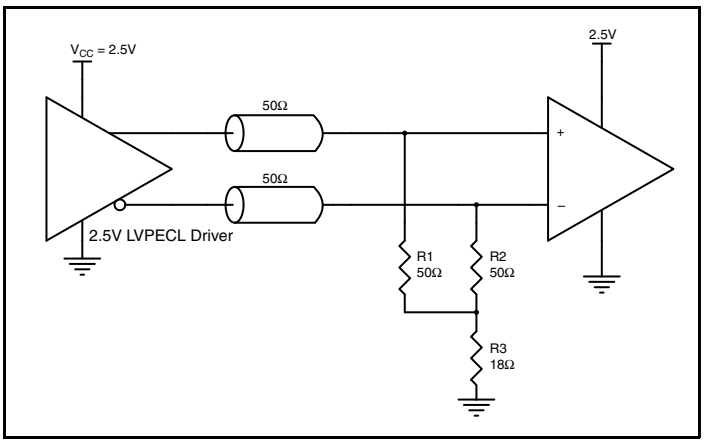



**Figure 6B. 2.5V LVPECL Driver Termination Example**

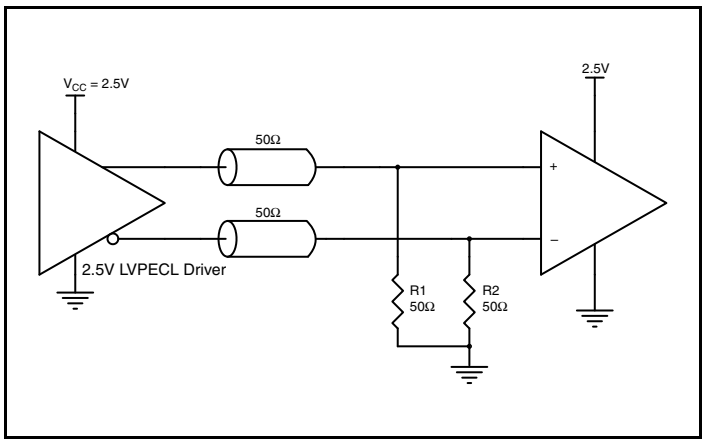



**Figure 6C. 2.5V LVPECL Driver Termination Example**

# Power Considerations

This section provides information on power dissipation and junction temperature for the ICS85314I-11.
Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS85314I-11 is the sum of the core power plus the power dissipated due to loading.
The following is the power dissipation for $V_{CC}$ = 3.8V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated due to loading.

- Power (core)$_{MAX}$ = $V_{CC\_MAX}$ * $I_{EE\_MAX}$ = 3.8V * 80mA = **304mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 5 * 30mW = **150mW**

**Total Power**$_{\_MAX}$ (3.6V, with all outputs switching) = 304mW + 150mW = **454mW**

### 2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and it directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming a moderate air flow or 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6B below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.454W * 66.6°C/W = 115°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 6A. Thermal Resistance $\theta_{JA}$ for 20 Lead SOIC, Forced Convection**

| $\theta_{JA}$ by Velocity | | | |
|---|---|---|---|
| Linear Feet per Minute | **0** | **200** | **500** |
| Single-Layer PCB, JEDEC Standard Test Boards | 83.2°C/W | 65.7°C/W | 57.5°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 46.2°C/W | 39.7°C/W | 36.8°C/W |

NOTE: Most modern PCB design use multi-layered boards. The data in the second row pertains to most designs.

**Table 6B. Thermal Resistance $\theta_{JA}$ for 20 Lead TSSOP, Forced Convection**

| $\theta_{JA}$ by Velocity | | | |
|---|---|---|---|
| Linear Feet per Minute | **0** | **200** | **500** |
| Single-Layer PCB, JEDEC Standard Test Boards | 114.5°C/W | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 73.2°C/W | 66.6°C/W | 63.5°C/W |

NOTE: Most modern PCB design use multi-layered boards. The data in the second row pertains to most designs.

**3. Calculations and Equations.**

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 7.*

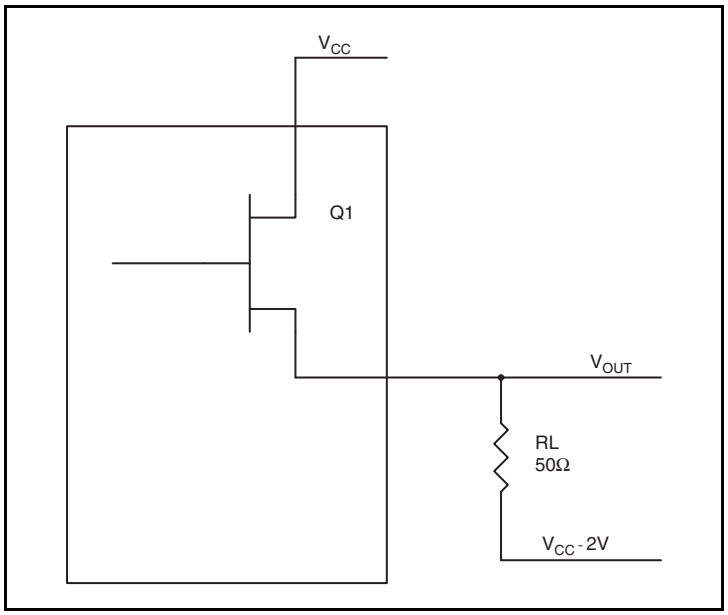



**Figure 7. LVPECL Driver Circuit and Termination**

To calculate power dissipation due to loading, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC}$ – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 0.9V}$
  $(V_{CC\_MAX} – V_{OH\_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.7V}$
  $(V_{CC\_MAX} – V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

# Reliability Information

**Table 7A. $\theta_{JA}$ vs. Air Flow Table for a 20 Lead SOIC, Forced Convection**

| $\theta_{JA}$ by Velocity | | | |
|---|---|---|---|
| Linear Feet per Minute | **0** | **200** | **500** |
| Single-Layer PCB, JEDEC Standard Test Boards | 83.2°C/W | 65.7°C/W | 57.5°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 46.2°C/W | 39.7°C/W | 36.8°C/W |

NOTE: Most modern PCB design use multi-layered boards. The data in the second row pertains to most designs.

**Table 7B. $\theta_{JA}$ vs. Air Flow Table for a 20 Lead TSSOP, Forced Convection**

| $\theta_{JA}$ by Velocity | | | |
|---|---|---|---|
| Linear Feet per Minute | **0** | **200** | **500** |
| Single-Layer PCB, JEDEC Standard Test Boards | 114.5°C/W | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 73.2°C/W | 66.6°C/W | 63.5°C/W |

NOTE: Most modern PCB design use multi-layered boards. The data in the second row pertains to most designs.

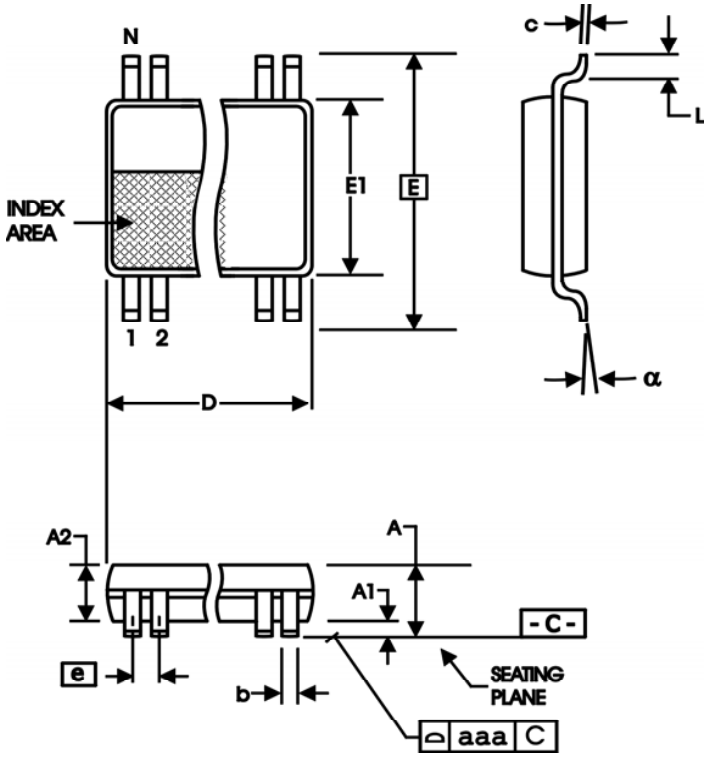
## Transistor Count

The transistor count for ICS85314I-11 is: 674

# Package Outlines and Package Dimensions

### Package Outline - G Suffix for 20 Lead TSSOP




### Package Outline - M Suffix for 20 Lead SOIC

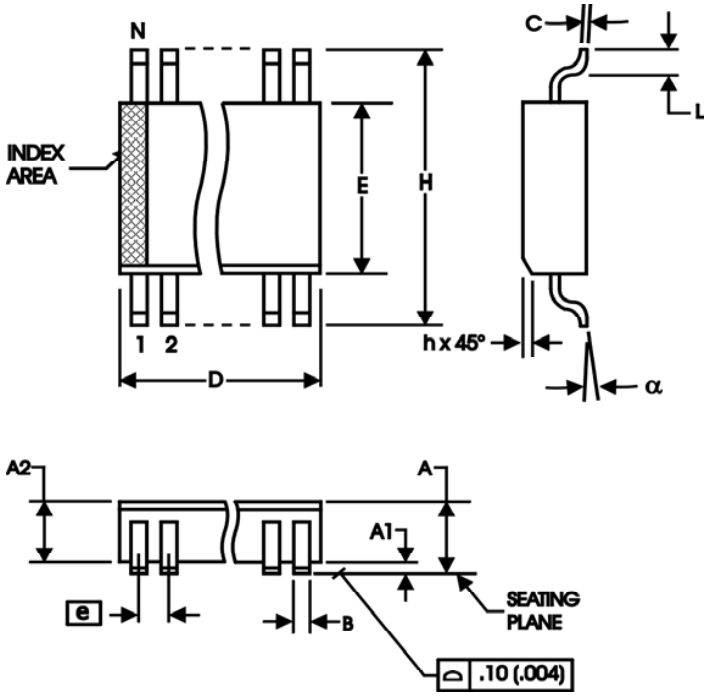



**Table 8A. Package Dimensions**

| All Dimensions in Millimeters | | |
|---|---|---|
| **Symbol** | **Minimum** | **Maximum** |
| **N** | 20 | |
| **A** | | 1.20 |
| **A1** | 0.05 | 0.15 |
| **A2** | 0.80 | 1.05 |
| **b** | 0.19 | 0.30 |
| **c** | 0.09 | 0.20 |
| **D** | 6.40 | 6.60 |
| **E** | 6.40 Basic | |
| **E1** | 4.30 | 4.50 |
| **e** | 0.65 Basic | |
| **L** | 0.45 | 0.75 |
| α | 0° | 8° |
| **aaa** | | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

**Table 8B. Package Dimensions for 20 Lead SOIC**

| 300 Millimeters<br>All Dimensions in Millimeters | | |
|---|---|---|
| **Symbol** | **Minimum** | **Maximum** |
| **N** | 20 | |
| **A** | | 2.65 |
| **A1** | 0.10 | |
| **A2** | 2.05 | 2.55 |
| **B** | 0.33 | 0.51 |
| **C** | 0.18 | 0.32 |
| **D** | 12.60 | 13.00 |
| **E** | 7.40 | 7.60 |
| **e** | 1.27 Basic | |
| **H** | 10.00 | 10.65 |
| **h** | 0.25 | 0.75 |
| **L** | 0.40 | 1.27 |
| α | 0° | 7° |

Reference Document: JEDEC Publication 95, MS-013, MS-119

# Ordering Information

**Table 9. Ordering Information**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 85314AGI-11LF | ICS5314AI11L | “Lead-Free” 20 Lead TSSOP | Tube | -40°C to 85°C |
| 85314AGI-11LFT | ICS5314AI11L | “Lead-Free” 20 Lead TSSOP | Tape & Reel | -40°C to 85°C |
| 85314AMI-11LF | ICS85314AMI-11LF | “Lead-Free” 20 Lead SOIC | Tube | -40°C to 85°C |
| 85314AMI-11LFT | ICS85314AMI-11LF | “Lead-Free” 20 Lead SOIC | Tape & Reel | -40°C to 85°C |

# Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|---|---|---|---|---|
| A | T1<br><br>T2 | 2<br><br>2<br>4<br>7<br>8 | Pin Description Table - Pin 14 & 17, nCLKx, deleted partial description and added Pullup in the “Type” column.<br>Pin Characteristics Table - $C_{IN}$ changed 4pF max. to 4pF typical.<br>AMR - corrected Output rating.<br>Added Wiring the Differential Input to Accept Single Ended Levels section.<br>Added Differential Clock Input Interface section. | 6/11/03 |
| B | T5 | 1<br>5<br>6<br>8<br>9 | Added Phase Noise bullet in Features section.<br>AC Characteristics Table - added RMS Phase Jitter.<br>Added Phase Jitter Plot.<br>Updated Termination for 3.3V LVPECL Output diagrams.<br>Added Termination for 2.5V LVPECL Output section. | 8/11/04 |
| B | T1<br>T9 | 1<br>2<br>16 | Features section - added Lead-Free bullet.<br>Pin Description Table - corrected CLK_SEL description.<br>Ordering Information Table - added ""Lead-Free"" part number for TSSOP package. | 3/22/05 |
| C | T5 | 1<br>5 | Features section - changed Part-to-Part Skew from 250ps max. to 350ps max.<br>AC Characteristics table - changed Part-to-Part Skew from 250ps max. to 350ps max. | 5/24/05 |
| D | T4D | 5<br>8 | LVPECL DC Characteristics Table - changed $V_{OH}$ max from $V_{CC}$ - 1.0V to $V_{CC}$ - 0.9V.<br>Application Information Section - added Recommendations for Unused Input and Output Pins. | 9/23/05 |
| E | T4C<br>T5<br><br>T9 | 4<br>5<br>9<br>17 | Differential DC Characteristics Table - corrected typo in $I_{IH}$ row, nCLKx to 5uA from 150uA.<br>Added thermal note to AC Characteristics Table.<br>Updated “Wiring the Differential Input to Accept Single-ended Levels” section.<br>Ordering Information Table - added LF marking for SOIC package.<br>Converted datasheet format. | 4/16/10 |
| E | T9 | 17 | Ordering Information Table - corrected package in the Package Column. | 5/4/10 |
| F | T5<br><br><br><br><br><br>T9 | 1<br>5<br><br>6-7<br>8<br>10<br>12<br>19 | Features Section - updated packaging bullet. Deleted RMS Phase Noise bullet<br>AC Characteristics Table - removed RMS Phase Noise specification, and added Buffer Additive Phase Jitter specifications.<br>Removed RMS Phase Noise Plot, and replaced with Additive Phase Jitter plots.<br>Parameter Measurement Information - corrected Phase Noise diagram.<br>Updated *Wiring the Differential Inputs to Accept Single-ended Levels* application note.<br>Added *2.5V Differential Clock Input Interface* application note.<br>Ordering Information Table - deleted leaded parts, deleted tape and reel count. | 9/16/13 |

# We've Got Your Timing Solution


6024 Silver Creek Valley Road
San Jose, California 95138

**Sales**
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

**Technical Support Sales**
netcom@idt.com
+480-763-2056