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LOW SKEW, 1-TO-4, CRYSTAL OSCILLATOR/ DIFFERENTIAL-TO-3.3V LVPECL FANOUT BUFFER

ICS8533I-31

General Description

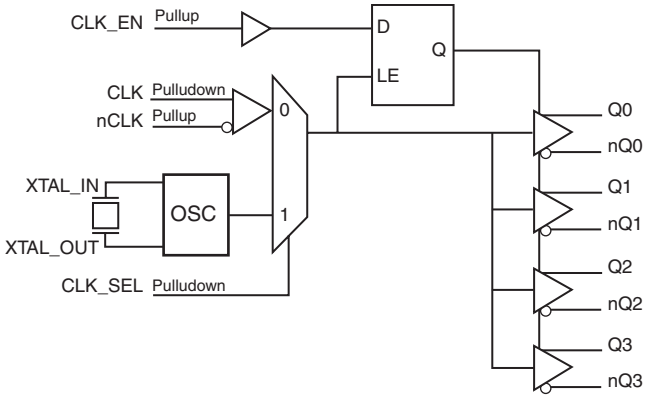
The ICS8533I-31 is a low skew, high performance 1-to-4 Crystal Oscillator/Differential-to-3.3V LVPECL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS8533I-31 has selectable differential clock or crystal inputs. The CLK, nCLK pair can accept most standard differential input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS8533I-31 ideal for those applications demanding well defined performance and repeatability.

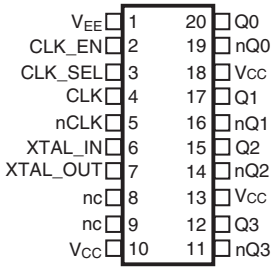
Features

- Four differential LVPECL output pairs
- Selectable differential CLK/nCLK or crystal oscillator interface
- Maximum output frequency: 650MHz
- Translates any single-ended input signal to 3.3V LVPECL levels with resistor bias on nCLK input
- Additive phase jitter, RMS: TBD
- Output skew: 25ps (typical)
- Part-to-part skew: 150ps (typical)
- Propagation delay: 1.5ns (typical)
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS8533I-31
20-Lead TSSOP
6.5mm x 4.4mm x 0.925mm
package body

G Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{EE}	Power		Negative supply pin.
2	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follows clock input. When LOW, Q outputs are forced low, nQ outputs are forced high. LVCMOS / LVTTL interface levels.
3	CLK_SEL	Input	Pulldown	Clock select input. When LOW, selects CLK, nCLK input. When HIGH, selects XTAL input. LVCMOS / LVTTL interface levels.
4	CLK	Input	Pulldown	Non-inverting differential clock input.
5	nCLK	Input	Pullup	Inverting differential clock input.
6, 7	XTAL_IN XTAL_OUT	Input		Crystal oscillator interface XTAL_IN is the input, XTAL_OUT is the output.
8, 9	nc	Unused		No connect.
10, 13, 18	V_{CC}	Power		Power supply pins.
11, 12	nQ3, Q3	Output		Differential clock output pair. LVPECL interface levels.
14, 15	nQ2, Q2	Output		Differential clock output pair. LVPECL interface levels.
16, 17	nQ1, Q1	Output		Differential clock output pair. LVPECL interface levels.
19, 20	nQ0, Q0	Output		Differential clock output pair. LVPECL interface levels.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Control Input Function Table

Inputs			Outputs	
CLK_EN	**CLK_SEL**	**Selected Source**	**Q0:Q3**	**nQ0:nQ3**
0	0	CLK, nCLK	Disabled; Low	Disabled; High
0	1	XTAL_IN, XTAL_OUT	Disabled; Low	Disabled; High
1	0	CLK, nCLK	Enabled	Enabled
1	1	XTAL_IN, XTAL_OUT	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock or crystal oscillator edge as shown in Figure 1. In the active mode, the state of the outputs are a function of the CLK, nCLK and XTAL inputs as described in Table 3B.

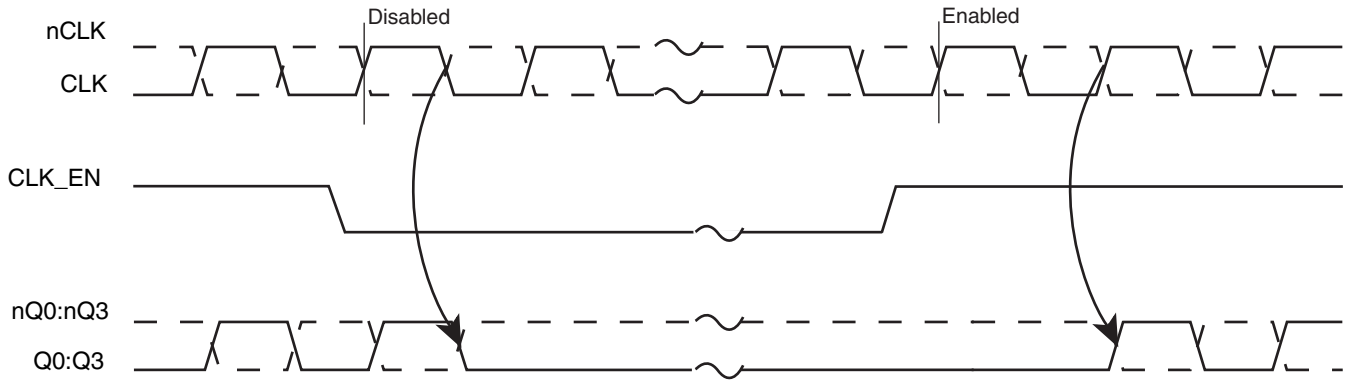


Figure 1. CLK_EN Timing Diagram

Table 3B. Clock Input Function Table

Inputs		Outputs			
CLK	**nCLK**	**Q0:Q3**	**nQ0:nQ3**	**Input to Output Mode**	**Polarity**
0	1	LOW	HIGH	Differential to Differential	Non inverting
1	0	HIGH	LOW	Differential to Differential	Non inverting
0	Biased; NOTE 1	LOW	HIGH	Single-ended to Differential	Non inverting
1	Biased; NOTE 1	HIGH	LOW	Single-ended to Differential	Non inverting
Biased; NOTE 1	0	HIGH	LOW	Single-ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single-ended to Differential	Inverting

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O Continuos Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	91.12°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{EE} = 3.3V ± 5%, V_{CC} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current			40		mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{EE} = 3.3V ± 5%, V_{CC} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK_EN	V_{CC} = V_{IN} = 3.465V			5	µA
		CLK_SEL	V_{CC} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	CLK_EN	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
		CLK_SEL	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA

Table 4C. Differential DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK	$V_{CC} = V_{IN}$ = 3.465V			5	µA
		CLK	$V_{CC} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	nCLK	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
		CLK	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

Table 4D. LVPECL DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} – 1.4		V_{CC} – 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} – 2.0		V_{CC} – 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Output termination with 50Ω to V_{CC} – 2V.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		14		25	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

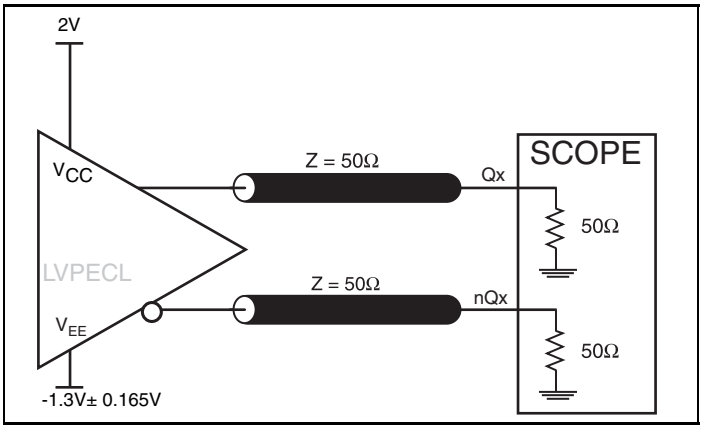
AC Electrical Characteristics

Table 6. AC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

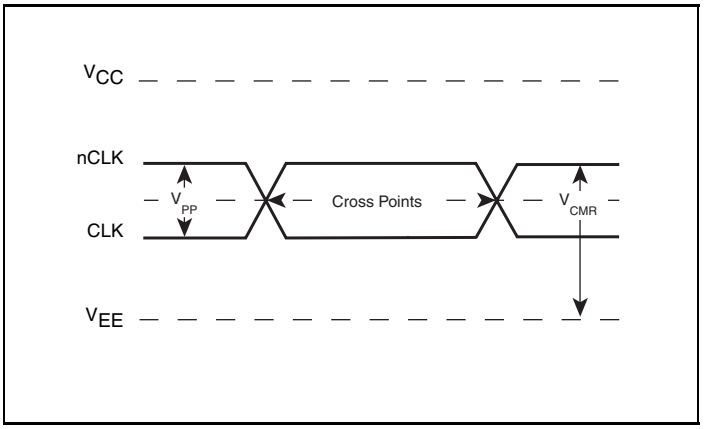
Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				650	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 650MHz		1.5		ns
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	650MHz, (Integration Range: 1.875MHz – 20MHz)		TBD		ps
*t*sk(o)	Output Skew; NOTE 2, 5			25		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5			150		ps
t_R / t_F	Output Rise/Fall Time	20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle			50		%

All parameters measured at 500MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions.
Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: Measured using CLK. For XTAL input, refer to Application Note.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

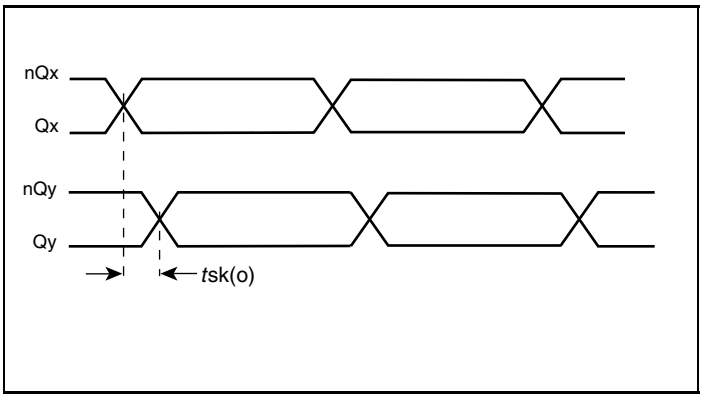
Parameter Measurement Information



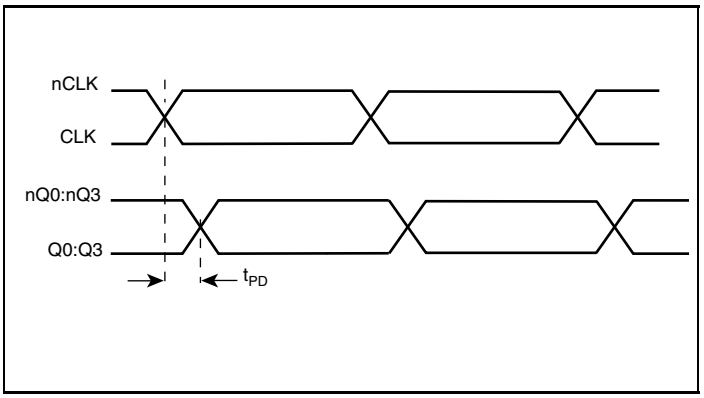
3.3V LVPECL Output Load AC Test Circuit



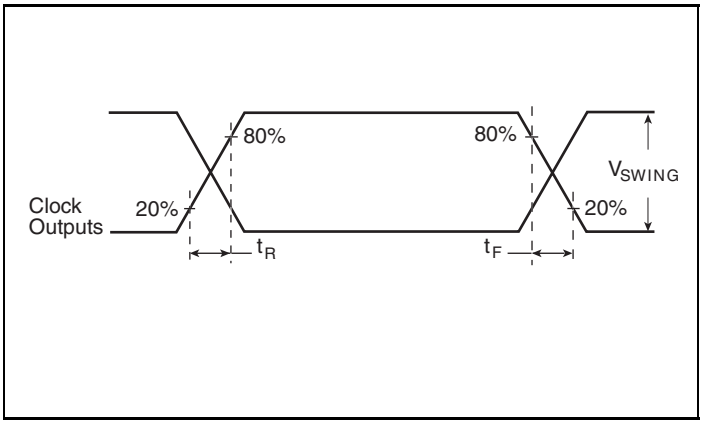
Differential Input Level



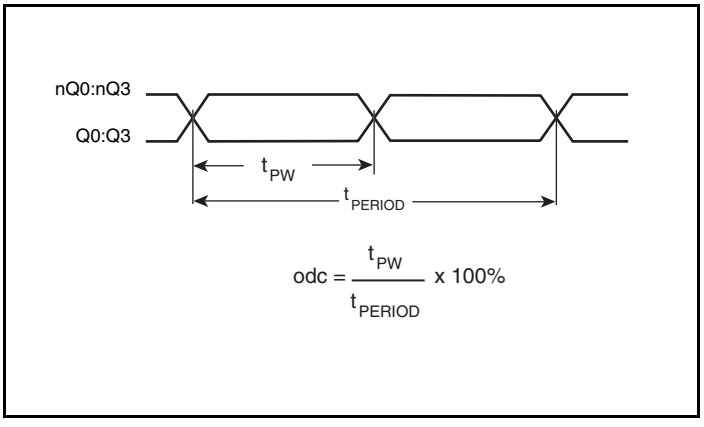
Output Skew



Propagation Delay



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how the differential input can be wired to accept single-ended levels. The reference voltage V_REF = V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

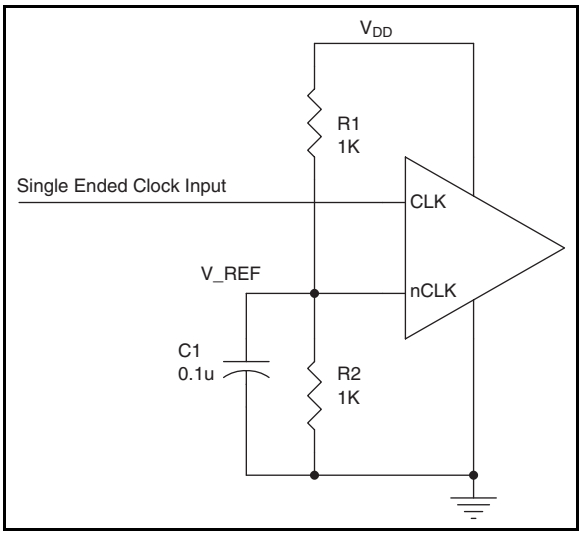


Figure 2. Single-Ended Signal Driving Differential Input

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

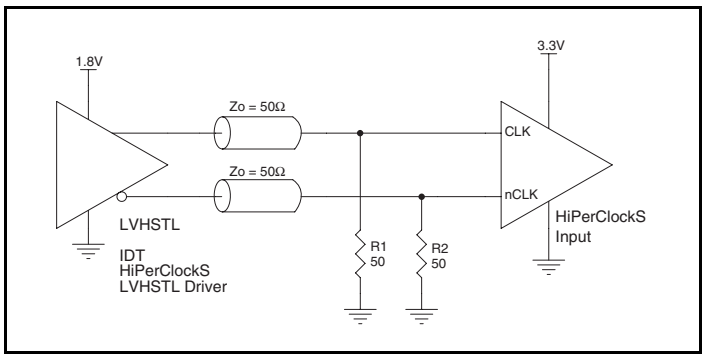


Figure 3A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

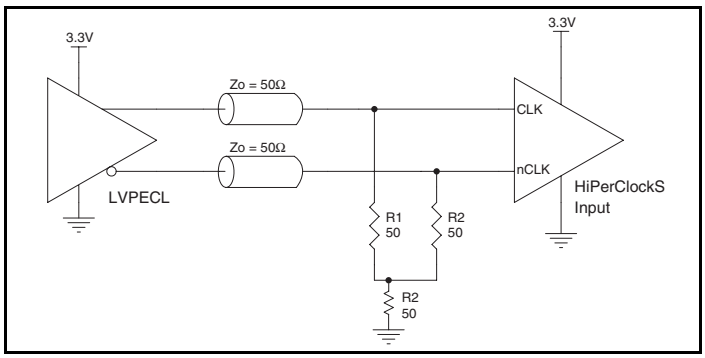


Figure 3B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

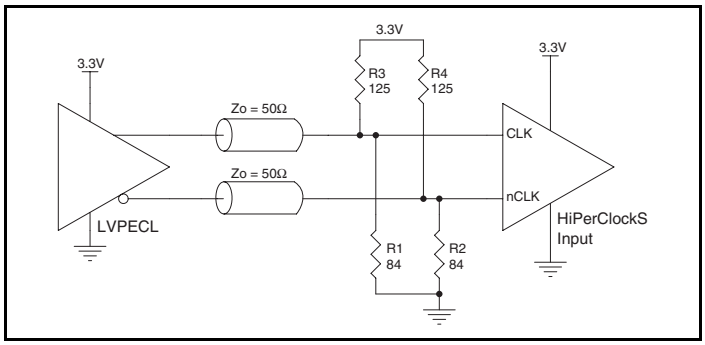


Figure 3C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

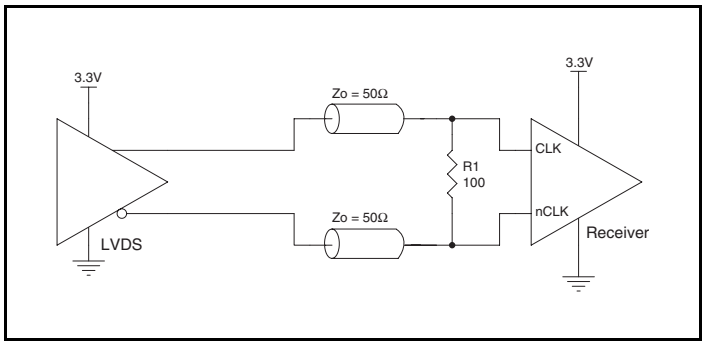


Figure 3D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

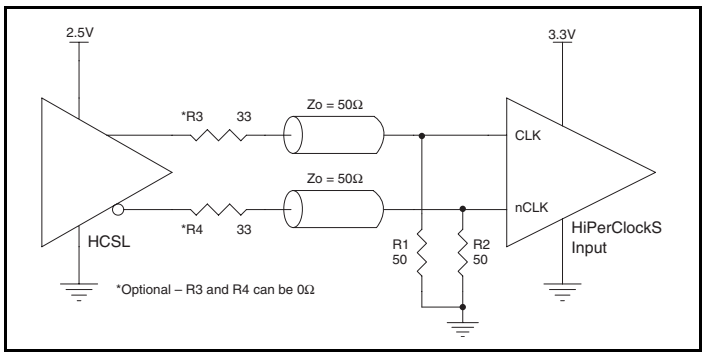


Figure 3E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver

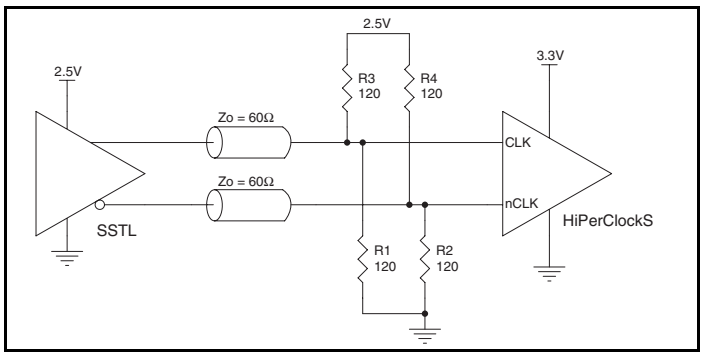


Figure 3F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver

Crystal Input Interface

A crystal can be characterized for either series or parallel mode operation. The ICS8533I-31 fanout buffer has a built-in crystal oscillator circuit. This interface can accept either a series or parallel crystal without additional components as shown in *Figure 4.* The physical location of the crystal should be located as close as possible to the XTAL_IN and XTAL_OUT pins. The experiments show that using a 19.44MHz crystal results in an output frequency of 19.4404746MHz and approximately 44% of duty cycle.

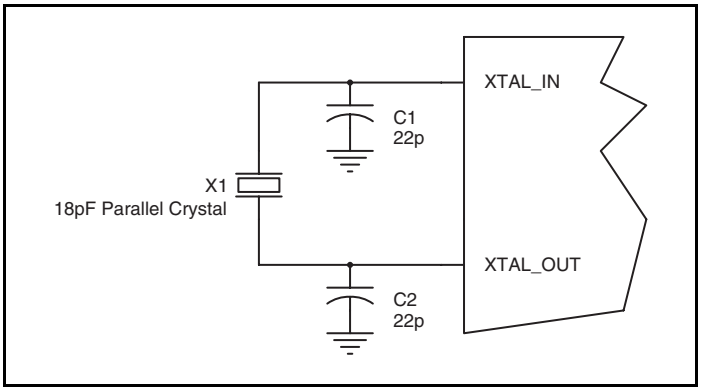


Figure 4. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 5.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

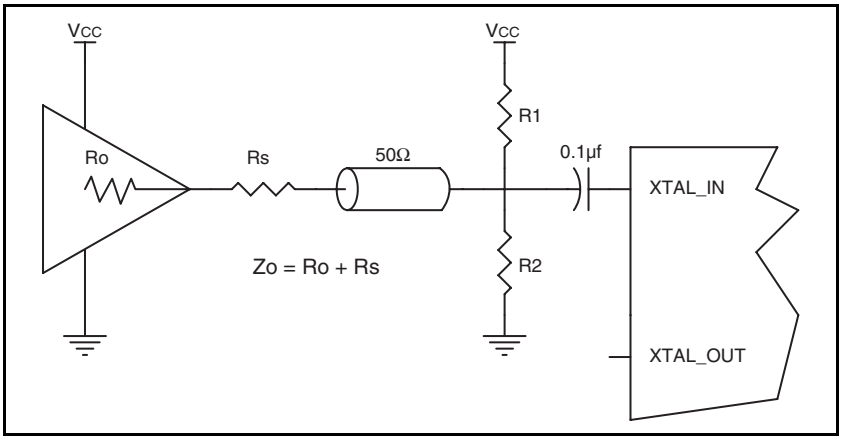


Figure 5. General Diagram for LVCMOS Driver to XTAL Input Interface

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 6A and 6B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

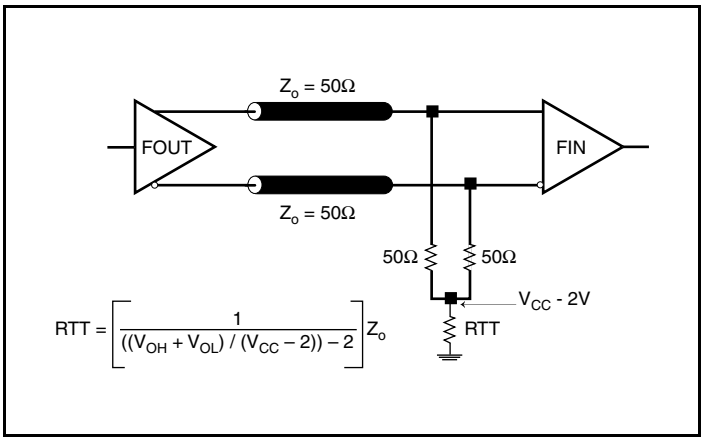


Figure 6A. 3.3V LVPECL Output Termination

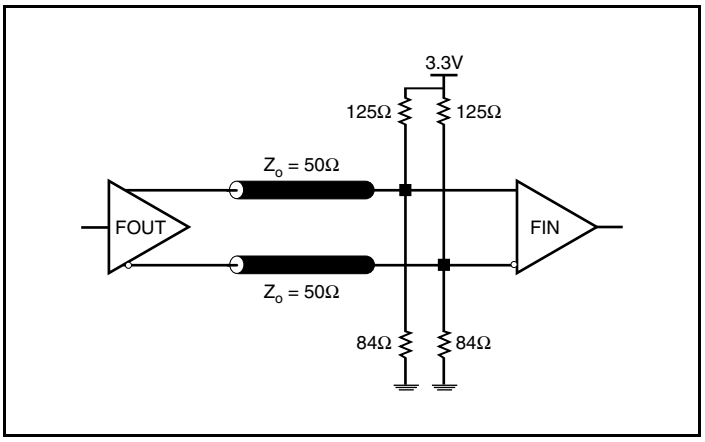


Figure 6B. 3.3V LVPECL Output Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8533I-31.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8533I-31 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 40mA = **138.6mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 30mW = **120mW**

Total Power$_{\_MAX}$ (3.3V, with all outputs switching) = 138.6mW + 60mW = **258.6mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 91.1°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.259W * 91.1°C/W = 108.6°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 7. Thermal Resistance θ_{JA} for 16 Lead TSSOP, Forced Convection

θ_{JA} **vs. Air Flow**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	91.1°C/W	86.7°C/W	84.6°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7.*

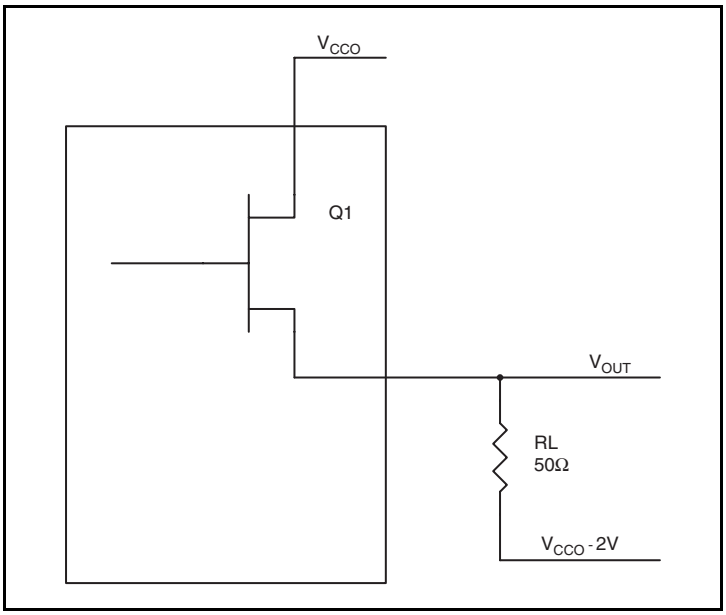


Figure 7. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} – 0.9V$
  $(V_{CC\_MAX} – V_{OH\_MAX}) =$ **0.9V**
- For logic low, $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} – 1.7V$
  $(V_{CC\_MAX} – V_{OL\_MAX}) =$ **1.7V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.9V)/50Ω] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_{L]} * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.7V)/50Ω] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 20 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	91.1°C/W	86.7°C/W	84.6°C/W

Transistor Count

The transistor count for ICS8533I-31 is: TBD

Package Outline and Package Dimensions

Package Outline - G Suffix for 20-Lead TSSOP

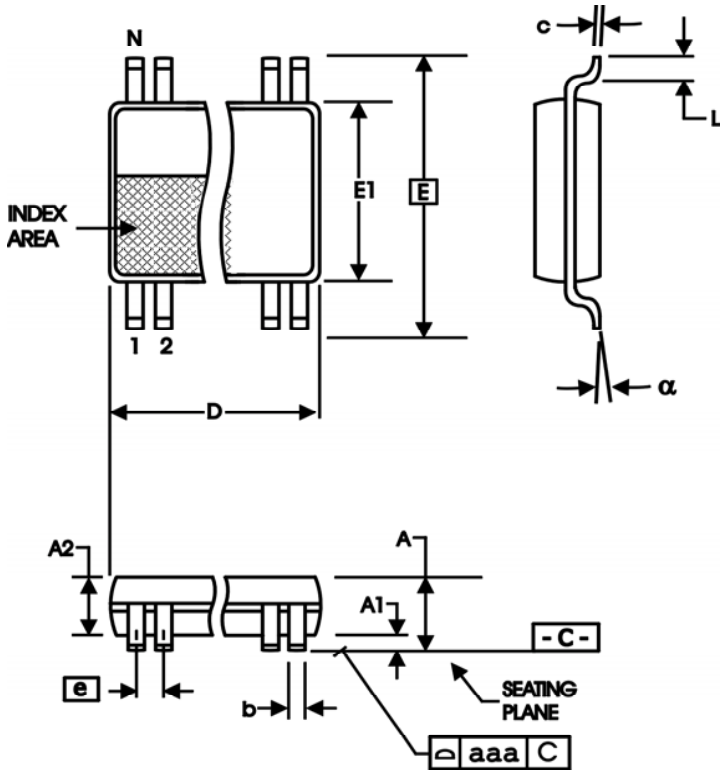


Table 9. Package Dimensions for 20 Lead TSSOP

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	20	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8533AGI-31	ICS8533AGI31	20 Lead TSSOP	Tube	-40°C to 85°C
8533AGI-31T	ICS8533AGI31	20 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C
8533AGI-31LF	TBD	“Lead-Free” 20 Lead TSSOP	Tube	-40°C to 85°C
8533AGI-31LFT	TBD	“Lead-Free” 20 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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