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Integrated Circuit Systems, Inc.

ICS85357I-01

4:1 OR 2:1 DIFFERENTIAL-TO-3.3V LVPECL / ECL CLOCK MULTIPLEXER

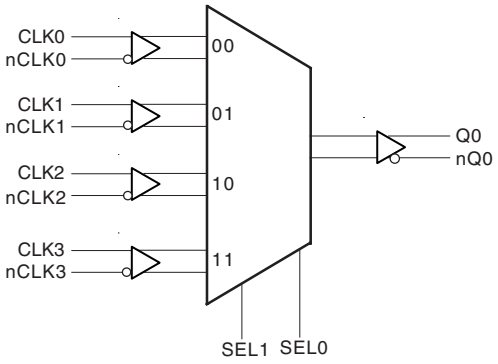
GENERAL DESCRIPTION

The ICS85357I-01 is a 4:1 or 2:1 Differential-to-3.3V LVPECL / ECL clock multiplexer which can operate up to 750MHz and is a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS85357I-01 has 4 selectable clock inputs. The CLK, nCLK pair can accept most standard differential input levels. The device can operate using a 3.3V LVPECL (V_{EE} = 0V, V_{CC} = 3.135V to 3.465V) or 3.3V ECL (V_{CC} = 0V, V_{EE} = -3.135V to -3.465V). The fully differential architecture and low propagation delay make it ideal for use in clock distribution circuits. The select pins have internal pulldown resistors. Leaving one input unconnected (pulled to logic low by the internal resistor) will transform the device into a 2:1 multiplexer. The SEL1 pin is the most significant bit and the binary number applied to the select pins will select the same numbered data input (i.e., 00 selects CLK0, nCLK0).

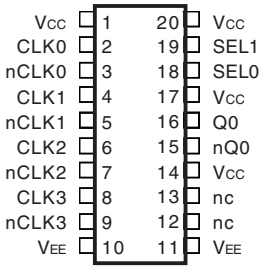
FEATURES

- High speed differential multiplexer. The device can be configured as either a 4:1 or 2:1 multiplexer
- 1 differential 3.3V LVPECL output
- 4 selectable CLK, nCLK inputs
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency: 750MHz
- Translates any single ended input signal to 3.3V LVPECL levels with resistor bias on nCLKx input
- Part-to-part skew: 415ps (maximum)
- Propagation delay: 1.5ns (maximum)
- LVPECL mode operating voltage supply range: V_{CC} = 3.135V to 3.465V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3.135V to -3.465V
- -40°C to 85°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS85357I-01
20-Lead TSSOP
4.40mm x 6.50mm x 0.90mm body package
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 14, 17, 20	V_{CC}	Power		Positive supply pins.
2	CLK0	Input	Pulldown	Non-inverting differential clock input.
3	nCLK0	Input	Pullup	Inverting differential clock input.
4	CLK1	Input	Pulldown	Non-inverting differential clock input.
5	nCLK1	Input	Pullup	Inverting differential clock input.
6	CLK2	Input	Pulldown	Non-inverting differential clock input.
7	nCLK2	Input	Pullup	Inverting differential clock input.
8	CLK3	Input	Pulldown	Non-inverting differential clock input.
9	nCLK3	Input	Pullup	Inverting differential clock input.
10, 11	V_{EE}	Power		Negative supply pins.
12, 13	nc	Unused		No connect.
15, 16	nQ0, Q0	Output		Differential output pairs. LVPECL interface levels.
18	SEL0	Input	Pulldown	Clock select input. LVCMOS / LVTTL interface levels.
19	SEL1	Input	Pulldown	Clock select input. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ

TABLE 3. CONTROL INPUT FUNCTION TABLE

Inputs		Clock Out
SEL1	SEL0	CLK
0	0	CLK0, nCLK0
0	1	CLK1, nCLK1
1	0	CLK2, nCLK2
1	1	CLK3, nCLK3

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	73.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA= -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				35	mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA= -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	SEL0, SEL1		2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	SEL0, SEL1		-0.3		0.8	V
I_{IH}	Input High Current	SEL0, SEL1	V_{CC} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	SEL0, SEL1	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA= -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0, CLK1, CLK2, CLK3	V_{CC} = V_{IN} = 3.465V			150	µA
		nCLK0, nCLK1, nCLK2, nCLK3	V_{CC} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	CLK0, CLK1, CLK2, CLK3	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK0, nCLK1, nCLK2, nCLK3	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} - 0.85	V

NOTE 1: Common mode input voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLKx, nCLKx is V_{CC} + 0.3V.

TABLE 4D. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA= -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.4		V_{CC} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} -1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

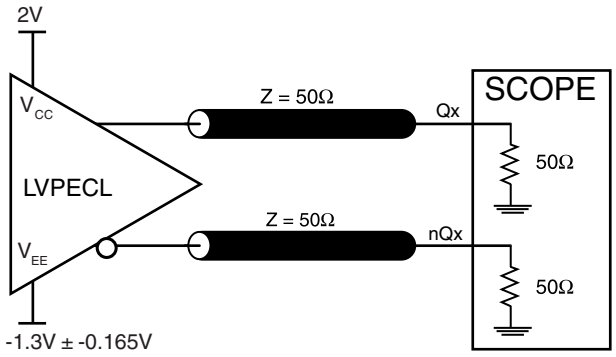
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 5. AC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA= -40°C TO 85°C

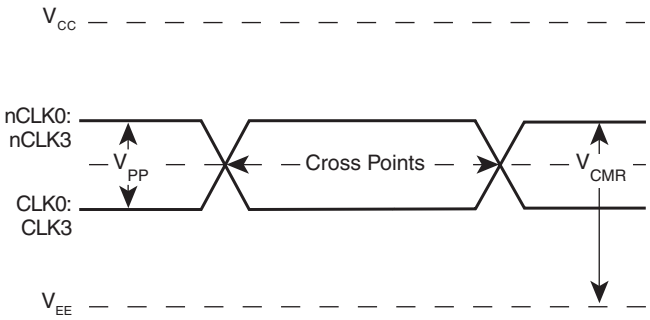
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency				750	MHz
t_{PD}	Propagation Delay; NOTE 1		1		1.5	ns
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				415	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		46		54	%

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

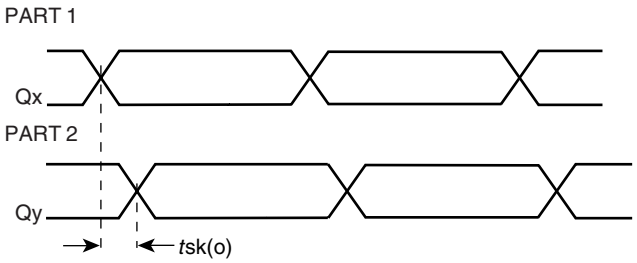
PARAMETER MEASUREMENT INFORMATION



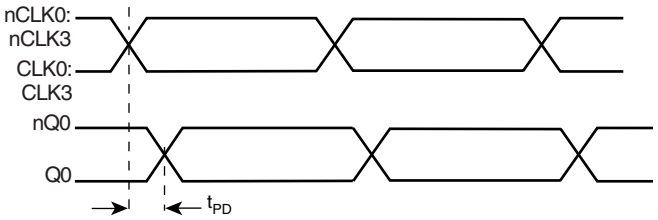
3.3V OUTPUT LOAD AC TEST CIRCUIT



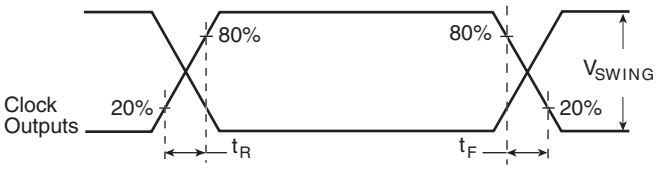
DIFFERENTIAL INPUT LEVEL



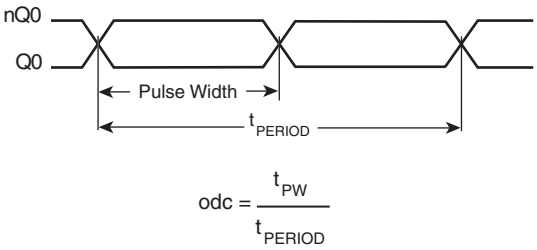
PART-TO-PART SKEW



PROPAGATION DELAY



OUTPUT RISE/FALL TIME



OUTPUT DUTY CYLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF ~ V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

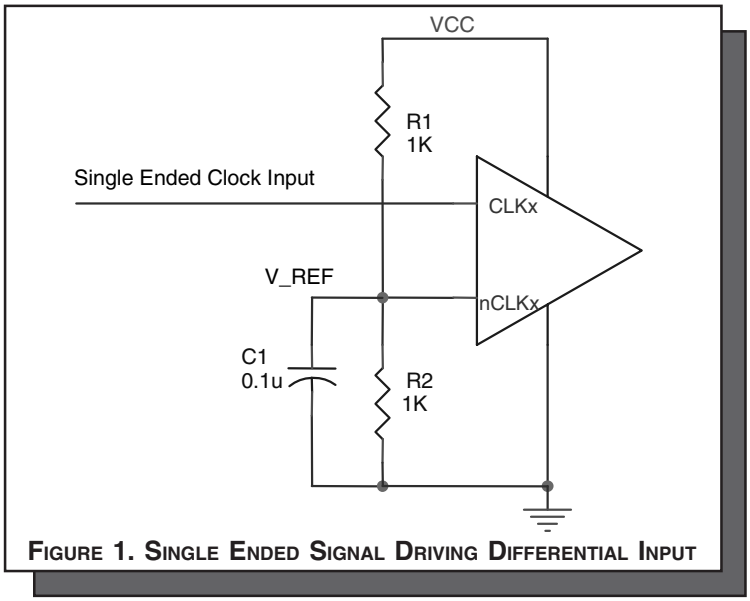


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

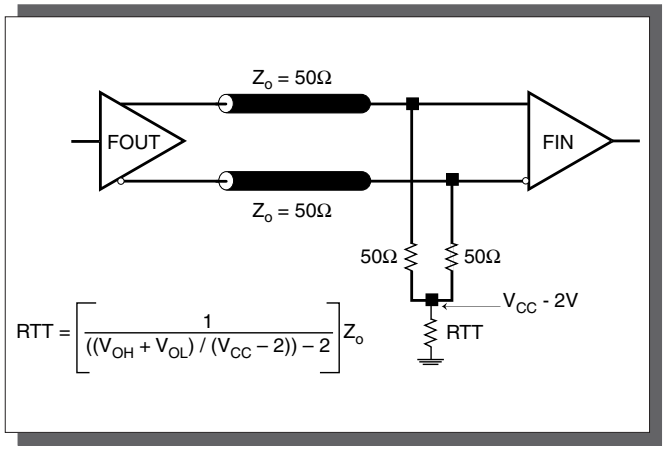


FIGURE 2A. LVPECL OUTPUT TERMINATION

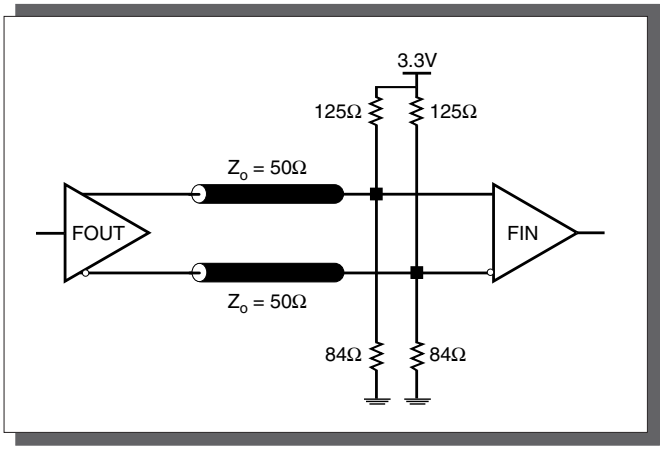


FIGURE 2B. LVPECL OUTPUT TERMINATION

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 4A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

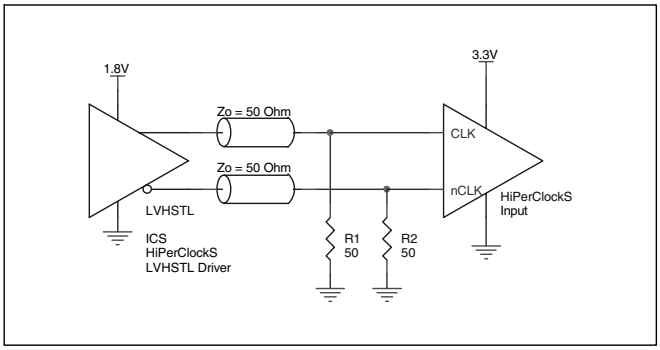


FIGURE 3A. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY ICS HIPERCLOCKS LVHSTL DRIVER

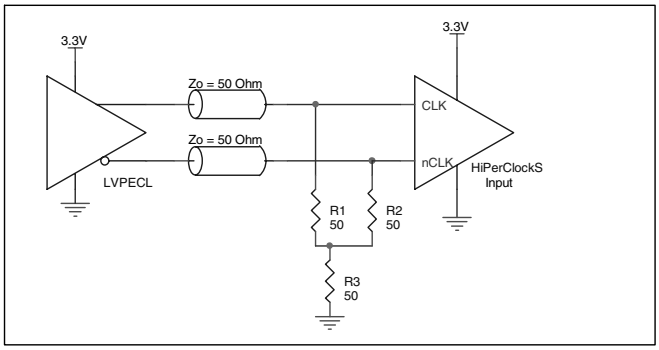


FIGURE 3B. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

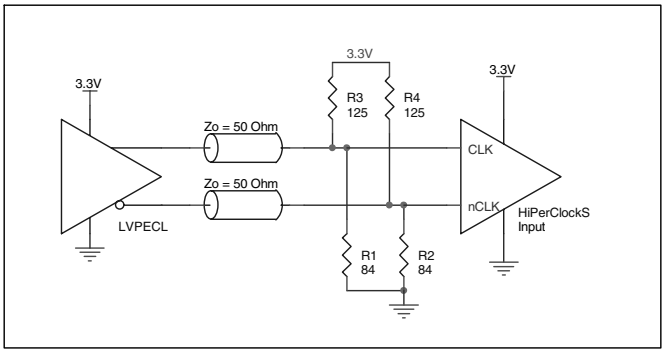


FIGURE 3C. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

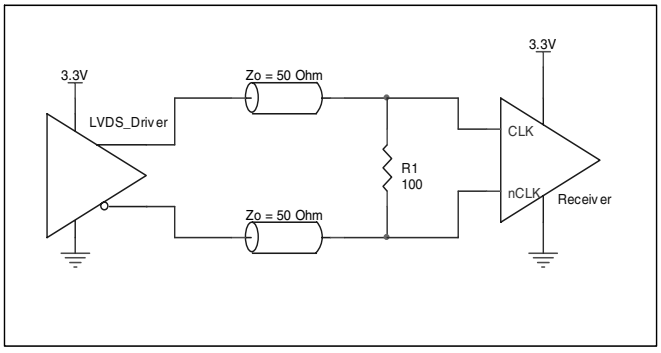


FIGURE 3D. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

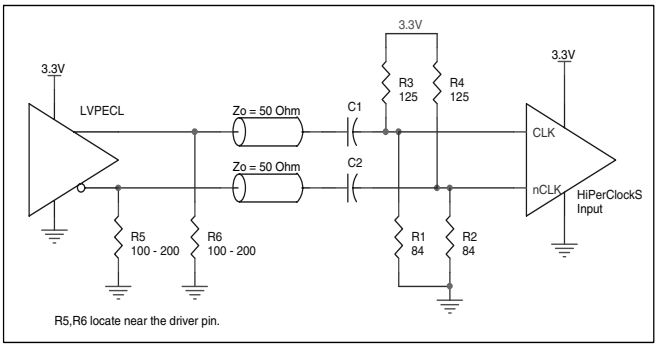


FIGURE 3E. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS85357I-01.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS85357I-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 35mA = **121.3mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 1 * 30mW = **30mW**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 121.3mW + 30mW = **151.3mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.151W * 66.6°C/W = 95.05°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 20-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

LVPECL output driver circuit and termination are shown in *Figure 4.*

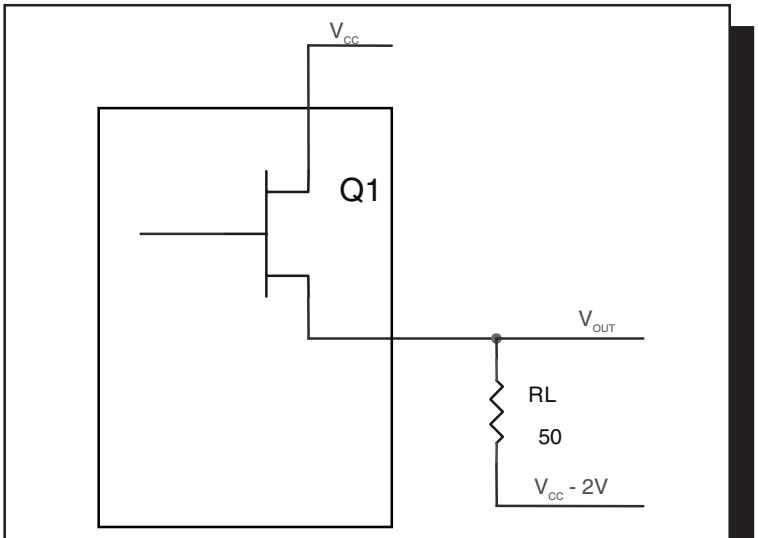


FIGURE 4. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 0.9V}$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.7V}$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50Ω] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50Ω] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 20 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS85357I-01 is: 400

PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP

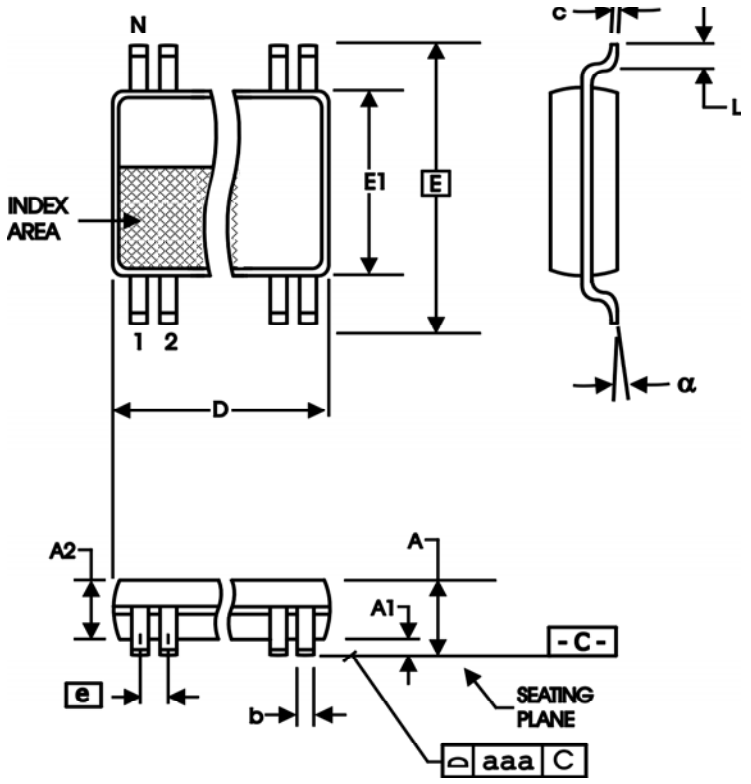


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS85357AGI-01	ICS85357AI01	20 lead TSSOP	74 per tube	-40°C to 85°C
ICS85357AGI-01T	ICS85357AI01	20 lead TSSOP on Tape and Reel	2500	-40°C to 85°C