Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!


# Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

## General Description

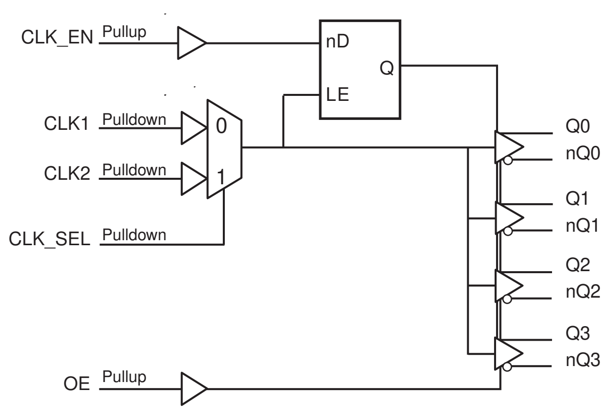
The 8545I-02 is a low skew, high performance 1-to-4 LVCMOS/LVTTL-to-LVDS Clock Fanout Buffer. Utilizing Low Voltage Differential Signaling (LVDS) the 8545I-02 provides a low power, low noise, solution for distributing clock signals over controlled impedances of 100Ω. The 8545I-02 accepts an LVCMOS/LVTTL input level and translates it to 3.3V LVDS output levels.

Guaranteed output and part-to-part skew characteristics make the 8545I-02 ideal for those applications demanding well defined performance and repeatability.

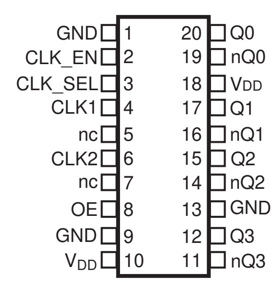
## Features

- Four differential LVDS output pairs
- Two LVCMOS/LVTTL clock inputs to support redundant or selectable frequency fanout applications
- Maximum output frequency: 350MHz
- Translates LVCMOS/LVTTL input signals to LVDS levels
- Output skew: 60ps (maximum)
- Part-to-part skew: 450ps (maximum)
- Propagation delay: 1.45ns (maximum)
- Additive phase jitter, RMS: 0.14ps (typical)
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

## Block Diagram




## Pin Assignment




**8545I-02**

**20-Lead TSSOP**
**6.5mm x 4.4mm x 0.925mm package body**
**G Package**
**Top View**

## Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1, 9, 13 | GND | Power | | Power supply ground. |
| 2 | CLK_EN | Input | Pullup | Synchronizing clock enable. When HIGH, clock outputs follows clock input. When LOW, Qx outputs are forced low, nQx outputs are forced high. LVCMOS / LVTTL interface levels. |
| 3 | CLK_SEL | Input | Pulldown | Clock select input. When HIGH, selects CLK2 input. When LOW, selects CLK1 input. LVCMOS / LVTTL interface levels. |
| 4 | CLK1 | Input | Pulldown | Single-ended clock input. LVCMOS/LVTTL interface levels. |
| 5, 7 | nc | Unused | | No connect. |
| 6 | CLK2 | Input | Pulldown | Single-ended clock input. LVCMOS/LVTTL interface levels. |
| 8 | OE | Input | Pullup | Output enable. Controls enabling and disabling of outputs Q0/nQ0 through Q3/nQ3. LVCMOS/LVTTL interface levels. |
| 10, 18 | $V_{DD}$ | Power | | Positive supply pins. |
| 11, 12 | nQ3, Q3 | Output | | Differential output pair. LVDS interface levels. |
| 14, 15 | nQ2, Q2 | Output | | Differential output pair. LVDS interface levels. |
| 16, 17 | nQ1, Q1 | Output | | Differential output pair. LVDS interface levels. |
| 19, 20 | nQ0, Q0 | Output | | Differential output pair. LVDS interface levels. |

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

## Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | kΩ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | kΩ |

# Function Tables

**Table 3A. Control Input Function Table**

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| **OE** | **CLK_EN** | **CLK_SEL** | **Selected Source** | **Q0:Q3** | **nQ0:nQ3** |
| 0 | X | X | | High-Impedance | High-Impedance |
| 1 | 0 | 0 | CLK1 | Low | High |
| 1 | 0 | 1 | CLK2 | Low | High |
| 1 | 1 | 0 | CLK1 | Active | Active |
| 1 | 1 | 1 | CLK2 | Active | Active |

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1. In the active mode, the state of the outputs are a function of the CLK1 and CLK2 inputs as described in Table 3B.

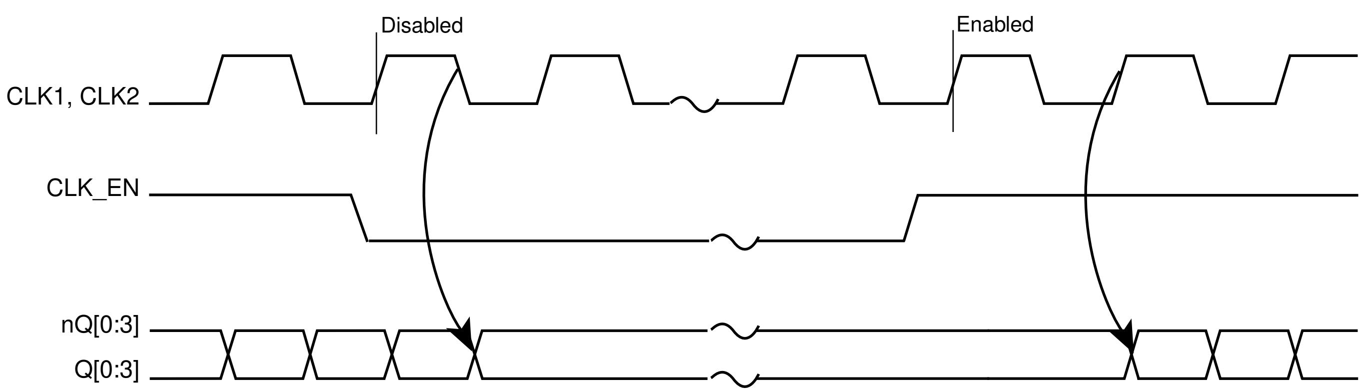



**Figure 1. CLK_EN Timing Diagram**

**Table 3B. Clock Input Function Table**

| Inputs | Outputs | |
|---|---|---|
| **CLK1 or CLK2** | **Q0:Q3** | **nQ0:nQ3** |
| 0 | LOW | HIGH |
| 1 | HIGH | LOW |

# Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|---|
| Supply Voltage, $V_{DD}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{DD}$ + 0.5V |
| Outputs, $I_O$<br>Continuos Current<br>Surge Current | <br>10mA<br>15mA |
| Package Thermal Impedance, $\theta_{JA}$ | 91.1°C/W (0 mps) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

# DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Positive Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{DD}$ | Power Supply Current | | | | 90 | mA |

**Table 4B. LVCMOS/LVTTL DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | 2 | | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | | -0.3 | | 0.8 | V |
| $I_{IH}$ | Input High Current | CLK1, CLK2, CLK_SEL | $V_{DD} = V_{IN}$ = 3.465V | | | 150 | µA |
| | | OE, CLK_EN | $V_{DD} = V_{IN}$ = 3.465V | | | 5 | µA |
| $I_{IL}$ | Input Low Current | CLK1, CLK2, CLK_SEL | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -5 | | | µA |
| | | OE, CLK_EN | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | µA |

**Table 4C. LVDS DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OD}$ | Differential Output Voltage | | 275 | | 525 | mV |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change | | | | 50 | mV |
| $V_{OS}$ | Offset Voltage | | 1.1 | 1.25 | 1.4 | V |
| $\Delta V_{OS}$ | $V_{OS}$ Magnitude Change | | | 5 | 50 | mV |

# AC Electrical Characteristics

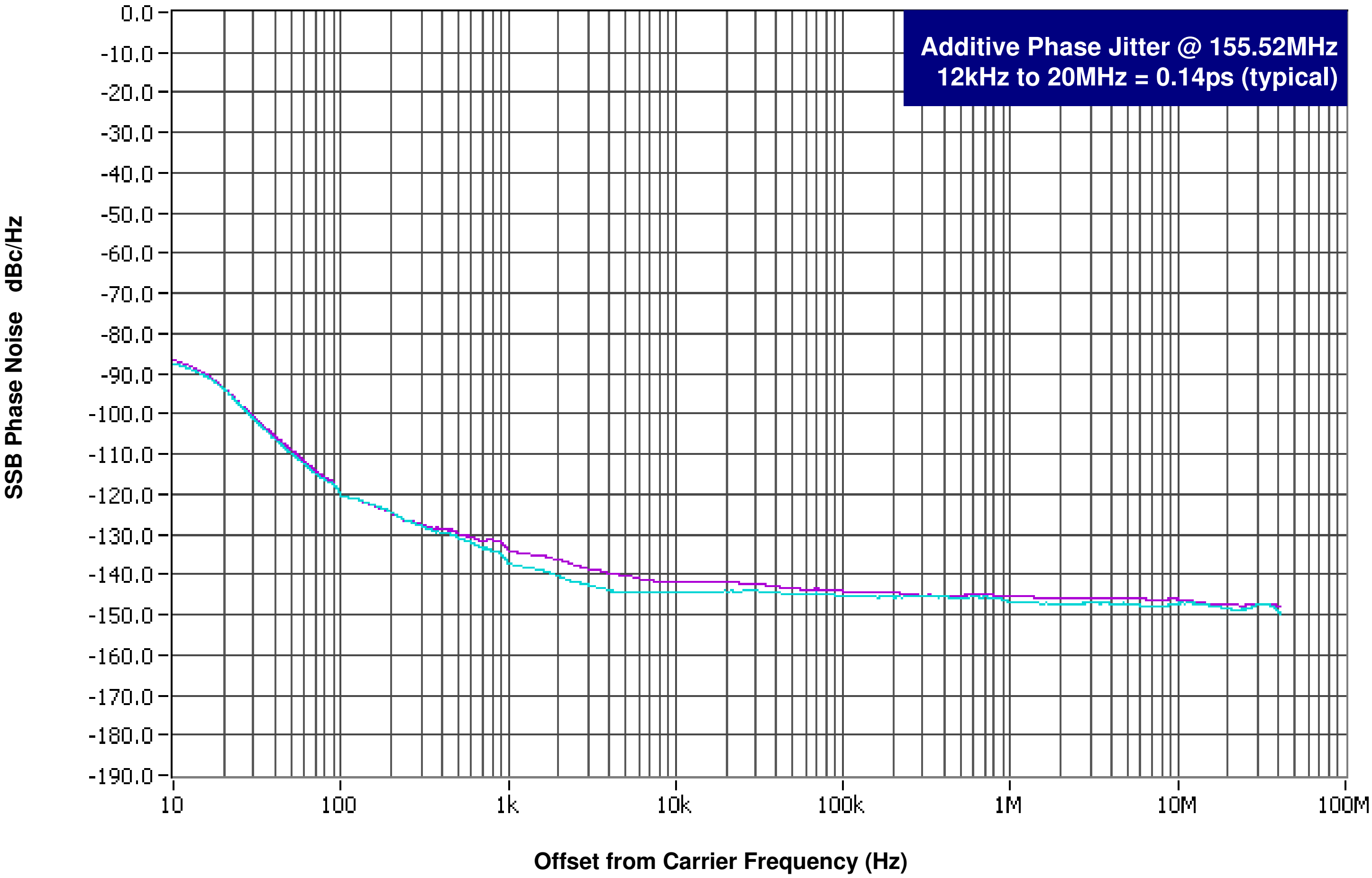
**Table 5. AC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | | | | 350 | MHz |
| $t_{PD}$ | Propagation Delay; NOTE 1 | | 1.0 | | 1.45 | ns |
| *t*jit | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section | 155.52MHz, Integration Range: 12kHz – 20MHz | | 0.14 | | ps |
| *t*sk(o) | Output Skew; NOTE 2, 4 | | | | 60 | ps |
| *t*sk(pp) | Part-to-Part Skew; NOTE 3, 4 | | | | 450 | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 150 | | 700 | ps |
| odc | Output Duty Cycle; NOTE 5 | $f \le$ 166MHz | 45 | | 55 | % |
| | | $f >$ 166MHz | 40 | | 60 | % |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
All parameters measured at $f_{MAX}$ unless noted otherwise.
NOTE 1: Measured from $V_{DD}$/2 of the input to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 5: Measured using 50% duty cycle.

# Additive Phase Jitter

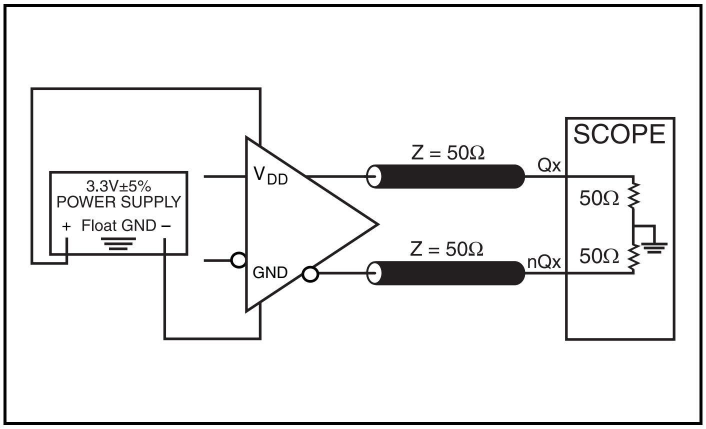
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



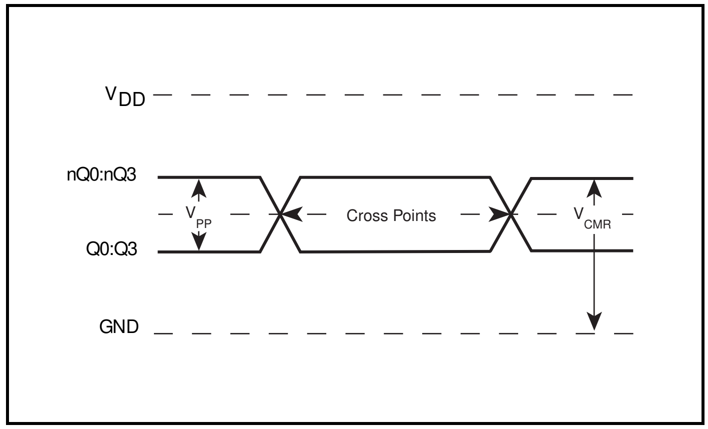

As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

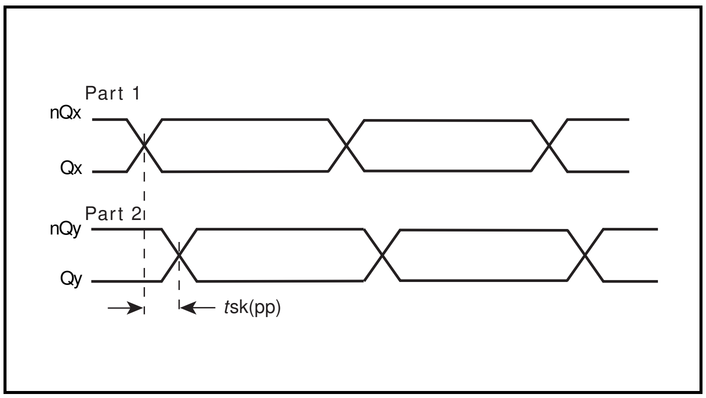
# Parameter Measurement Information



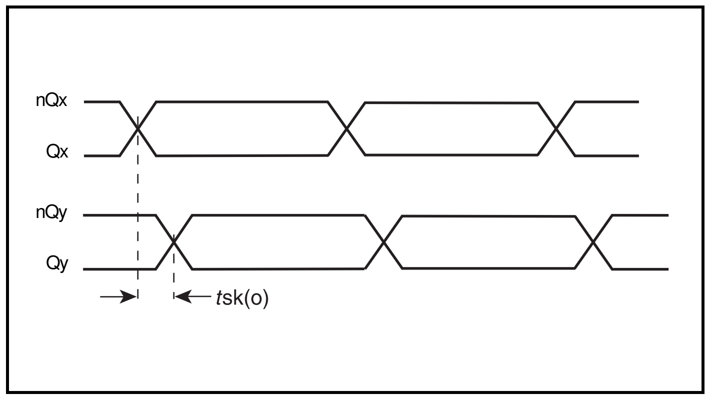

**3.3V LVDS Output Load AC Test Circuit**



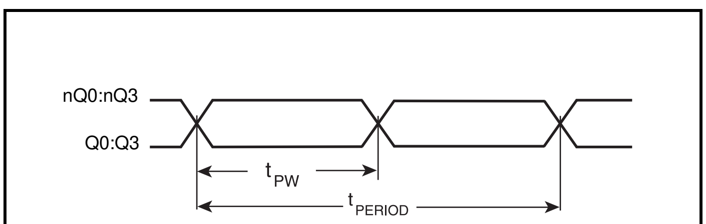

**Differential Output Level**




**Part-to-Part Skew**

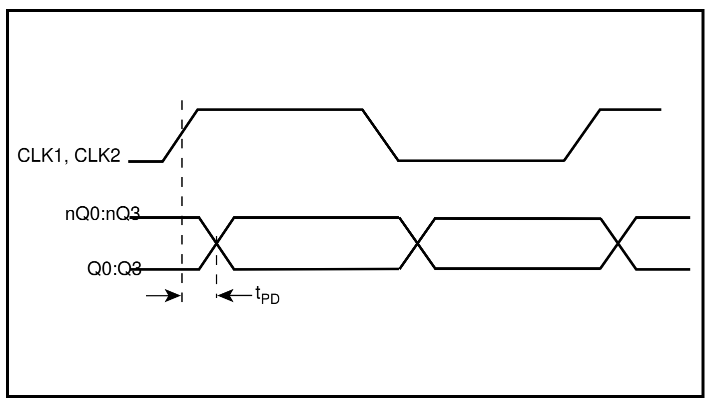



**Output Skew**



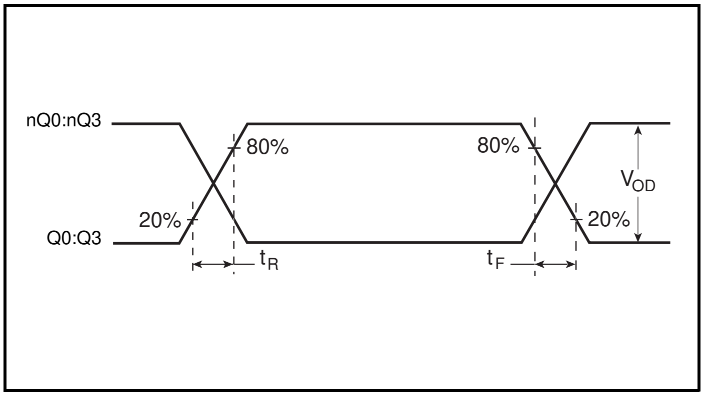

$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

**Output Duty Cycle/Pulse Width/Period**

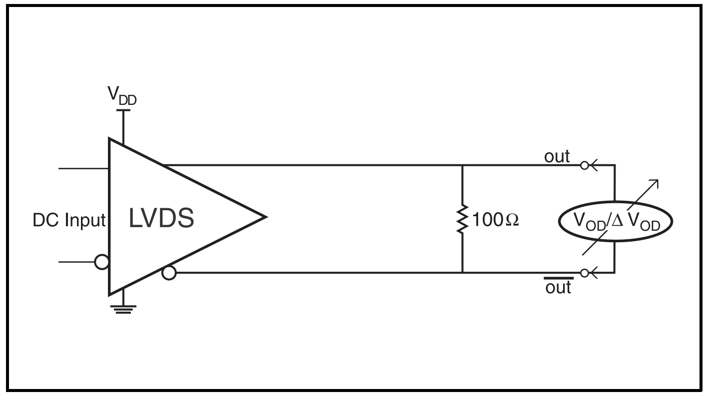



**Propagation Delay**

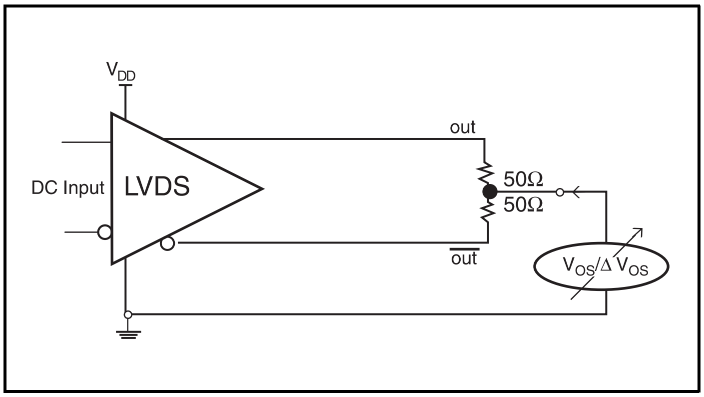
# Parameter Measurement Information, continued




**Output Rise/Fall Time**




**Differential Output Voltage Setup**




**Offset Voltage Setup**

# Application Information

## Recommendations for Unused Input and Output Pins

## Inputs:

### CLK Inputs

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

### LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

## Outputs:

### LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

## 3.3V LVDS Driver Termination

A general LVDS interface is shown in Figure 2. In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

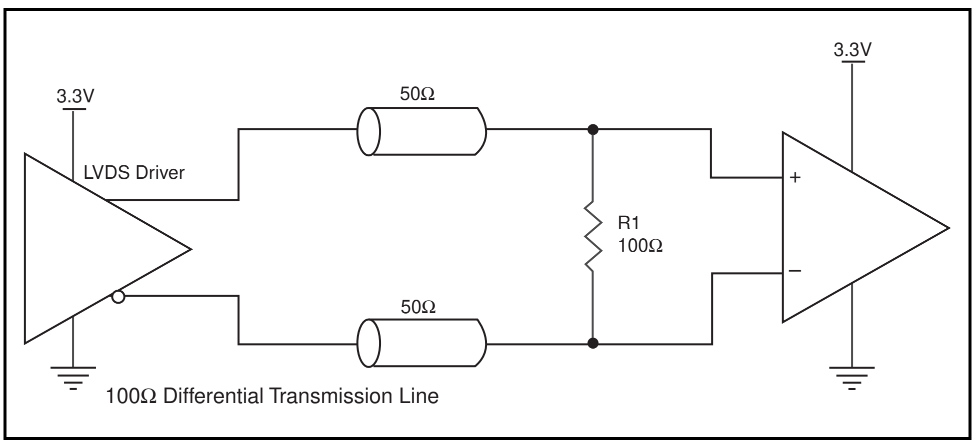



**Figure 2. Typical LVDS Driver Termination**

# Power Considerations

This section provides information on power dissipation and junction temperature for the 8545I-02.
Equations and example calculations are also provided.

## 1. Power Dissipation.

The total power dissipation for the 8545I-02 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for $V_{DD}$ = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD\_MAX}$ = 3.465V * 90mA = **311.85mW**

## 2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: Tj = $\theta_{JA}$ * Pd_total + $T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 91.1°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.312W * 91.1°C/W = 113.4°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

### Table 6. Thermal Resistance $\theta_{JA}$ for 20 Lead TSSOP, Forced Convection

| $\theta_{JA}$ by Velocity | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 91.1°C/W | 86.7°C/W | 84.6°C/W |

# Reliability Information

**Table 7. $\theta_{JA}$ vs. Air Flow Table for a 20 Lead TSSOP**

| $\theta_{JA}$ by Velocity | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 91.1°C/W | 86.7°C/W | 84.6°C/W |

## Transistor Count

The transistor count for 8545I-02 is: 360

# Package Outline and Package Dimensions

**Package Outline - G Suffix for 20 Lead TSSOP**

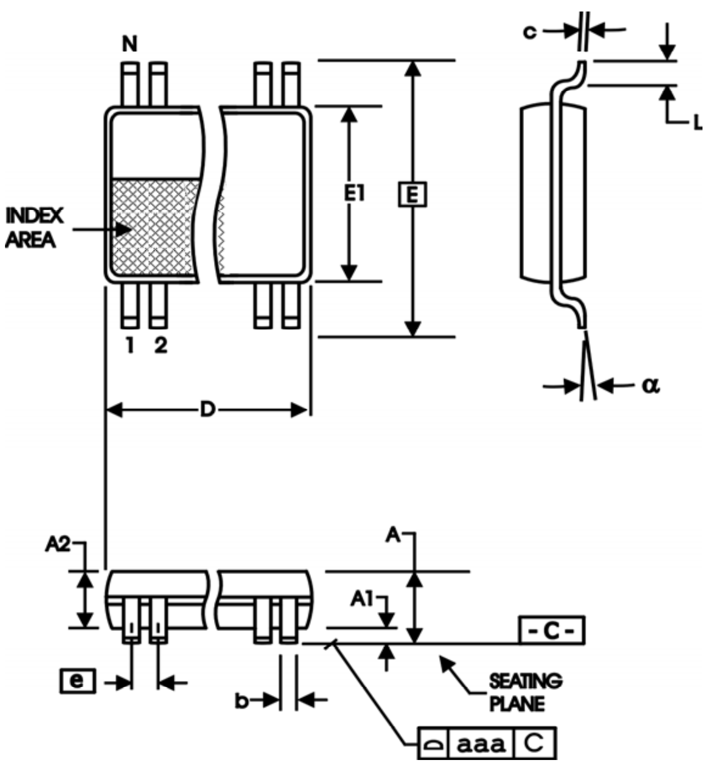



**Table 8. Package Dimensions**

| All Dimensions in Millimeters | | |
|---|---|---|
| **Symbol** | **Minimum** | **Maximum** |
| **N** | 20 | |
| **A** | | 1.20 |
| **A1** | 0.05 | 0.15 |
| **A2** | 0.80 | 1.05 |
| **b** | 0.19 | 0.30 |
| **c** | 0.09 | 0.20 |
| **D** | 6.40 | 6.60 |
| **E** | 6.40 Basic | |
| **E1** | 4.30 | 4.50 |
| **e** | 0.65 Basic | |
| **L** | 0.45 | 0.75 |
| $\alpha$ | 0° | 8° |
| **aaa** | | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

# Ordering Information

### Table 9. Ordering Information

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 8545AGI-02LF | ICS8545AI02L | "Lead-Free" 20 Lead TSSOP | Tube | -40°C to 85°C |
| 8545AGI-02LFT | ICS8545AI02L | "Lead-Free" 20 Lead TSSOP | 2500 Tape & Reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

## Revision History

5/7/15 Product Discontinuation Notice - PDN CQ-15-03.

www.IDT.com

6024 Silver Creek Valley Road
San Jose, California 95138

**Sales**
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

**Technical Support**
clocks@idt.com
+480-763-2056