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LVCMOS/LVTTL FANOUT BUFFER/DIVIDER ICS87004-03

General Description

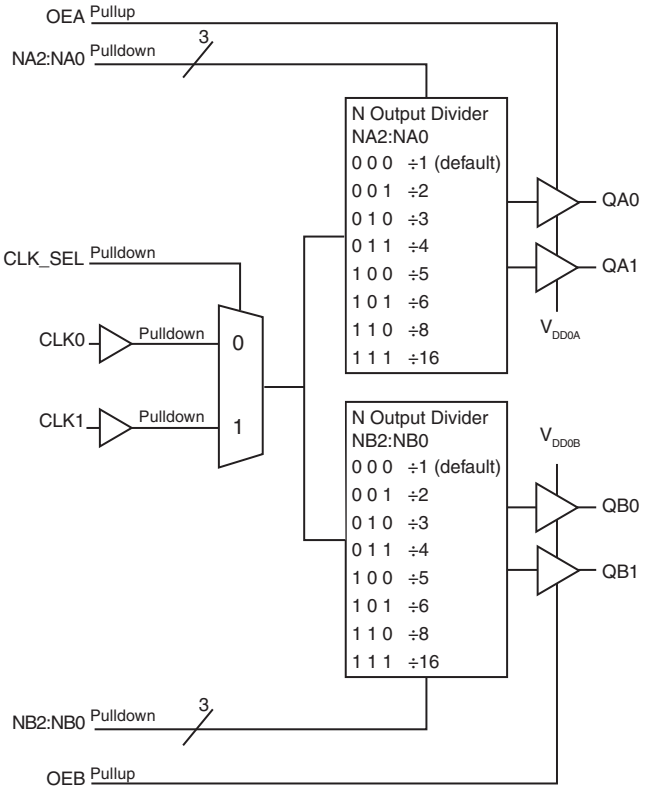
The ICS87004-03 is a low skew, ÷1, ÷2 ÷3, ÷4 ÷5, ÷6 ÷8, ÷16 LVCMOS/LVTTL Fanout Buffer/ Divider and a member of theHiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS87004-03 has selectable clock inputs that accept single ended input levels. Output enable pin controls whether the output is in the active or high impedance state.

The ICS87004-03 is characterized at 3.3V, 2.5V and mixed 3.3V/ 2.5V, 3.3V/1.8V, 2.5V/1.8V input/output supply operating modes. Guaranteed bank, output, and part-to-part skew characteristics make the ICS87004-03 ideal for those applications demanding well defined performance and repeatability.

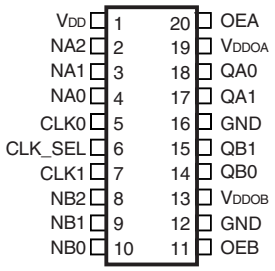
Features

- Two banks of two LVCMOS/LVTTL outputs, 15Ω typical output impedance
- Selectable LVCMOS/LVTTL clock inputs
- LVCMOS_CLK supports the following input types: LVCMOS, LVTTL
- Maximum output frequency: 200MHz
- Output skew: 100ps (typical)
- Bank skew: 50ps (typical)
- Part-to-part skew: TBD
- Power supply modes:
  Core/Output
  3.3V/3.3V
  3.3V/2.5V
  3.3V/1.8V
  2.5V/2.5V
  2.5V/1.8V
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS87004-03
20-Lead TSSOP
6.50mm x 4.40mm x 0.92mm package body
G Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{DD}	Power		Power supply pin.
2, 3, 4	NA2, NA1, NA0	Input	Pulldown	N divider pins for Bank A outputs. LVCMOS / LVTTL interface levels.
5, 7	CLK0, CLK1	Input	Pulldown	LVCMOS / LVTTL clock inputs.
6	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1 input. When LOW, selects CLK0 input. LVCMOS / LVTTL interface levels.
8, 9, 10	NB2, NB1, NB0	Input	Pulldown	N divider pins for Bank B outputs. LVCMOS / LVTTL interface levels.
11	OEB	Input	Pullup	Output enable. When LOW, Bank B outputs are in HIGH impedance state. When HIGH, Bank B outputs are active. LVCMOS / LVTTL interface levels.
12, 16	GND	Power		Power supply ground.
13	V_{DDOB}	Power		Output supply pin for Bank B outputs.
14, 15	QB0, QB1	Output		Bank B clock outputs. LVCMOS / LVTTL interface levels.
17, 18	QA1, QA0	Output		Bank A clock outputs. LVCMOS / LVTTL interface levels.
19	V_{DDOA}	Power		Bank A output supply pin.
20	OEA	Input	Pullup	Output enable. When LOW, Bank A outputs are in HIGH impedance state. When HIGH, Bank A outputs are active. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)			TBD		pF
R_{OUT}	Output Impedance			15		Ω

TABLE 3. PROGRAMMABLE OUTPUT DIVIDER FUNCTION TABLE

Inputs				Output Frequency (MHz)	
N2	N1	N0	N Divider Value	Minimum	Maximum
0	0	0	÷1 (default)		
0	0	1	÷2		
0	1	0	÷3		
0	1	1	÷4		
1	0	0	÷5		
1	0	1	÷6		
1	1	0	÷8		
1	1	1	÷16		

NOTE: Some combinations of Bank A and Bank B output divider selections are not synchronous.

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	93.1°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V±5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDOA}, V_{DDOB}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			40		mA
I_{DDOA}, I_{DDOB}	Output Supply Current			1		mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = 3.3V±5\%$, $V_{DDOA} = V_{DDOB} = 2.5V±5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDOA}, V_{DDOB}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			40		mA
I_{DDOA}, I_{DDOB}	Output Supply Current			1		mA

Table 4C. Power Supply DC Characteristics, $V_{DD} = 3.3V±5\%$, $V_{DDOA} = V_{DDOB} = 1.8V±0.15V$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDOA}, V_{DDOB}	Output Supply Voltage		1.65	1.8	1.95	V
I_{DD}	Power Supply Current			40		mA
I_{DDOA}, I_{DDOB}	Output Supply Current			1		mA

Table 4D. Power Supply DC Characteristics, $V_{DD} = V_{DDOA} = V_{DDOB} = 2.5V±5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
V_{DDOA}, V_{DDOB}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			39		mA
I_{DDOA}, I_{DDOB}	Output Supply Current			1		mA

Table 4E. Power Supply DC Characteristics, $V_{DD} = 2.5V±5\%$, $V_{DDOA} = V_{DDOB} = 1.8V±0.15V$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
V_{DDOA}, V_{DDOB}	Output Supply Voltage		1.65	1.8	1.95	V
I_{DD}	Power Supply Current			39		mA
I_{DDOA}, I_{DDOB}	Output Supply Current			1		mA

TABLE 4F. LVCMOS/LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V±5% OR 2.5V±5%V_{DDOA} = V_{DDOB} = 3.3V±5%, 2.5V±5% OR 1.8V±0.15V, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	CLK0, CLK1, CLK_SEL, NA2:NA0, NB2:NB0	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
		OEA, OEB	V_{DD} = V_{IN} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	CLK0, CLK1, CLK_SEL, NA2:NA0, NB2:NB0	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
		OEA, OEB	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		V_{DDOX} = 3.3V ± 5%	2.6			V
			V_{DDOX} = 2.5V ± 5%	1.8			V
			V_{DDOX} = 1.8V ± 0.15V	1.5			V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDOX} = 3.3V ± 5%			0.5	V
			V_{DDOX} = 2.5V ± 5%			0.5	V
			V_{DDOX} = 1.8V ± 0.15V			0.4	V
I_{OZL}	Output Hi-Z Current Low			-5			µA
I_{OZH}	Output Hi-Z Current High					5	µA

NOTE 1: Outputs terminated with 50Ω to V_{DDOX}/2. See Parameter Measurement Information, Output Load Test Circuit.

TABLE 5A. AC CHARACTERISTICS, V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				200	MHz
t_{PD}	Propagation Delay, NOTE 1			4.5		ns
*t*sk(o)	Output Skew; NOTE 2, 3			100		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			TBD		ps
*t*sk(b)	Bank Skew; NOTE 3, 5			50		ps
t_R / t_F	Output Rise/Fall Time; NOTE 6	20% to 80%		800		ps
odc	Output Duty Cycle			50		%
t_{EN}	Output Enable Time; NOTE 6				5	ns
t_{DIS}	Output Disable Time; NOTE 6				5	ns

All parameters measured at $f \leq$ TBDMHz unless noted otherwise.
NOTE 1: Measured from V_{DD}/2 of the input to V_{DDOX}/2 of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDOX}/2.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDOX}/2.
NOTE: 5 Defined as skew within a bank with equal load conditions.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

TABLE 5B. AC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, V_{DDOA} = V_{DDOB} = 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				200	MHz
t_{PD}	Propagation Delay, NOTE 1			4.5		ns
*t*sk(o)	Output Skew; NOTE 2, 3			100		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			TBD		ps
*t*sk(b)	Bank Skew; NOTE 3, 5			50		ps
t_R / t_F	Output Rise/Fall Time; NOTE 6	20% to 80%		850		ps
odc	Output Duty Cycle			50		%
t_{EN}	Output Enable Time; NOTE 6				5	ns
t_{DIS}	Output Disable Time; NOTE 6				5	ns

All parameters measured at $f \leq$ TBDMHz unless noted otherwise.
NOTE 1: Measured from V_{DD}/2 of the input to V_{DDOX}/2 of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDOX}/2.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDOX}/2.
NOTE: 5 Defined as skew within a bank with equal load conditions.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

TABLE 5C. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDOA} = V_{DDOB} = 1.8V±0.15V, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				200	MHz
t_{PD}	Propagation Delay, NOTE 1			4.5		ns
*t*sk(o)	Output Skew; NOTE 2, 3			100		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			TBD		ps
*t*sk(b)	Bank Skew; NOTE 3, 5			50		ps
t_R / t_F	Output Rise/Fall Time; NOTE 6	20% to 80%		900		ps
odc	Output Duty Cycle			50		%
t_{EN}	Output Enable Time; NOTE 6				5	ns
t_{DIS}	Output Disable Time; NOTE 6				5	ns

All parameters measured at $f \leq$ TBDMHz unless noted otherwise.
NOTE 1: Measured from V_{DD}/2 of the input to V_{DDOX}/2 of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDOX}/2.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDOX}/2.
NOTE: 5 Defined as skew within a bank with equal load conditions.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

TABLE 5D. AC CHARACTERISTICS, $V_{DD} = V_{DDOA} = V_{DDOB} = 2.5V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				200	MHz
t_{PD}	Propagation Delay, NOTE 1			4.5		ns
*t*sk(o)	Output Skew; NOTE 2, 3			100		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			TBD		ps
*t*sk(b)	Bank Skew; NOTE 3, 5			50		ps
t_R / t_F	Output Rise/Fall Time; NOTE 6	20% to 80%		950		ps
odc	Output Duty Cycle			50		%
t_{EN}	Output Enable Time; NOTE 6				5	ns
t_{DIS}	Output Disable Time; NOTE 6				5	ns

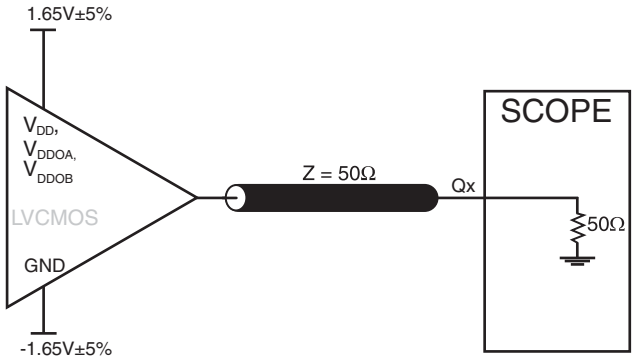
All parameters measured at $f \leq$ TBDMHz unless noted otherwise.
NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDOX}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOX}/2$.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDOX}/2$.
NOTE: 5 Defined as skew within a bank with equal load conditions.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

TABLE 5E. AC CHARACTERISTICS, $V_{DD} = 2.5V \pm 5\%$, $V_{DDOA} = V_{DDOB} = 1.8V \pm 0.15V$, $T_A = 0°C$ TO $70°C$

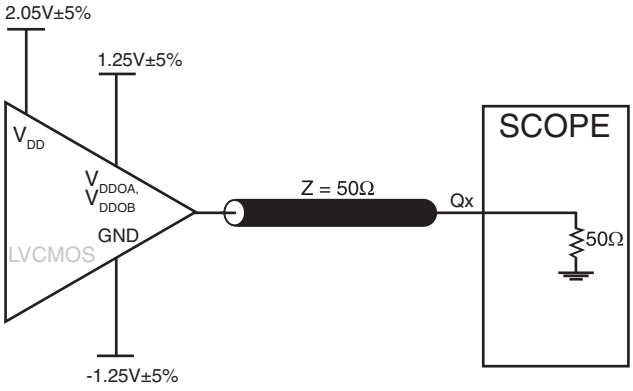
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				200	MHz
t_{PD}	Propagation Delay, NOTE 1			4.5		ns
*t*sk(o)	Output Skew; NOTE 2, 3			100		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			TBD		ps
*t*sk(b)	Bank Skew; NOTE 3, 5			50		ps
t_R / t_F	Output Rise/Fall Time; NOTE 6	20% to 80%		1000		ps
odc	Output Duty Cycle			50		%
t_{EN}	Output Enable Time; NOTE 6				5	ns
t_{DIS}	Output Disable Time; NOTE 6				5	ns

All parameters measured at $f \leq$ TBDMHz unless noted otherwise.
NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDOX}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOX}/2$.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDOX}/2$.
NOTE: 5 Defined as skew within a bank with equal load conditions.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

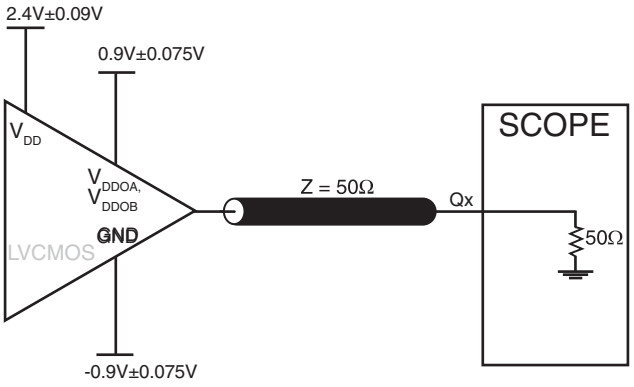
PARAMETER MEASUREMENT INFORMATION



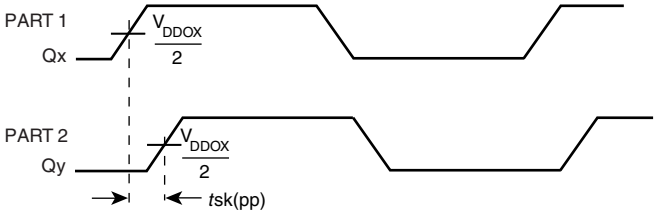
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



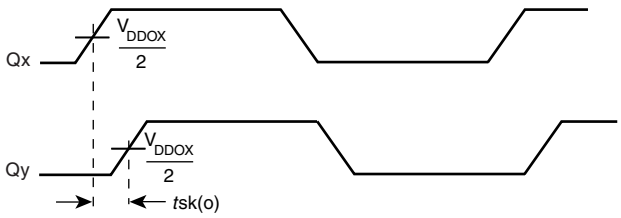
3.3V CORE/ 2.5V OUTPUT LOAD AC TEST CIRCUIT



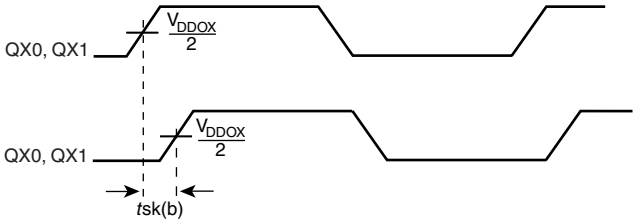
3.3V CORE/ 1.8V OUTPUT LOAD AC TEST CIRCUIT



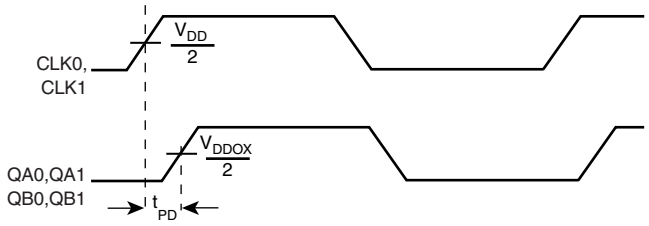
PART-TO-PART SKEW



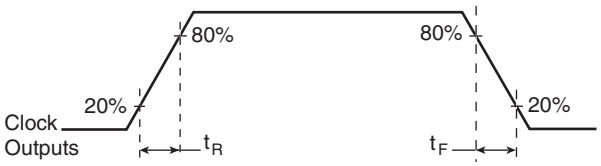
OUTPUT SKEW



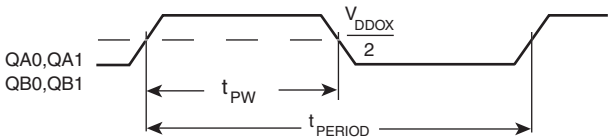
BANK SKEW



PROPAGATION DELAY



OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CLK INPUT:
For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

LVCMOS CONTROL PINS:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUT:
All unused LVCMOS output can be left floating. There should be no trace attached.

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 20 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	93.1°C/W	88.7°C/W	86.6°C/W

TRANSISTOR COUNT

The transistor count for ICS87004-03 is: 2781

Package Outline - G Suffix for 20 Lead TSSOP

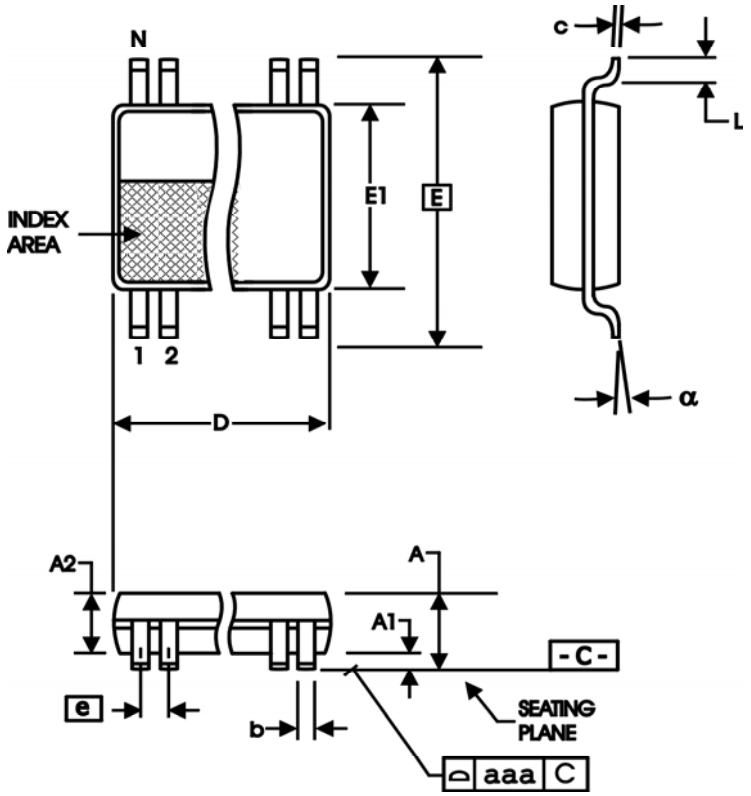


Table 7. Package Dimensions

SYMBOL	Millimeters	
	MIN	MAX
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS87004BG-03	ICS87004BG03	20 Lead TSSOP	tube	0°C to 70°C
ICS87004BG-03T	ICS87004BG03	20 Lead TSSOP	2500 tape & reel	0°C to 70°C
ICS87004BG-03LF	ICS87004B03L	20 Lead "Lead-Free" TSSOP	tube	0°C to 70°C
ICS87004BG-03LFT	ICS87004B03L	20 Lead "Lead-Free" TSSOP	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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