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General Description

The ICS871004I-04 is a high performance Jitter Attenuator designed for use in PCI Express™ systems. In some PCI Express systems, such as those found in desktop PCs, the PCI Express clocks are generated from a low bandwidth, high phase noise PLL frequency synthesizer. In these systems, a jitter attenuator may be required to attenuate high frequency random and deterministic jitter components from the PLL synthesizer and from the system board. The ICS871004I-04 has three PLL bandwidth modes: 200kHz, 700kHz and 1700kHz. The 200kHz mode provides the maximum jitter attenuation, but it also results in higher PLL tracking time. In this mode, the spread spectrum modulation may also be attenuated. The 700kHz bandwidth provides an intermediate bandwidth that can easily track tri-angular spread profiles, while providing good jitter attenuation. The 1700kHz bandwidth provides the best tracking skew and will pass most spread profiles, but the jitter attenuation will not be as good as the lower bandwidth modes. The ICS871004I-04 can be set for different modes using the F_SELx pins as shown in Table 3C.

The ICS871004I-04 uses IDT's 3RD Generation FemtoClock® PLL technology to achieve the lowest possible phase noise. The device is packaged in a 24 Lead TSSOP package, making it ideal for use in space constrained applications such as PCI Express add-in cards.

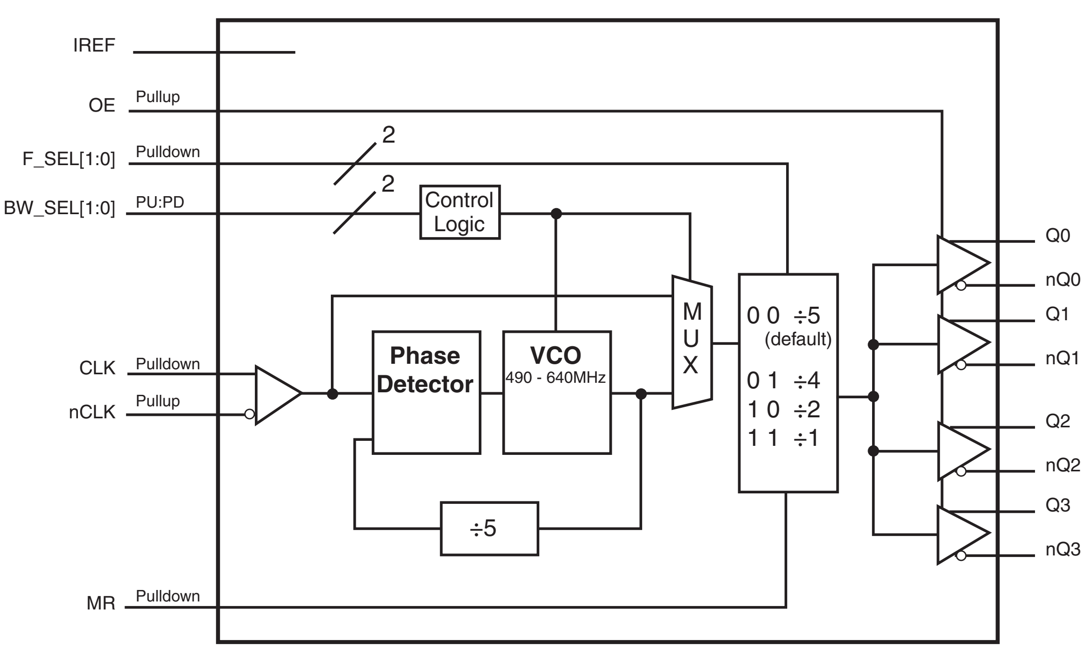
Features

- Four differential HCSL output pairs
- One differential clock input
- CLK, nCLK can accept the following differential input levels: LVPECL, LVDS, HSTL, HCSL
- Output frequency range: 98MHz to 640MHz
- Input frequency range: 98MHz to 128MHz
- VCO range: 490MHz - 640MHz
- Cycle-to-cycle jitter: 7.5ps (typical)
- Three bandwidth modes allow the system designer to make jitter attenuation/tracking skew design trade-offs
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

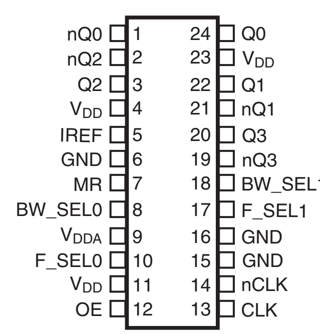
PLL Bandwidth (typical) Table

BW_SEL[1:0]
00 = PLL Bandwidth: ~200kHz
01 = PLL Bandwidth: ~700kHz (default)
10 = PLL Bandwidth: ~1700kHz
11 = PLL BYPASS

Block Diagram



Pin Assignment



ICS871004I-04
24-Lead TSSOP
4.4mm x 7.8mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 24	nQ0, Q0	Output		Differential output pair. HCSL interface levels.
2, 3	nQ2, Q2	Output		Differential output pair. HCSL interface levels.
4, 11, 23	V_{DD}	Power		Core supply pins.
5	IREF	Input		An external fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode Qx, nQx clock outputs.
6, 15, 16	GND	Power		Power supply ground.
7	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs (Qx) to go low and the inverted outputs (nQx) to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
8	BW_SEL0	Input	Pullup	Selects the PLL Bandwidth input.
9	V_{DDA}	Power		Analog supply pin.
10, 17	F_SEL0, F_SEL1	Input	Pulldown	Frequency select pins.LVCMOS/LVTTL interface levels
12	OE	Input	Pullup	Output enable pin. When HIGH, the outputs are active. When LOW, the outputs are in a high impedance state. LVCMOS/LVTTL interface levels. See Table 3A.
13	CLK	Input	Pulldown	Non-inverting differential clock input.
14	nCLK	Input	Pullup	Inverting differential clock input.
18	BW_SEL1	Input	Pulldown	Selects the PLL Bandwidth input.
19, 20	nQ3, Q3	Output		Differential output pair. HCSL interface levels.
21, 22	nQ1, Q1	Output		Differential output pair. HCSL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Output Enable Function Table

Input	Outputs	
OE	**Q[0:3]**	**nQ[0:3]**
0	High-Impedance	High-Impedance
1 (default)	Enabled	Enabled

Table 3B. PLL Bandwidth Control Table

Input		
BW_SEL1	**BW_SEL0**	**PLL Bandwidth**
0	0	~200kHz
0	1	~700kHz (default)
1	0	~1700kHz
1	1	PLL BYPASS

Table 3C. F_SELx Function Table

	Inputs			
Input Frequency (MHz)	**F_SEL1**	**F_SEL0**	**Divider Value**	**Output Frequency (MHz)**
100	0	0	÷5	100 (default)
100	0	1	÷4	125
100	1	0	÷2	250
100	1	1	÷1	500

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	82.3°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. LVDS Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.10	3.3	V_{DD}	V
I_{DD}	Power Supply Current			40	55	mA
I_{DDA}	Analog Supply Current			6.4	10	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	MR, OE, F_SEL[1:0]		2		V_{DD} + 0.3	V
		BW_SEL[1:0]		V_{DD} – 0.3		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	MR, OE, F_SEL[1:0]		-0.3		0.8	V
		BW_SEL[1:0]		-0.3		0.3	V
I_{IH}	Input High Current	BW_SEL0 OE, F_SEL1	V_{DD} = V_{IN} = 3.465V			5	µA
		F_SEL[1:0], MR, BW_SEL1	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	BW_SEL0 OE, F_SEL1	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		F_SEL[1:0], MR, BW_SEL1	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA

Table 4C. Differential DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		nCLK,	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

Table 5A. PCI Express Jitter Specifications, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	PCIe Industry Specification	Units
t_j (PCIe Gen 1)	Phase Jitter Peak-to-Peak; NOTE 1, 4	*ƒ* = 100MHz, Evaluation Band: 0Hz - Nyquist (clock frequency/2)		32.4	50.1	86	ps
$t_{REFCLK\_HF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 2, 4	*ƒ* = 100MHz, High Band: 1.5MHz - Nyquist (clock frequency/2)		1.29	2.33	3.1	ps
$t_{REFCLK\_LF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 2, 4	*ƒ* = 100MHz, Low Band: 10kHz - 1.5MHz		1.37	2.14	3.0	ps
t_{REFCLK_RMS} (PCIe Gen 3)	Phase Jitter RMS; NOTE 3, 4	*ƒ* = 100MHz, Evaluation Band: 0Hz - Nyquist (clock frequency/2)		0.419	0.619	0.8	ps

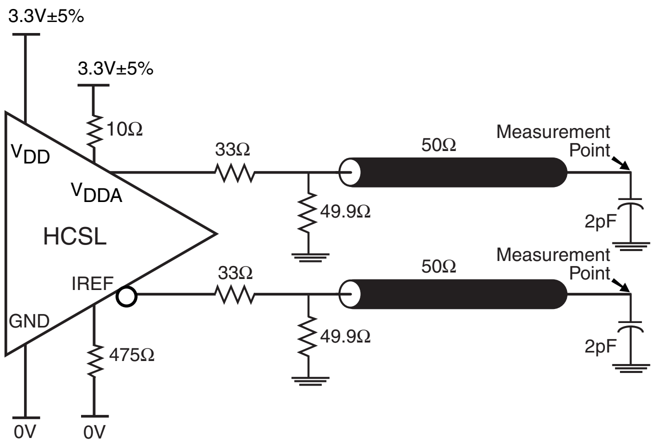
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions. For additional information, refer to the *PCI Express Application Note section* in the datasheet.
NOTE: PCIe jitter parameters were obtained with Spread Spectrum Modulation disabled.
NOTE 1: Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of 10^6 clock periods.
NOTE 2: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{REFCLK\_HF\_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK\_LF\_RMS}$ (Low Band).
NOTE 3: RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the *PCI Express Base Specification Revision 0.7, October 2009* and is subject to change pending the final release version of the specification.
NOTE 4: This parameter is guaranteed by characterization. Not tested in production.

Table 5B. AC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		98		640	MHz
*t*jit(per)	RMS Period Jitter; NOTE 1			6	18	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1			7.5	17	ps
V_{MAX}	Absolute Max. Output Voltage; NOTE 2, 3				1150	mV
V_{MIN}	Absolute Min. Output Voltage; NOTE 2, 4		-300			mV
V_{RB}	Ringback Voltage; NOTE 5, 6		-100		100	mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 2, 7, 8		250		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges; NOTE 2, 7, 9				140	mV
t_R / t_F	Output Rise/Fall Time	Single-ended measurements from 20% – 80%	230		560	ps
t_{SLEW+} / t_{SLEW-}	Rising/Falling Edge Rate; NOTE 5, 10	Measured between -150mV to +150mV differential measurement			125	ps
t_L	PLL Lock Time				10	ms
odc	Output Duty Cycle		48		52	%

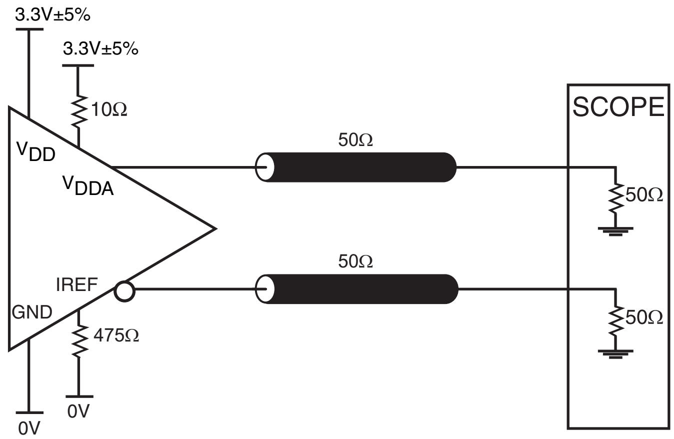
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at f ≤ 250MHz unless noted otherwise.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: Measurement taken from single ended waveform.
NOTE 3: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.
NOTE 4: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.
NOTE 5: Measurement taken from differential waveform.
NOTE 6:T_{STABLE} is the time the differential clock must maintain a minimum ± 150mV differential voltage after rising/falling edges before it is allowed to drop back into the V_{RB} ±100mV differential range.
NOTE 7: Measured at crossing point where the instantaneous voltage value of the rising edge of Q equals the falling edge of nQ.
NOTE 8: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
NOTE 9: Defined as the total variation of all crossing voltages of rising Q and falling nQ, This is the maximum allowed variance in Vcross for any particular system.
NOTE 10: Measured from -150mV to +150mV on the differential waveform (derived from Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing. See Parameter Measurement Information Section.

Parameter Measurement Information



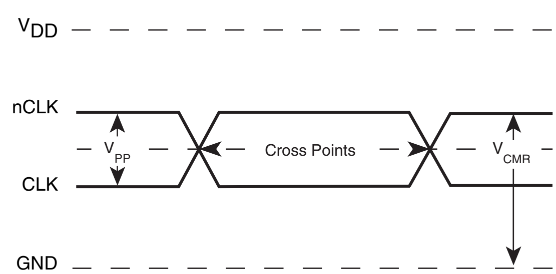
This load condition is used for V_{MAX}, V_{MIN}, V_{RB}, t_{STABLE}, V_{CROSS}, ΔV_{CROSS} and $t_{SLEW\pm}$ measurements.

3.3V HCSL Output Load AC Test Circuit

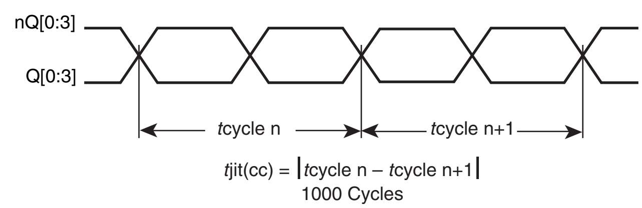


This load condition is used for I_{DD}, tjit(cc), tjit(per)) and odc measurements.

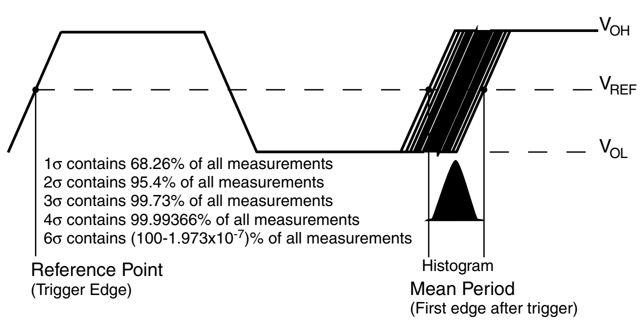
3.3V HCSL Output Load AC Test Circuit



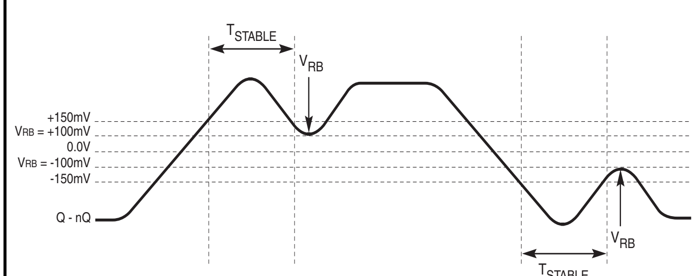
Differential Input Level



Cycle-to-Cycle Jitter

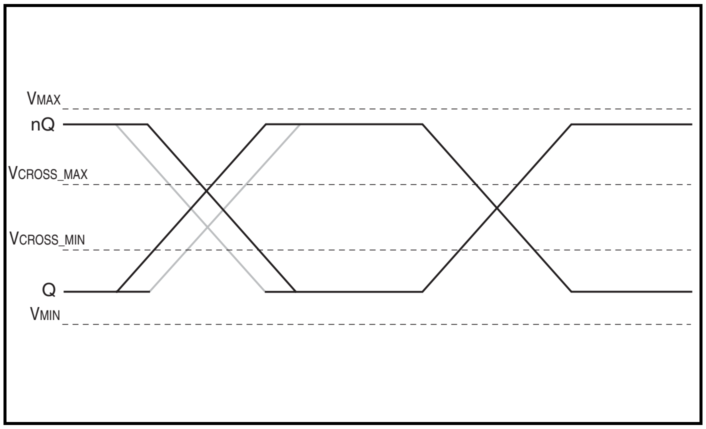


RMS Period Jitter

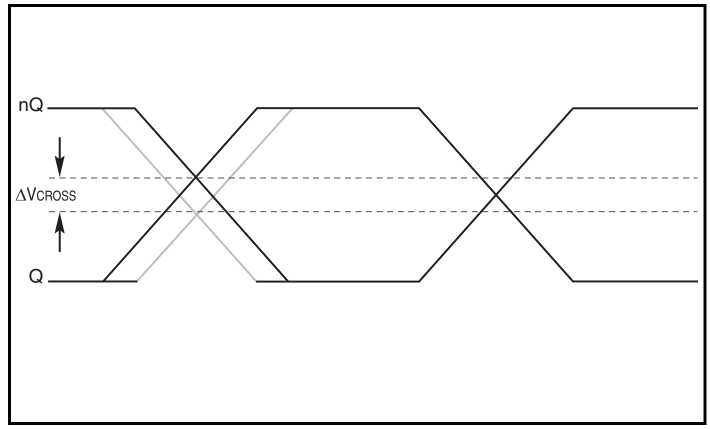


Differential Measurement Points for Ringback

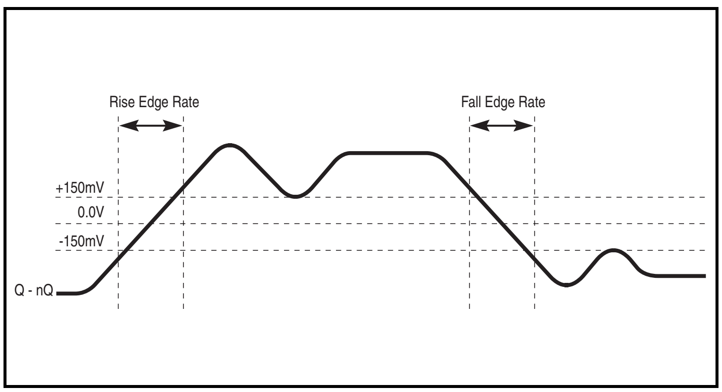
Parameter Measurement Information, continued



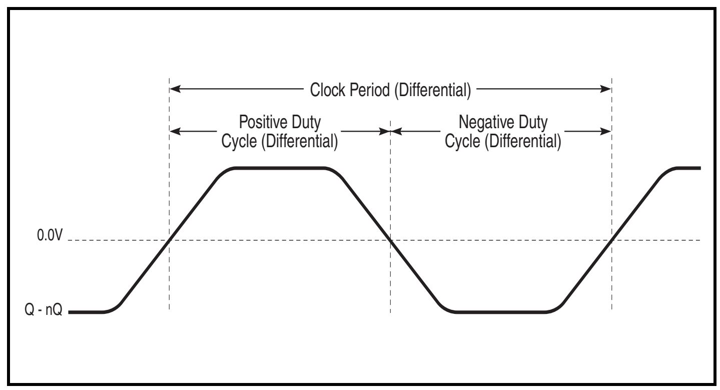
Single-ended Measurement Points for Absolute Cross Point and Swing



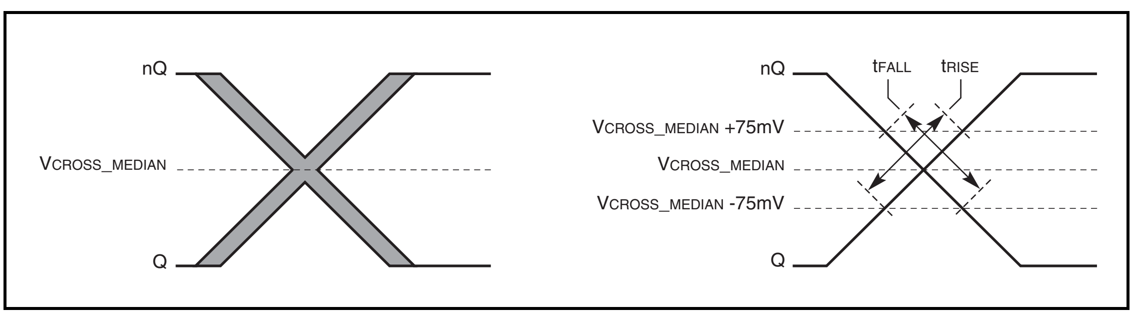
Single-ended Measurement Points for Delta Cross Point



Output Rise/Fall Time



Differential Measurement Points for Duty Cycle/Period



Rise/Fall Time Edge Rate

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

Differential Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

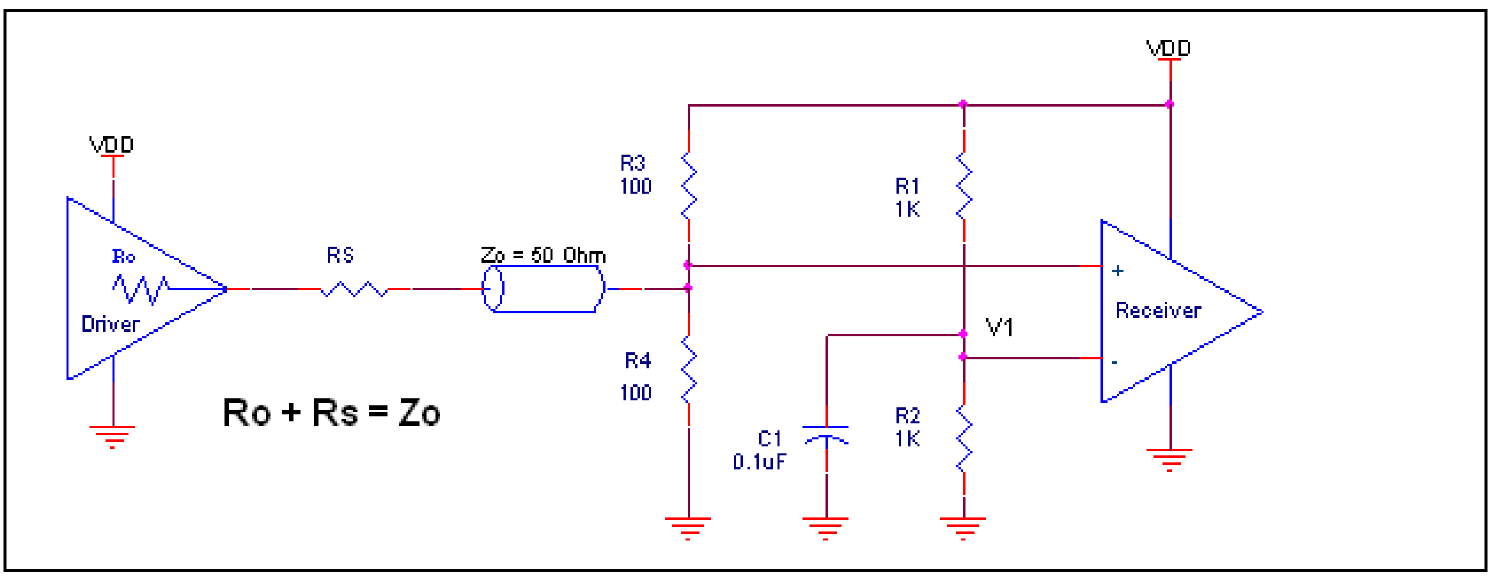
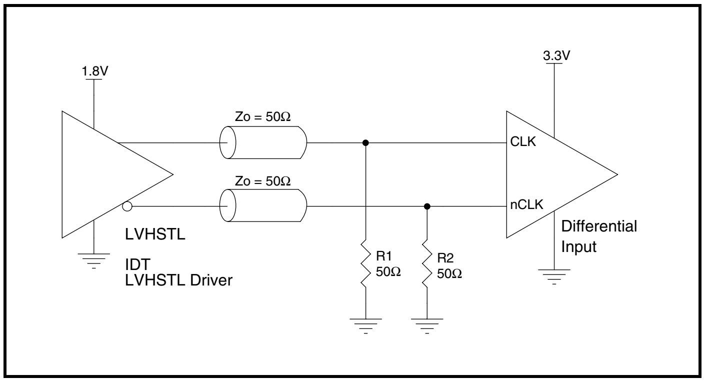


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. The differential signal must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT open emitter HSTL drivers. If you are using an HSTL driver from another vendor, use their termination recommendation.



2A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

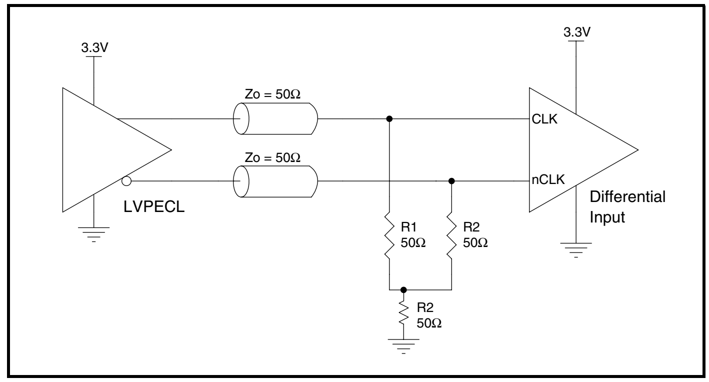


Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

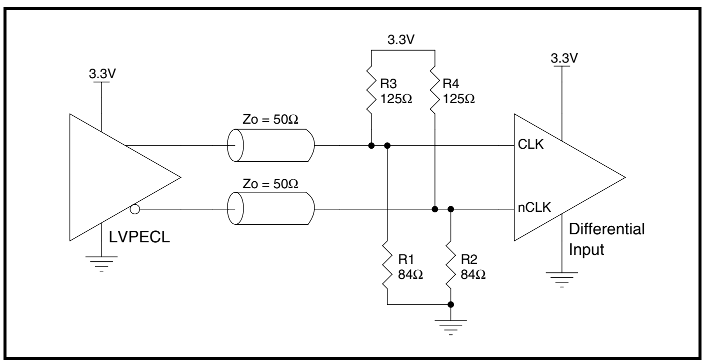


Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

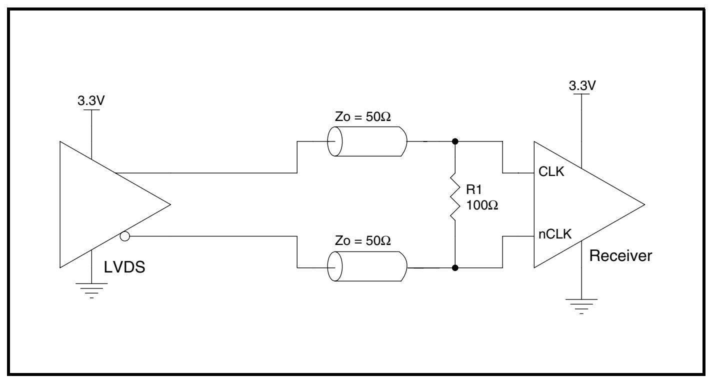


Figure 2D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

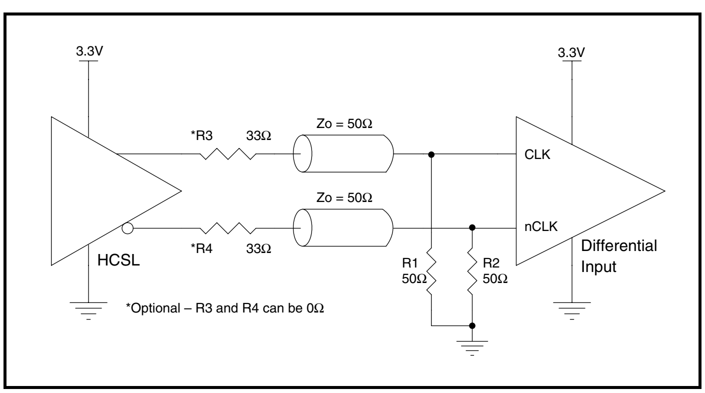


Figure 2E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

Recommended Termination

Figure 3A is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output types.

All traces should be 50Ω impedance single-ended or 100Ω differential.

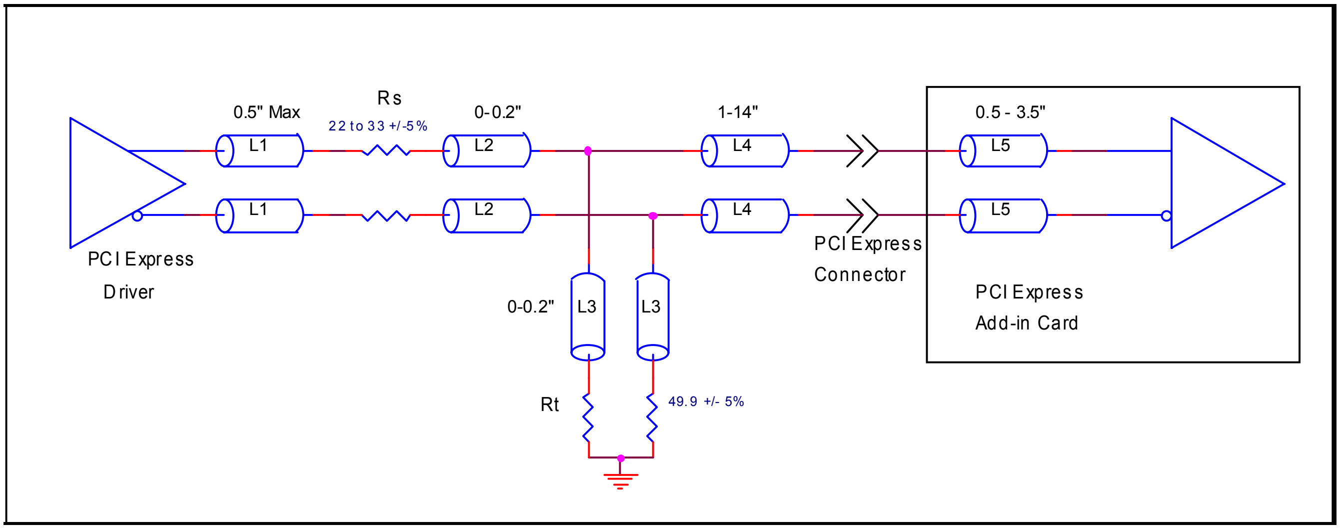


Figure 3A. Recommended Source Termination (where the driver and receiver will be on separate PCBs)

Figure 3B is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

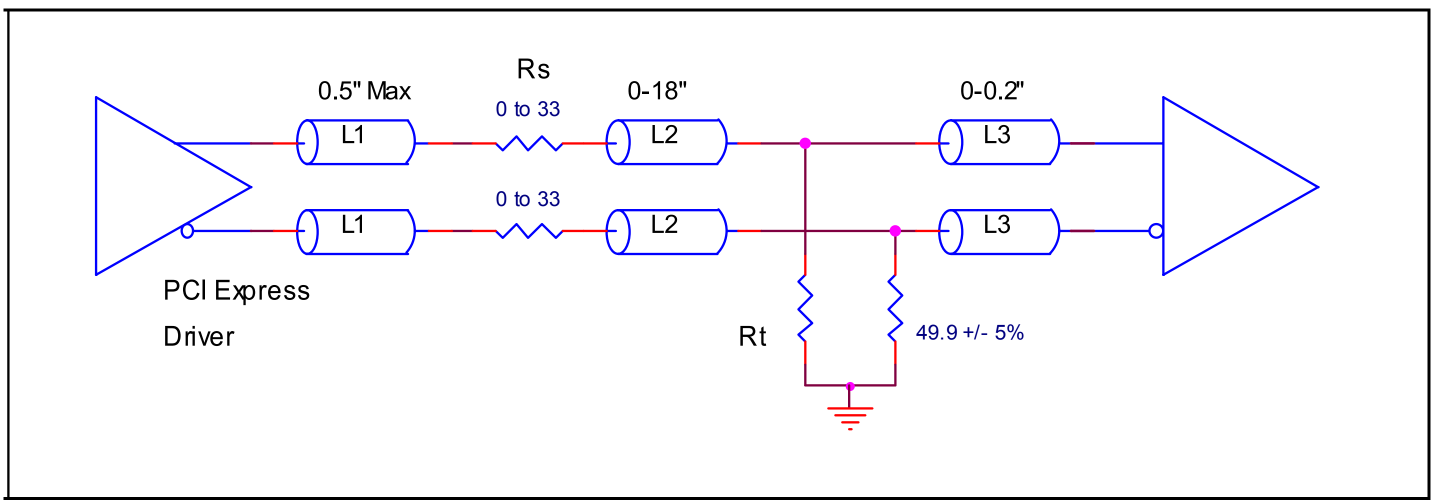


Figure 3B. Recommended Termination (where a point-to-point connection can be used)

PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

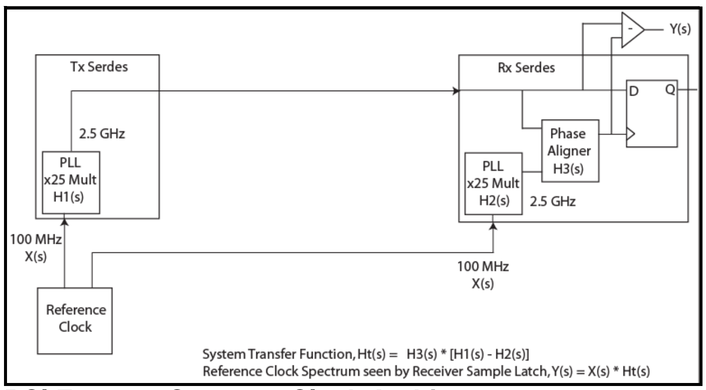
In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

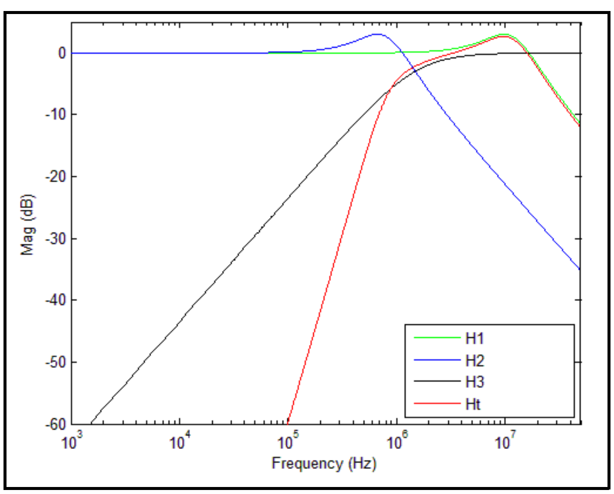
$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].



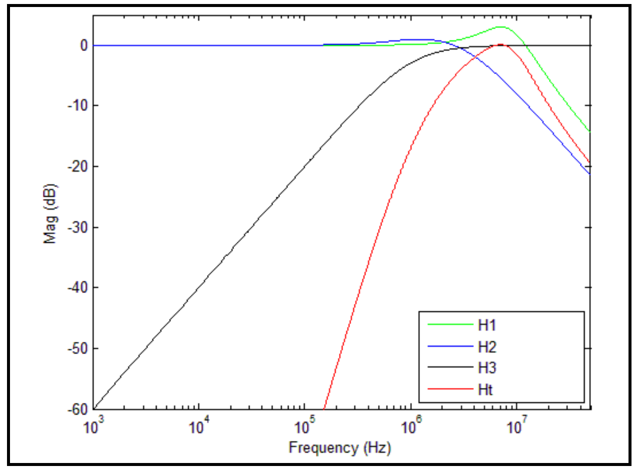
PCI Express Common Clock Architecture

For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

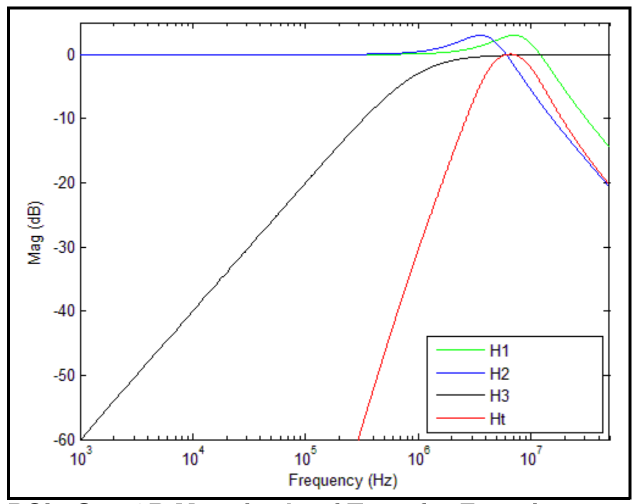


PCIe Gen 1 Magnitude of Transfer Function

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in RMS. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.

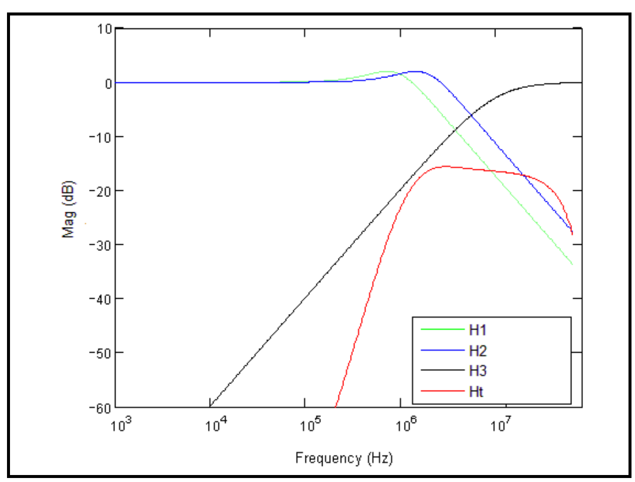


PCIe Gen 2A Magnitude of Transfer Function



PCIe Gen 2B Magnitude of Transfer Function

For **PCI Express Gen 3**, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.



PCIe Gen 3 Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements.*

Schematic Layout

Figure 4 (next page) shows an example of ICS871004I-04 application schematic. The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set. Input and output terminations shown are also intended as examples only and may not represent the exact user configuration

In this example, the input is driven by LVDS but HCSL, 3.3V LVPECL or 2.5V LVPECL inputs will work as well. All the control pins can be defined with an FPGA, rather than pull up and pull down resistors as shown.

As with any high speed analog circuitry, the power supply pins are vulnerable to noise. To achieve optimum jitter performance, power supply isolation is required. The ICS871004I-04 provides separate power supplies to isolate from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitances in the local area of all devices.

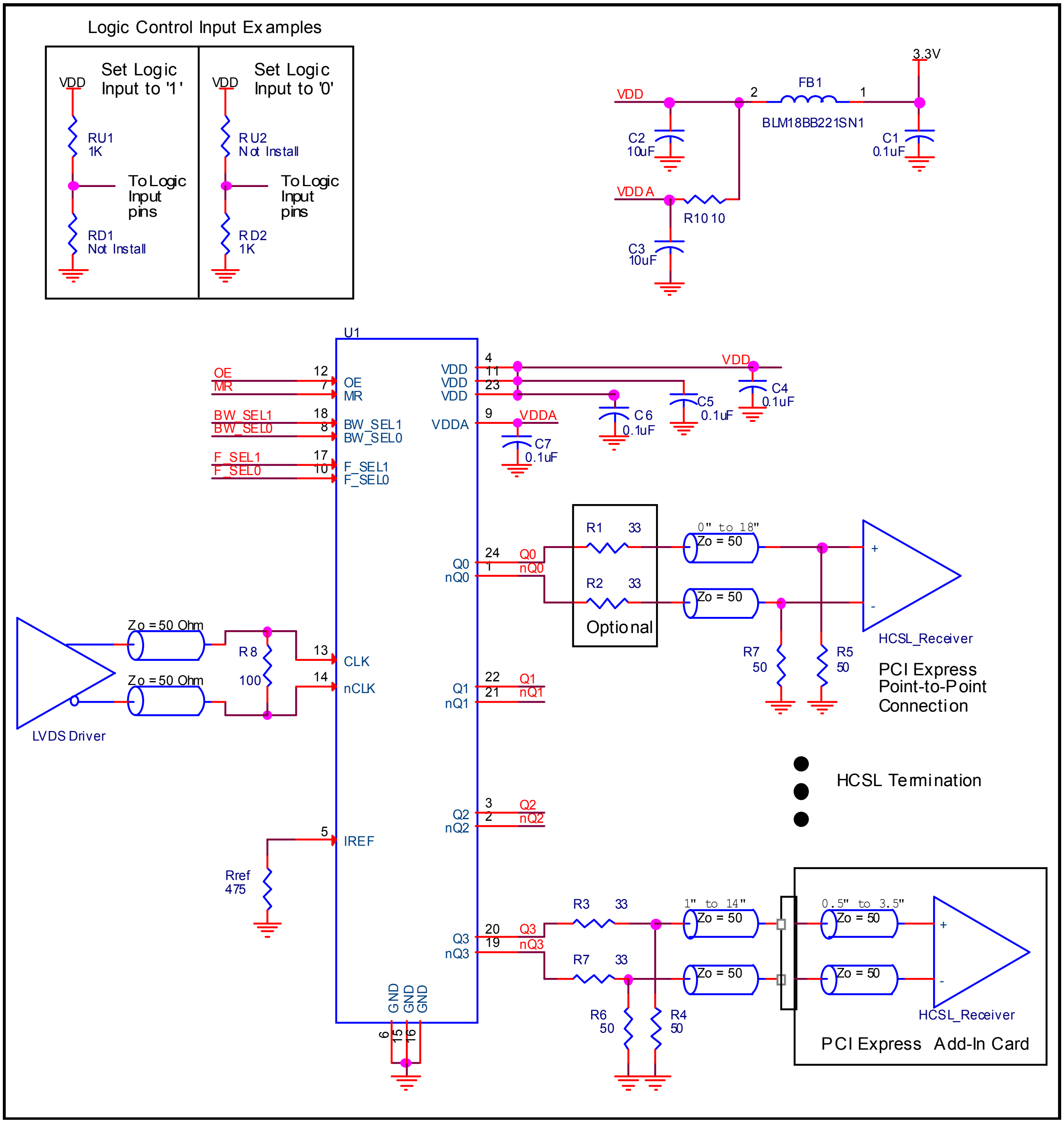


Figure 4. ICS871004I-04 Schematic Layout

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS871004I-04.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS71004I-04 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX})$ = 3.465V * (55mA + 10mA) = **225.225mW**
- Power $(outputs)_{MAX}$ = **44.5mW/Loaded Output Pair**
  If all outputs are loaded, the total power is 4 * 44.5mW = **178mW**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 225.225mW + 178mW = **403.225mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 82.3°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.403W * 82.3°C/W = 118.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 24 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	82.3°C/W	78.0°C/W	75.9°C/W

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 6.*

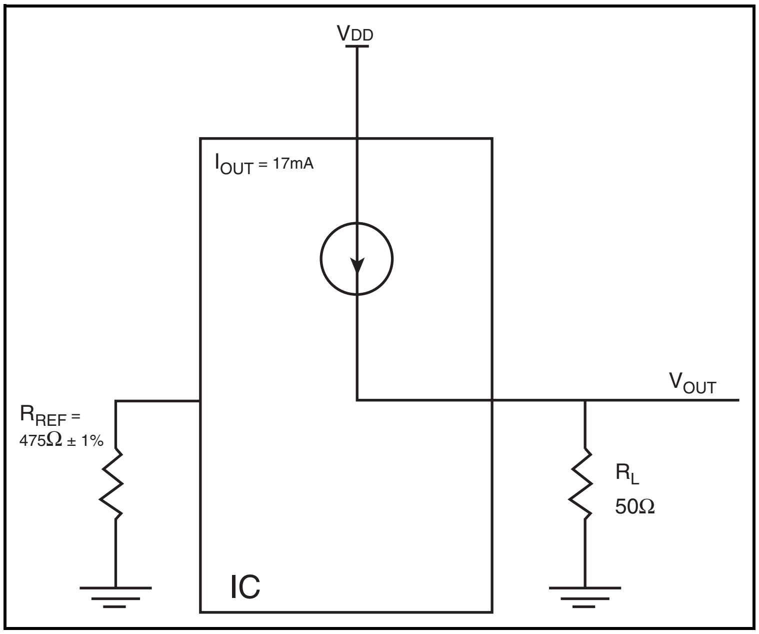


Figure 6. HCSL Driver Circuit and Termination

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when V_{DD-MAX}.

Power $= (V_{DD\_MAX} – V_{OUT}) * I_{OUT}$,

since $V_{OUT} – I_{OUT} * R_L$

$= (V_{DD\_MAX} – I_{OUT} * R_L) * I_{OUT}$

$= (3.465V – 17mA * 50\Omega) * 17mA$

Total Power Dissipation per output pair = **44.5mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 24 Lead TSSOP

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	82.3°C/W	78.0°C/W	75.9°C/W

Transistor Count

The transistor count for ICS871004I-04 is: 1,395

Package Outline and Package Dimensions

Package Outline - G Suffix for 20 Lead TSSOP

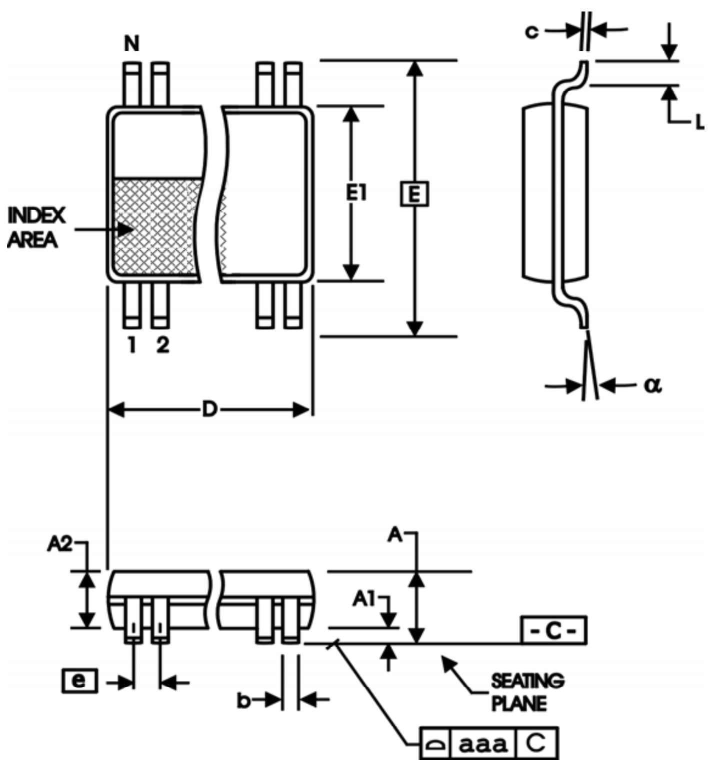


Table 8 Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	20	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
871004AGI-04LF	ICS71004AI04L	“Lead-Free” 24 Lead TSSOP	Tube	-40°C to 85°C
871004AGI-04LFT	ICS71004AI04LL	“Lead-Free” 24 Lead TSSOP	Tape & Reel	-40°C to 85°C

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