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FEMTOCLOCKS™ LVDS/LVPECL ZERO DELAY BUFFER/ CLOCK GENERATOR FOR PCI EXPRESS™ AND ETHERNET

ICS8743004I

General Description

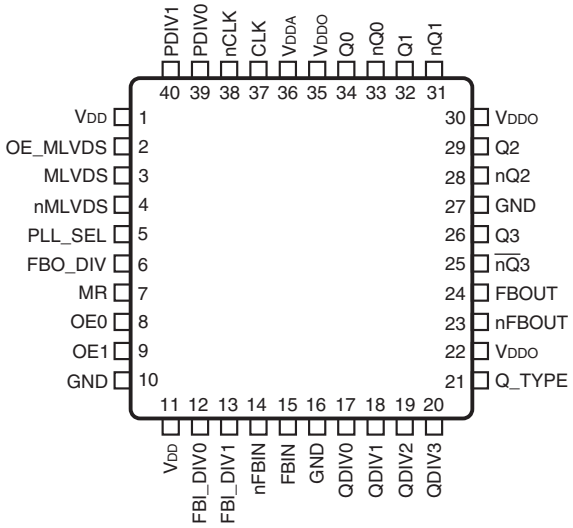
The ICS8743004I is Zero-Delay Buffer/Frequency Multiplier with four differential LVDS or LVPECL output pairs (pin selectable output type), and uses external feedback for “zero delay” clock regeneration. In PCI Express and Ethernet applications, 100MHz and 125MHz are the most commonly used reference clock frequencies and each of the four output pairs can be independently set for either 100MHz or 125MHz. With an output frequency range of 98MHz to 165MHz, the device is also suitable for use in a variety of other applications such as Fibre Channel (106.25MHz) and XAUI (156.25MHz). The M-LVDS Input/Output pair is useful in backplane applications when the reference clock can either be local (on the same board as the ICS8743004I) or remote via a backplane connector. In output mode, an input from a local reference clock applied to the CLK/nCLK input pins is translated to M-LVDS and driven out to the MLVDS/nMLVDS pins. In input mode, the internal M_LVDS driver is placed in Hi-Z state using the OE_MLVDS pin and MLVDS/nMLVDS pin then becomes an input (e.g. from a backplane).

The ICS8743004I uses very low phase noise FemtoClock™ technology, thus making it ideal for such applications as PCI Express Generation 1 and 2 as well as for Gigabit Ethernet, Fibre Channel, and 10 Gigabit Ethernet. It is packaged in a 40-VFQFN package (6mm x 6mm).

Features

- Four differential output pairs with selectable pin type: LVDS or LVPECL. Each output pair is individually selectable for 100MHz or 125MHz (for PCIe and Ethernet applications).
- One differential clock input pair CLK/nCLK can accept the following differential input levels: LVPECL, LVDS, M-LVDS, LVHSTL, HCSL
- One M-LVDS I/O (MLVDS/nMLVDS)
- Output frequency range: 98MHz - 165MHz
- Input frequency range: 19.6MHz - 165MHz
- VCO range: 490MHz - 660MHz
- PCI Express (2.5 Gb/S) and Gen 2 (5 Gb/s) jitter compliant
- External feedback for “zero delay” clock regeneration
- RMS phase jitter @ 125MHz (1.875MHz – 20MHz): 0.57ps (typical)
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) packages

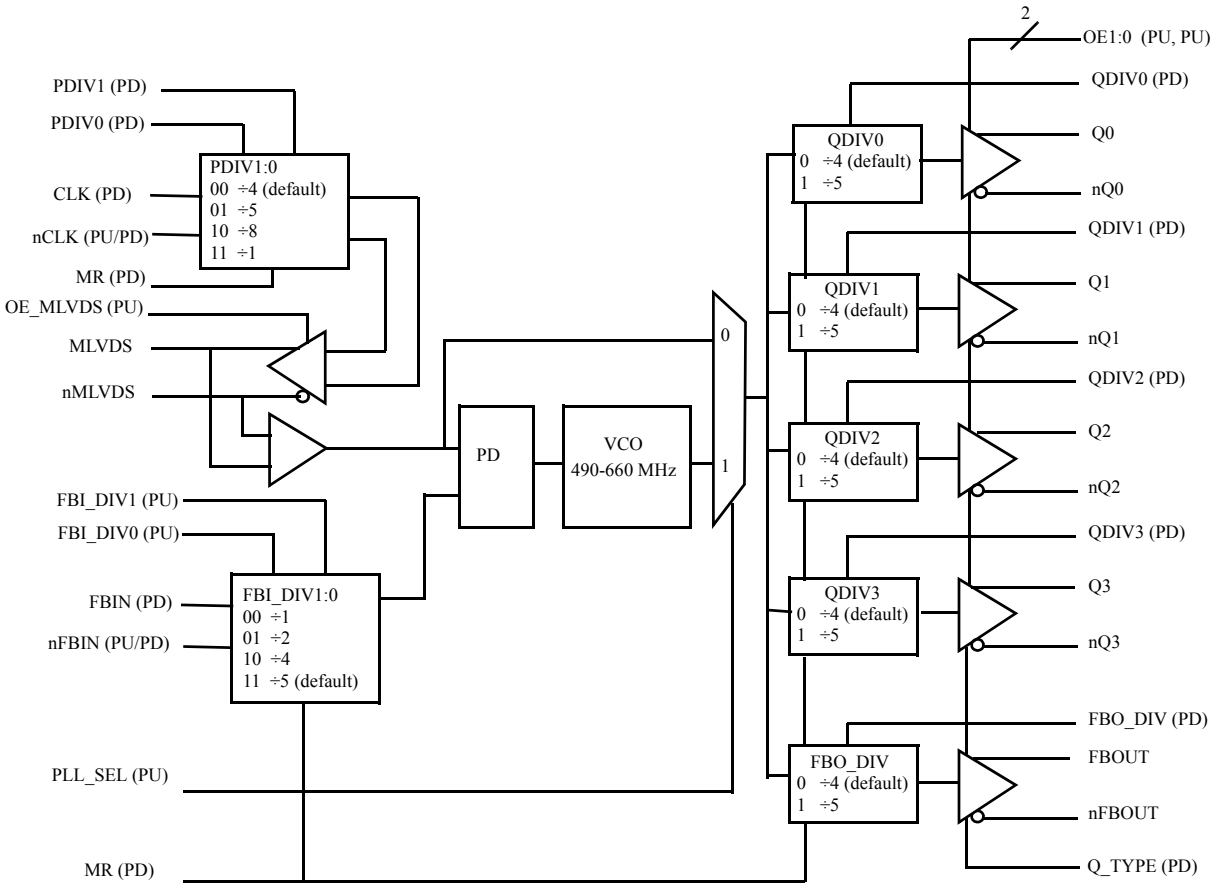
Pin Assignment



ICS8743004I
40-Lead VFQFN
6mm x 6mm x 0.925mm package body
K Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

Block Diagram



PU means internal pull-up resistor on pin (power-up default is HIGH if not externally driven)
PD means internal pull-down resistor on pin (power-up default is LOW if not externally driven)

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 11	V_{DD}	Power		Core supply pins.
2	OE_MLVDS	Input	Pullup	Active High Output Enable. When HIGH, the M-LVDS output driver is active and provides a buffered copy of reference clock applied the CLK/nCLK input to the MLVDS/nMLVDS output pins. The MLVDS/nMLVDS frequency equals the CLK/ nCLK frequency divided by the PDIV Divider value (selectable ÷1, ÷4, ÷5, ÷8). When LOW, the M-LVDS output driver is placed into a Hi-Z state and the MLVDS/nMLVDS pins can accept a differential input. LVCMOS/LVTTL interface levels.
3	MLVDS	I/O		Non-Inverting M-LVDS input/output. The input/output state is determined by the OE_MLVDS pin. When OE_MLVDS = HIGH, this pin is an output and drives the non-inverting M-LVDS output. When OE_MLVDS = LOW, this pin is an input and can accept the following differential input levels: M-LVDS, LVDS, LVPECL, HSTL, HCSL.
4	nMLVDS	I/O		Inverting M-LVDS input/output. The input/output state is determined by the OE_MLVDS pin. When OE_MLVDS = HIGH, this pin is an output and drives the inverting M-LVDS output. When OE_MLVDS = LOW, this pin is an input and can accept the following differential input levels: M-LVDS, LVDS, LVPECL, HSTL, HCSL. The output driver is always M-LVDS and is not affected by the state of the Q-TYPE pin which affects Q0/nQ0:Q3/nQ3, and FBOUT/nFBOUT.
5	PLL_SEL	Input	Pullup	PLL select. Determines if the PLL is in bypass or enabled mode (default). In enabled mode, the output frequency = VCO frequency/QDIV divider. In bypass mode, the output frequency = reference clock frequency/ (PDIV*QDIV). LVCMOS/LVTTL interface levels.
6	FBO_DIV	Input	Pulldown	Output Divider Control for the feedback output pair, FBOUT/nFBOUT. Determines if the output divider = ÷4 (default), or ÷5. LVCMOS/LVTTL interface levels.
7	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the Qx/nQx outputs to drive Hi-Z. Note that assertion of MR overrides the OE[0:2] control pins and all outputs are disabled. When logic LOW, the internal dividers are enabled and the state of the outputs is determined by OE[0:2]. MR must be asserted on power-up to ensure outputs phase aligned. LVCMOS/LVTTL interface levels.
8	OE0	Input	Pullup	Output Enable. Together with OE1, determines the output state of the outputs with the default state: all output pairs switching. When an LVDS or LVPECL output pair is disabled, the disable state is Qx/nQx = Hi-Z. It should also be noted that the feedback output pins (FBOUT/nFBOUT) are always switching and are not affected by the state of OE[0:1]. Refer to table 3B for truth table. LVCMOS/LVTTL Interface levels.
9	OE1	Input	Pullup	Output Enable. Together with OE0, determines the output state of the outputs with the default state: all output pairs switching. When an LVDS or LVPECL output pair is disabled, the disable state is Qx/nQx = Hi-Z. It should also be noted that the feedback output pins (FBOUT/nFBOUT) are always switching and are not affected by the state of OE[1:0]. Refer to table 3B for truth table. LVCMOS/LVTTL Interface levels
10, 16, 27	GND	Power		Power supply ground.
12	FBI_DIV0	Input	Pullup	Feedback Input Divide Select 0. Together with FB_DIV1, determines the feedback input divider value. LVCMOS/LVTTL interface levels.

Pin Descriptions continue on the next page.

Number	Name	Type		Description
13	FBI_DIV1	Input	Pullup	Feedback Input Divide Select 1. Together with FB_DIV0, determines the feedback input divider value. LVCMOS/LVTTL interface levels.
14	nFBIN	Input	Pullup/ Pulldown	Inverted differential feedback input to phase detector for regenerating clocks with “Zero Delay.”
15	FBIN	Input	Pulldown	Non-inverted differential feedback input to phase detector for regenerating clocks with “Zero Delay.”
17	QDIV0	Input	Pulldown	Output Divider Control for Q0/nQ0. Determines if the output divider = ÷4 (default), or ÷5. LVCMOS/LVTTL interface levels.
18	QDIV1	Input	Pulldown	Output Divider Control for Q1/nQ1. Determines if the output divider = ÷4 (default), or ÷5. LVCMOS/LVTTL interface levels.
19	QDIV2	Input	Pulldown	Output Divider Control for Q2/nQ2. Determines if the output divider = ÷4 (default), or ÷5. LVCMOS/LVTTL interface levels.
20	QDIV3	Input	Pulldown	Output Divider Control for Q3/nQ3. Determines if the output divider = ÷4 (default), or ÷5. LVCMOS/LVTTL interface levels.
21	Q_TYPE	Input	Pulldown	Output Type Select. 0 = LVDS outputs (default); 1 = LVPECL outputs on Q0/nQ0:Q3/nQ3, and FBOUT/nFBOUT. The MLVDS/nMLVDS driver is always M-LVDS and is NOT affected by the state of this pin. LVCMOS/LVTTL interface levels.
22, 30, 35	V_{DDO}	Power		Output supply pins.
23, 24	nFBOUT FBOUT	Output		Differential feedback output pair. The feedback output pair always switches independent of the output enable settings on the OE[1:0] pins. LVDS or LVPECL interface levels.
25, 26	nQ3/Q3	Output		Differential LVDS or LVPECL output pair. The output type is controlled by the Q_TYPE pin as follows: Q_TYPE = 0 LVDS (default); Q_TYPE = 1 LVPECL.
28, 29	nQ2/Q2	Output		Differential LVDS or LVPECL output pair. The output type is controlled by the Q_TYPE pin as follows: Q_TYPE = 0 LVDS (default); Q_TYPE = 1 LVPECL.
31, 32	nQ1/Q1	Output		Differential LVDS or LVPECL output pair. The output type is controlled by the Q_TYPE pin as follows: Q_TYPE = 0 LVDS (default); Q_TYPE = 1 LVPECL.
33, 34	nQ0/Q0	Output		Differential LVDS or LVPECL output pair. The output type is controlled by the Q_TYPE pin as follows: Q_TYPE = 0 LVDS (default); Q_TYPE = 1 LVPECL.
36	V_{DDA}	Power		Analog supply pin.
37	CLK	Input	Pulldown	Non-inverting differential clock input. Accepts HCSL, LVDS, M-LVDS, HSTL input levels.
38	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. Accepts HCSL, LVDS, M-LVDS, HSTL input levels.
39	PDIV0	Input	Pulldown	Input Divide Select 0. Together with PDIV1 determines the input divider value. LVCMOS/LVTTL Interface levels.
40	PDIV1	Input	Pulldown	Input Divide Select 1. Together with PDIV0 determines the input divider value. LVCMOS/LVTTL Interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Common Configuration Table (not exhaustive) NOTE 1

Input Frequency	Output Frequency	Application	Frequency Mult. Factor	PDIV	FBI_DIV	FBO_DIV	QDIVx
100MHz	100MHz	PCIe Buffer	1	÷1	÷1	÷5	÷5
125MHz	125MHz	PCIe, Ethernet Buffer	1	÷1	÷1	÷4	÷4
100MHz	125MHz	PCIe Multiplier	5/4	÷1	÷1	÷5	÷4
125MHz	100MHz	PCIe Divider	4/5	÷1	÷1	÷4	÷5
25MHz	100MHz	PCIe Multiplier	4	÷1	÷4	÷5	÷5
25MHz	125MHz	PCIe, Ethernet Multiplier	5	÷1	÷4	÷5	÷4
25MHz	156.25MHz	XAUI Multiplier	25/4	÷1	÷5	÷5	÷4
62.5MHz	125MHz	Ethernet Multiplier	2	÷1	÷2	÷4	÷4
53.125MHz	106.25MHz	Fibre Channel Multiplier	2	÷1	÷2	÷5	÷5

NOTE 1: This table shows more common configurations and is not exhaustive. When using alternate configurations, the designer must ensure the VCO frequency is always within its range of 490MHz – 660MHz.

Table 3B. Output Enable Truth Table

Inputs		State
OE1	OE0	Q[0:3] /nQ[0:3]
0	0	Q0/nQ0 switching, Q1/nQ1, Q2/nQ2, Q3/nQ3 disabled (Qx/nQx = Hi-Z)
0	1	Q0/nQ0, Q1/nQ1 switching, Q2/nQ2, Q3/nQ3 disabled (Qx/nQx = Hi-Z)
1	0	Q0/nQ0, Q1/nQ1, Q2/nQ2 switching, Q3/nQ3 disabled (Q3/nQ3 = Hi-Z)
1	1	All output pairs switching (default)

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVDS) Continuos Current Surge Current Outputs, I_O (LVPECL) Continuos Current Surge Current	 10mA 15mA 50mA 100mA
Package Thermal Impedance, θ_{JA}	32.4°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. LVDS Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.18	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			140		mA
I_{DDA}	Analog Supply Current			18		mA
I_{DDO}	Output Supply Current			140		mA

Table 4B. LVPECL Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.19	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current			240		mA
I_{DDA}	Analog Supply Current			19		mA

Table 4C. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	PDIV[0:1], QDIV[0:3], MR, FBO_DIV, Q_TYPE	$V_{DD} = V_{IN} = 3.465V$			150	µA
		OE_MLVDS, OE[0:1], FBI_DIV[0:1], PLL_SEL	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	PDIV[0:1], QDIV[0:3], MR, FBO_DIV, Q_TYPE	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5			µA
		OE_MLVDS, OE[0:1], FBI_DIV[0:1], PLL_SEL	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA

Table 4D. Differential DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK/nCLK, FBIN/nFBIN	$V_{DD} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	CLK, FBIN	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5			µA
		nCLK, nFBIN	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

Table 4E. LVDS DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			360		mV
ΔV_{OD}	V_{OD} Magnitude Change			20		mV
V_{OS}	Offset Voltage			1.31		V
ΔV_{OS}	V_{OS} Magnitude Change			25		mV

Table 4F. M-LVDS DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			440		mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage			1.6		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV
I_{SC}	Output Short Circuit Current			48		mA

Table 4G. LVPECL DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Current; NOTE 1		$V_{DDO} - 1.4$		$V_{DDO} - 0.9$	µA
V_{OL}	Output Low Current; NOTE 1		$V_{DDO} - 2.0$		$V_{DDO} - 1.7$	µA
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs termination with 50Ω to V_{DDO} – 2V.

AC Electrical Characteristics

Table 5A. LVDS AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		98		160	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1			25		ps
*t*sk(o)	Output Skew; NOTE 2			60		ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 3	125MHz, Integration Range: 1.875MHz – 20MHz		0.65		ps
		100MHz, Integration Range: 1.875MHz – 20MHz		0.73		ps
t_j	Phase Jitter Peak-to-Peak; NOTE 4	125MHz, (1.2MHz – 21.9MHz), 10^6 samples		13.49		ps
$t_{REFCLK\_HF\_RMS}$	Phase Jitter RMS; NOTE 5	125MHz		1.29		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		600		ps
odc	Output Duty Cycle			50		%

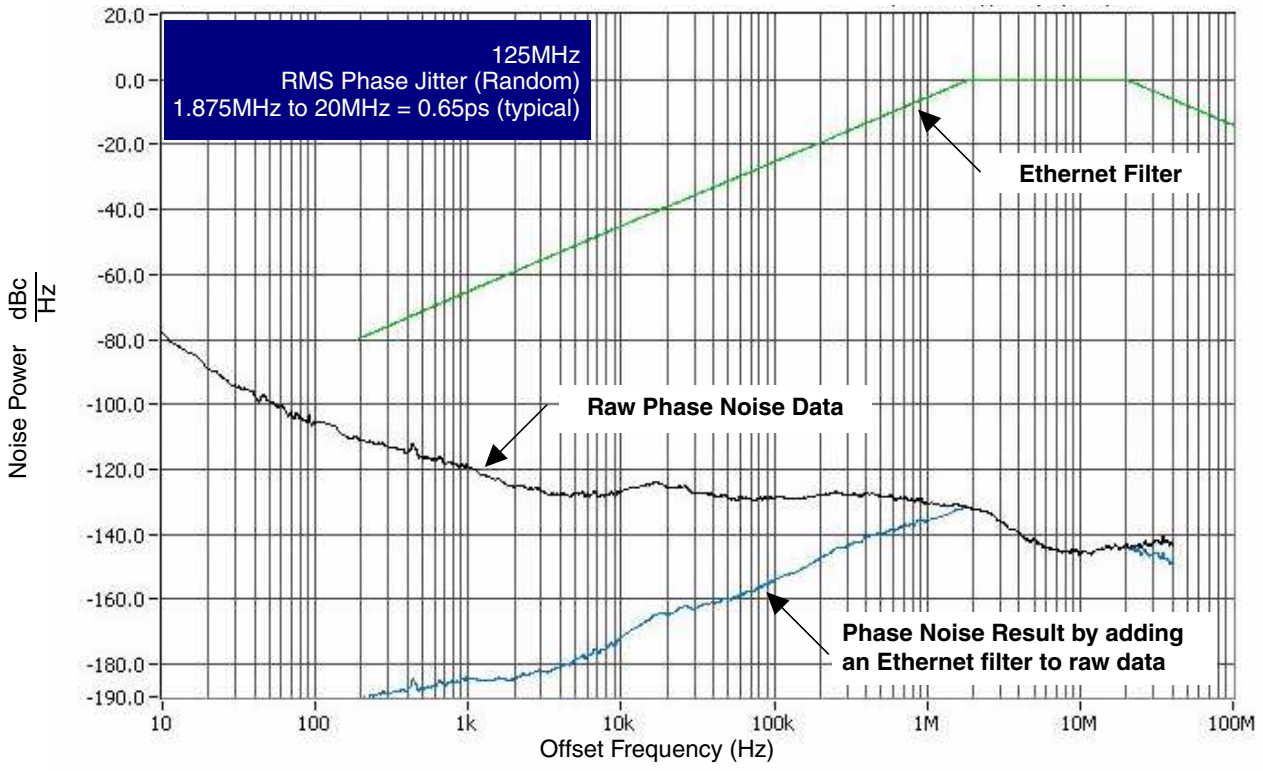
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the differential cross points.
NOTE 3: Please refer to the Phase Noise plots.
NOTE 4: RMS jitter after applying system transfer function. See IDT Application Note *PCI Express Reference Clock Requirements.* Maximum limit for PCI Express is 86ps peak-to-peak.
NOTE 5: RMS jitter after applying system transfer function. The pole frequencies for H1 and H2 for PCIe Gen 2 are 8-16MHz and 5-16MHz. See IDT Application Note *PCI Express Reference Clock Requirements.* Maximum limit for PCI Express Generation 2 is 3.1ps rms.

Table 5B. LVPECL AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

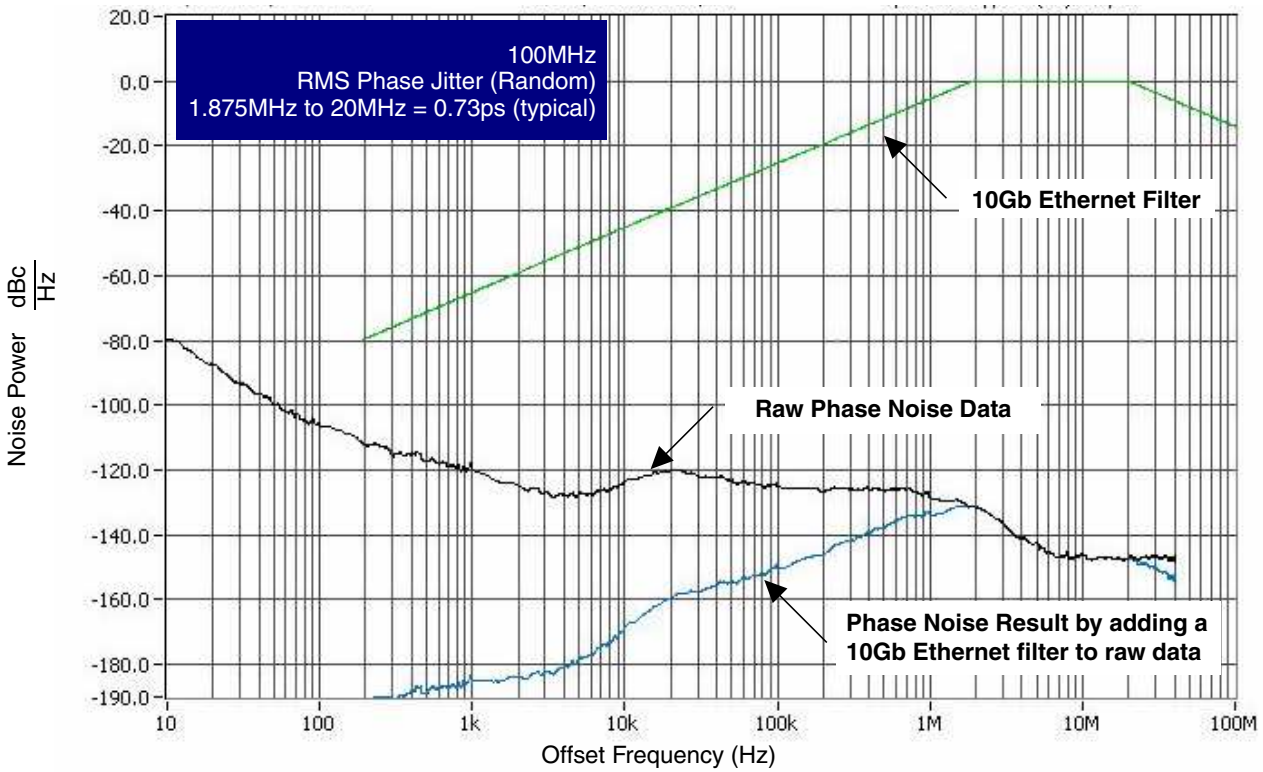
Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		98		160	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1			25		ps
*t*sk(o)	Output Skew; NOTE 2			60		ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 3	125MHz, Integration Range: 1.875MHz – 20MHz		0.57		ps
		100MHz, Integration Range: 1.875MHz – 20MHz		0.69		ps
t_j	Phase Jitter Peak-to-Peak; NOTE 4	125MHz, (1.2MHz – 21.9MHz), 10^6 samples		13.49		ps
$t_{REFCLK\_HF\_RMS}$	Phase Jitter RMS; NOTE 5	125MHz		1.29		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		600		ps
odc	Output Duty Cycle			50		%

NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the differential cross points.
NOTE 3: Please refer to the Phase Noise plots.
NOTE 4: RMS jitter after applying system transfer function. See IDT Application Note *PCI Express Reference Clock Requirements.*
Maximum limit for PCI Express is 86ps peak-to-peak.
NOTE 5: RMS jitter after applying system transfer function. The pole frequencies for H1 and H2 for PCIe Gen 2 are 8-16MHz and 5-16MHz. See IDT Application Note *PCI Express Reference Clock Requirements.* Maximum limit for PCI Express Generation 2 is 3.1ps rms.

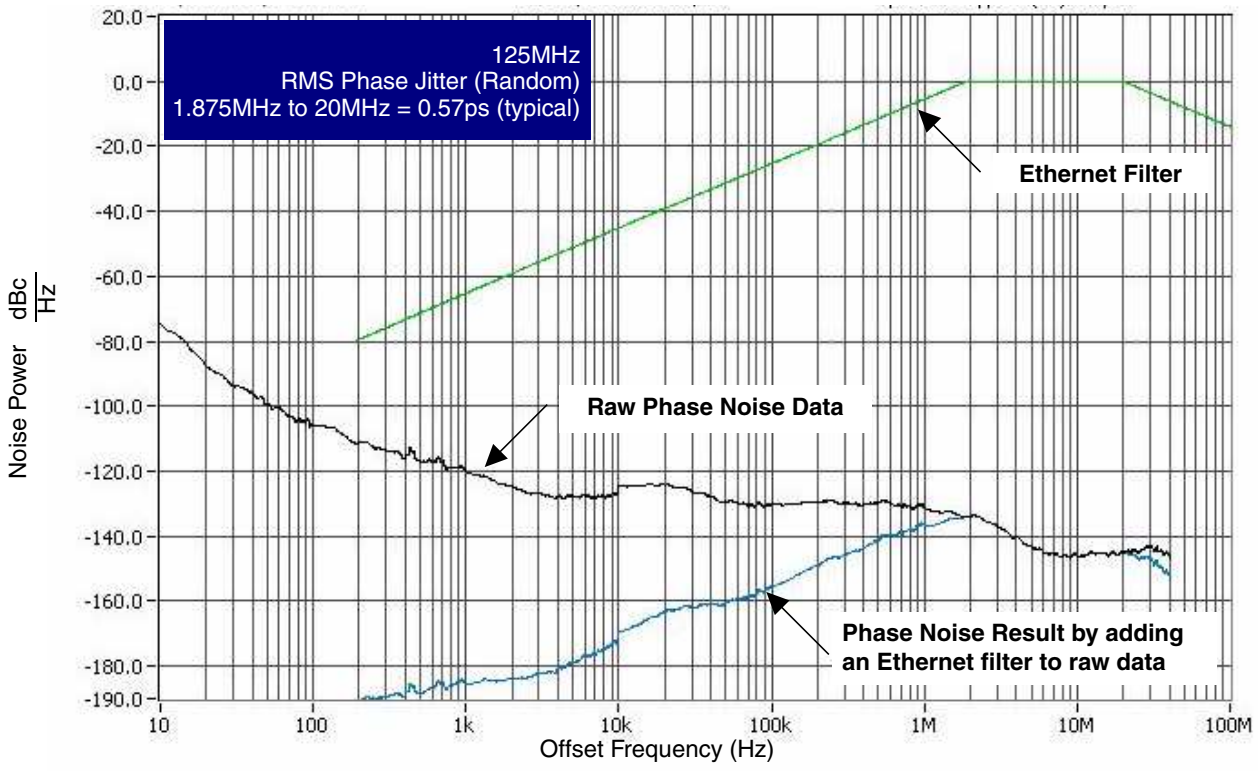
Typical LVDS Phase Noise at 125MHz



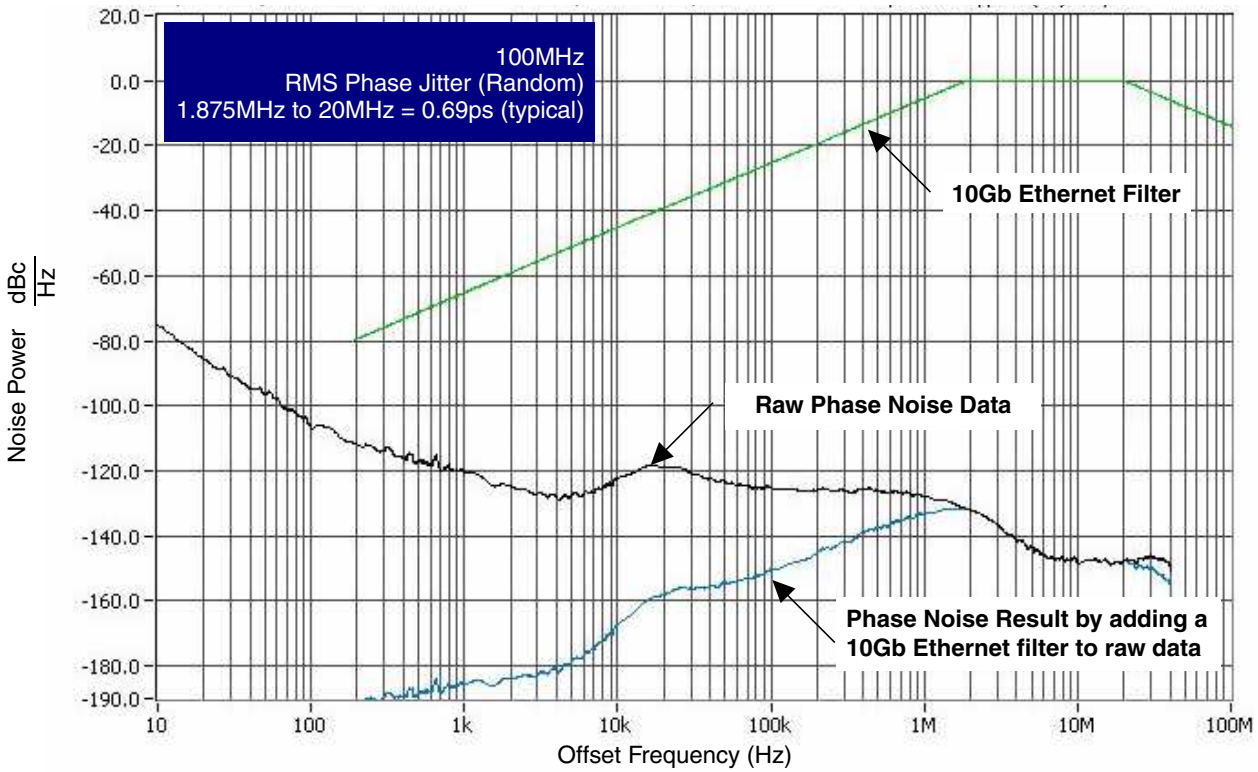
Typical LVDS Phase Noise at 100MHz



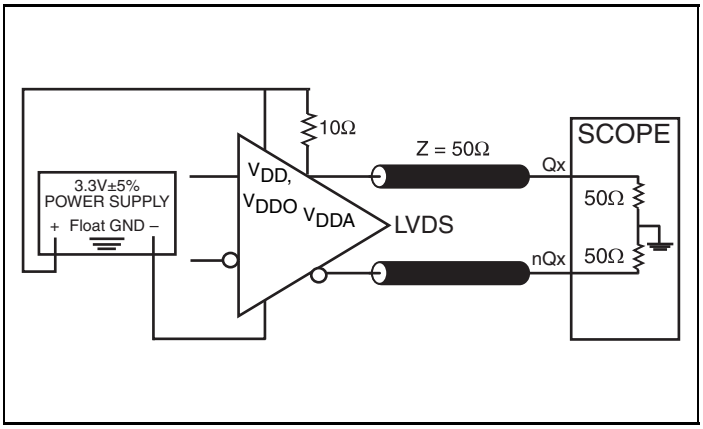
Typical LVPECL Phase Noise at 125MHz



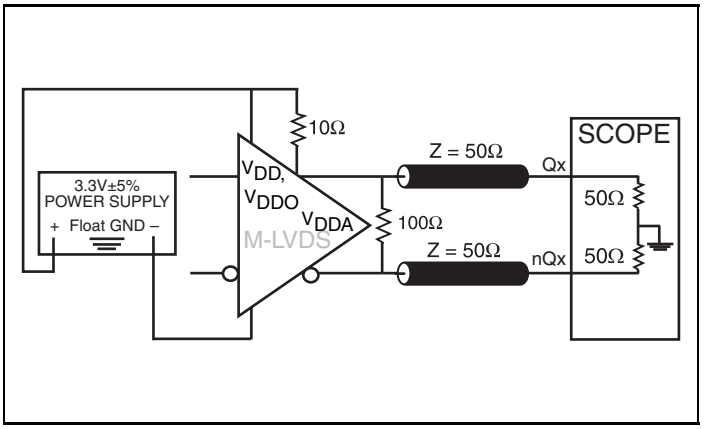
Typical LVPECL Phase Noise at 100MHz



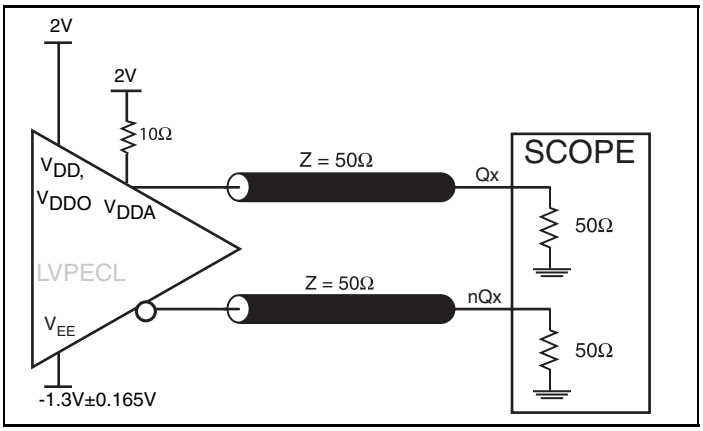
Parameter Measurement Information



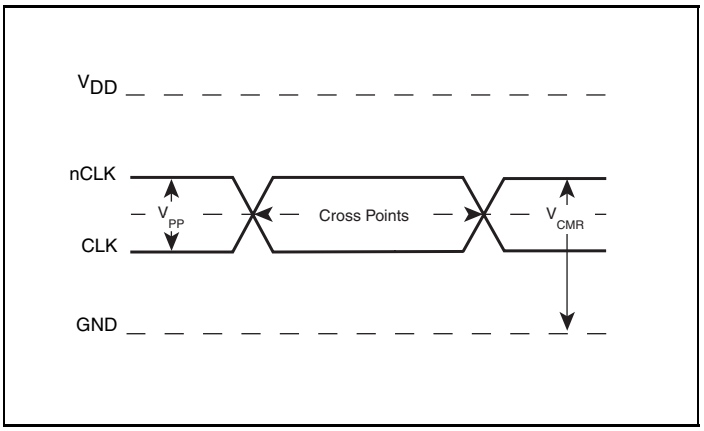
3.3V LVDS Output Load AC Test Circuit



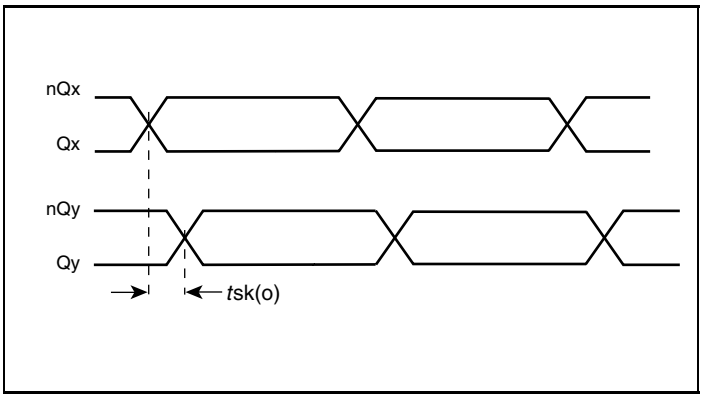
3.3V M-LVDS Output Load AC Test Circuit



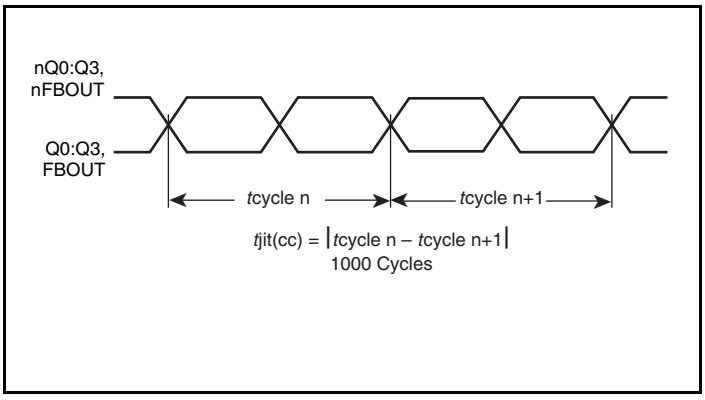
3.3V LVPECL Output Load AC Test Circuit



Differential Input Level

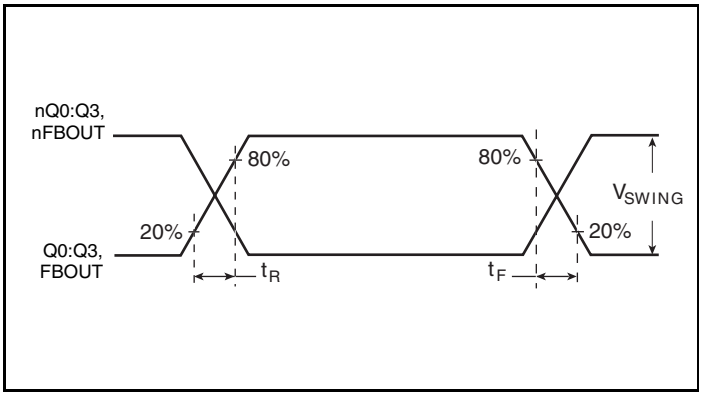


Output Skew

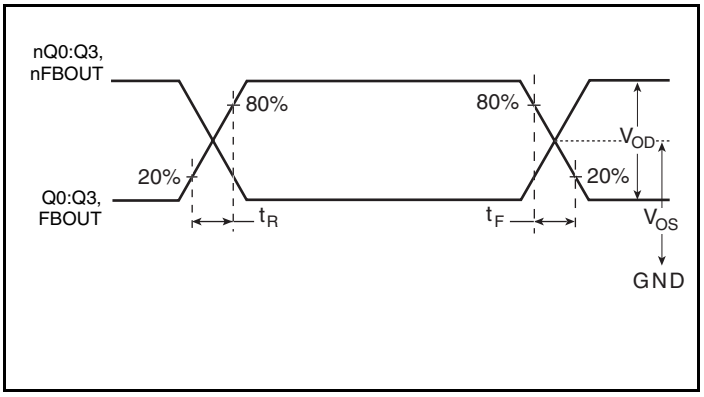


Cycle-to-Cycle Jitter

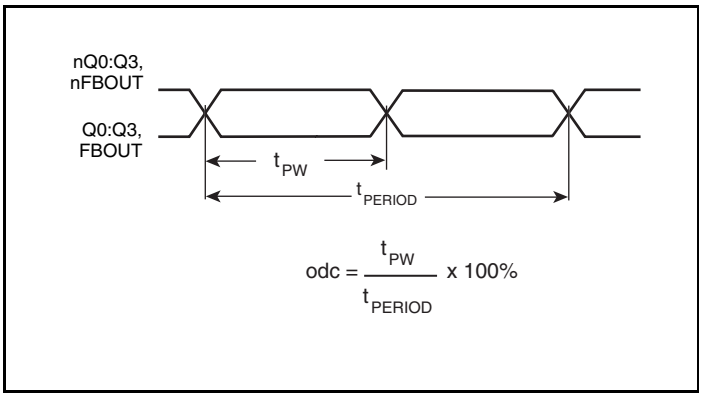
Parameter Measurement Information, continued



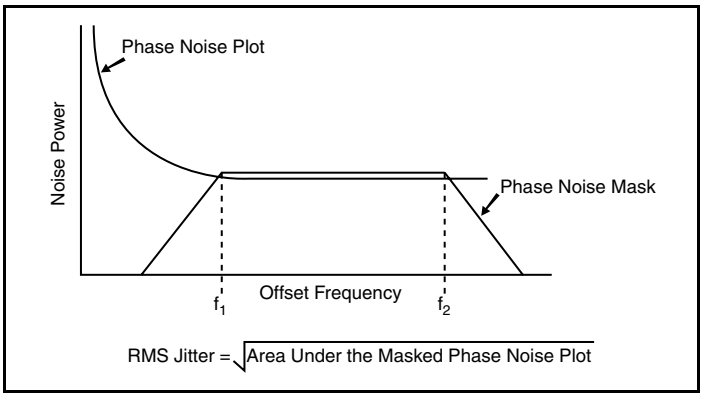
LVPECL Output Rise/Fall Time



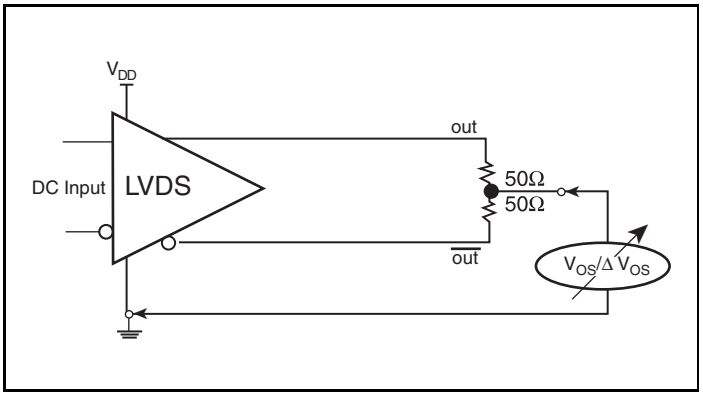
LVDS Output Rise/Fall Time



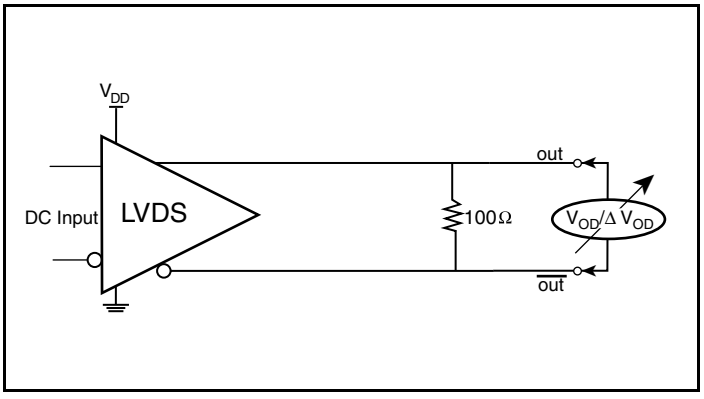
LVPECL/LVDS Output Duty Cycle/Pulse Width/Period



RMS Phase Jitter

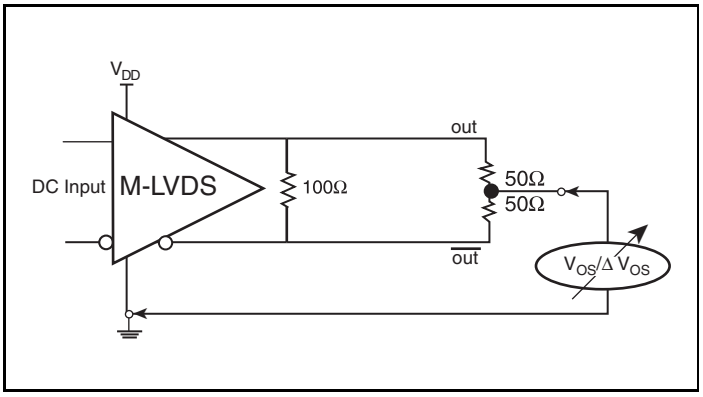


Offset Voltage Setup

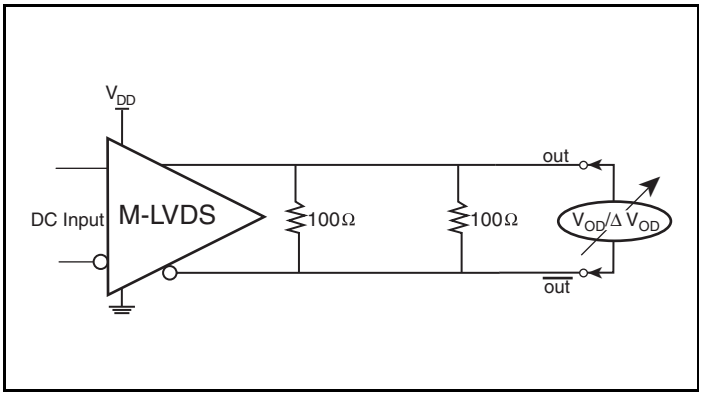


Differential Output Voltage Setup

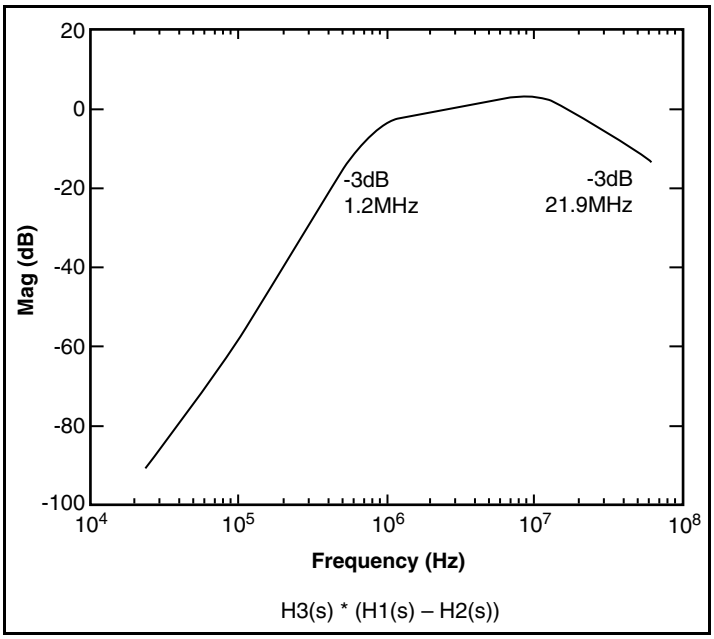
Parameter Measurement Information, continued



M-LVDS Offset Voltage Setup



M-LVDS Differential Output Voltage Setup



Composite PCIe Transfer Function

Application Information

Overview

The is a high performance FemtoClock Zero Delay Buffer/ Multiplier/Divider which uses external feedback for accurate clock regeneration and low static and dynamic phase offset. It can be used in a number different ways:

- Backplane clock multiplier. Many backplane clocks are relatively low frequency because of heavy electrical loading. The ICS8743004I can multiply a low frequency backplane clock (e.g. 25MHz) to an appropriate reference clock frequency for PCIe, Ethernet, 10G Ethernet: 100MHz, 125MHz, 156.25MHz. The device can also accept a high frequency local reference (100MHz or 125 MHz, for example) and divide the frequency down to 25MHz M-LVDS to drive a backplane.
- PCIe frequency translator for PCIe add-in cards. In personal computers, the PCIe reference clock is 100MHz, but some 2.5G serdes used in PCI Express require a 125MHz reference. The ICS8743004I can perform the 100MHz → 125MHz and 125MHz → 100MHz frequency translation for a PCI Express add-in card while delivering low dynamic and static phase offset.
- General purpose, low phase noise Zero Delay Buffer

Configuration Notes and Examples

When configuring the output frequency, the main consideration is keeping the VCO within its range of 490MHz - 660MHz. The designer must ensure that the VCO will always be within its allowed range for the expected input frequency range by using the appropriate choice of feedback output and input dividers. There are two input modes for the device. In the first mode, a reference clock is provided to the CLK/nCLK input and this reference clock is divided by the value of the PDIV divider (selectable ÷1, ÷4, ÷5, ÷8). In the second mode, a reference clock is provided to the MLVDS/ nMLVDS input pair. OE_MLVDS determines the input mode. When OE_MLVDS = HIGH (default), the M-LVDS driver is active and provides an M-LVDS output to the MLVDS/nMLVDS pins and also the reference to the phase detector via the PDIV divider. When OE_MLVDS is LOW, the internal M-LVDS driver is in Hi-Z state and the MLVDS/nMLVDS pin pair becomes an input and the reference clock applied to this input is applied to the phase detector.

MLVDS/nMLVDS Output Mode

OE_MLVDS = HIGH (default)

VCO frequency = CLK/nCLK frequency * FBI_DIV * FBO_DIV/ (PDIV value)

Allowed VCO frequency = 490MHz – 660MHz

Output frequency = VCO frequency/QDIVx value = CLK/nCLK freq. * FBI_DIV * FBO_DIV/(PDIV*QDIVx)

Example: a frequency synthesizer provides a 125MHz reference clock to CLK/nCLK input. The ICS8743004I must provide a 25MHz M-LVDS clock to the backplane and also provide two local clocks: one 100MHz LVDS output to an ASIC and one 125MHz output to the PCI Express serdes.

Solution. Since only two outputs are needed, the two unused outputs can be disabled. Set OE[1:0] = 01b so that only Q0/nQ0 and Q1/nQ1 are switching. Since a 25MHz backplane clock is needed from a 125MHz reference clock, set PDIV = ÷5 and OE_MLVDS = HIGH to enable the M-LVDS driver. 25MHz is applied to the MLVDS/nMLVDS pins and to the phase detector input. Set FBO_DIV = 4 and FBI_DIV = 5 which makes the VCO run at 500MHz (25MHz * 4 * 5 = 500MHz). Set QDIV0 = 0 (÷4) for 125MHz output and QDIV1 = 1 (÷5) for 100MHz output. To figure out what pins must pulled up or down externally with resistors, check the internal pullup or pulldown resistors on each pin in the pin description table or on the block diagram. PDIV[1:0] defaults to 00/÷4 and we need 01/÷5. So PDIV1 can be left floating (it has an internal pulldown resistor) and PDIV0 must be driven or pulled up via external pullup resistor to HIGH state. OE_MLVDS defaults to Logic 1 (active) and this is what we need, so that pin can be left floating. The FBO_DIV and FBIN dividers default to the desired values, so their respective control pins can be left floating (FBO_DIV and FBI_DIV[1:0]). QDIV0 needs to be ÷4, which is a default value so this pin can be left floating. QDIV1 must be HIGH for ÷5, so this pin must be pulled high or driven high externally. OE[1:0] = 01, so OE0 can Float and OE1must be pulled Low.

MLVDS/nMLVDS Input Mode

OE_MLVDS = LOW

VCO frequency = MLVDS/nMLVDS freq. * FBI_DIV * FBO_DIV

Output frequency = VCO frequency/QDIVx value = MLVDS/nMLVDS freq. * FBI_DIV * FBO_DIV/(QDIVx)

Example - backplane: The 8743004I sits on a backplane card and must multiply a 25MHz reference that comes from the backplane into one 125MHz reference clock for a gigabit Ethernet serdes and one 100MHz reference clock for a PCI Express serdes.

Solution. Since only two outputs are needed, the two unused outputs can be disabled. Set OE1:0 = 01b so that only Q0/nQ0 and Q1/nQ1 are switching. Set OE_MLVDS = 0 so the internal M-LVDS driver is in a Hi-Z state, allowing the MLVDS/nMLVDS pins to function as an input for the 25MHz clock reference. Set FBO_DIV = 4 and FBI_DIV = 5 which makes the VCO run at 500MHz (25MHz * 4 * 5 = 500MHz). Set QDIV0 = 0 (÷4) for 125MHz output and QDIV1 = 1 (÷5) for 100MHz output. To figure out what pins must pulled up or down externally with resistors, check the internal pullup or pulldown resistors on each pin in the pin description table or on the block diagram. PDIV[1:0] defaults to 00/÷4 and we need 01/÷5. So PDIV1 can be left floating (it has an internal pulldown resistor) and PDIV0 must be driven or pulled up via external pullup

resistor to HIGH state. OE_MLVDS defaults to Logic 1 (active) and this is what we need, so that pin can be left floating. The FBO_DIV and FBIN dividers default to the desired values, so their respective control pins can be left floating (FBO_DIV and FBI_DIV1:0).

QDIV0 needs to be ÷4, which is a default value so this pin can be left floating. QDIV1 must be HIGH for ÷5, so this pin must be pulled high or driven high externally. OE[1:0] = 01, so OE0 can Float and OE1must be pulled Low.

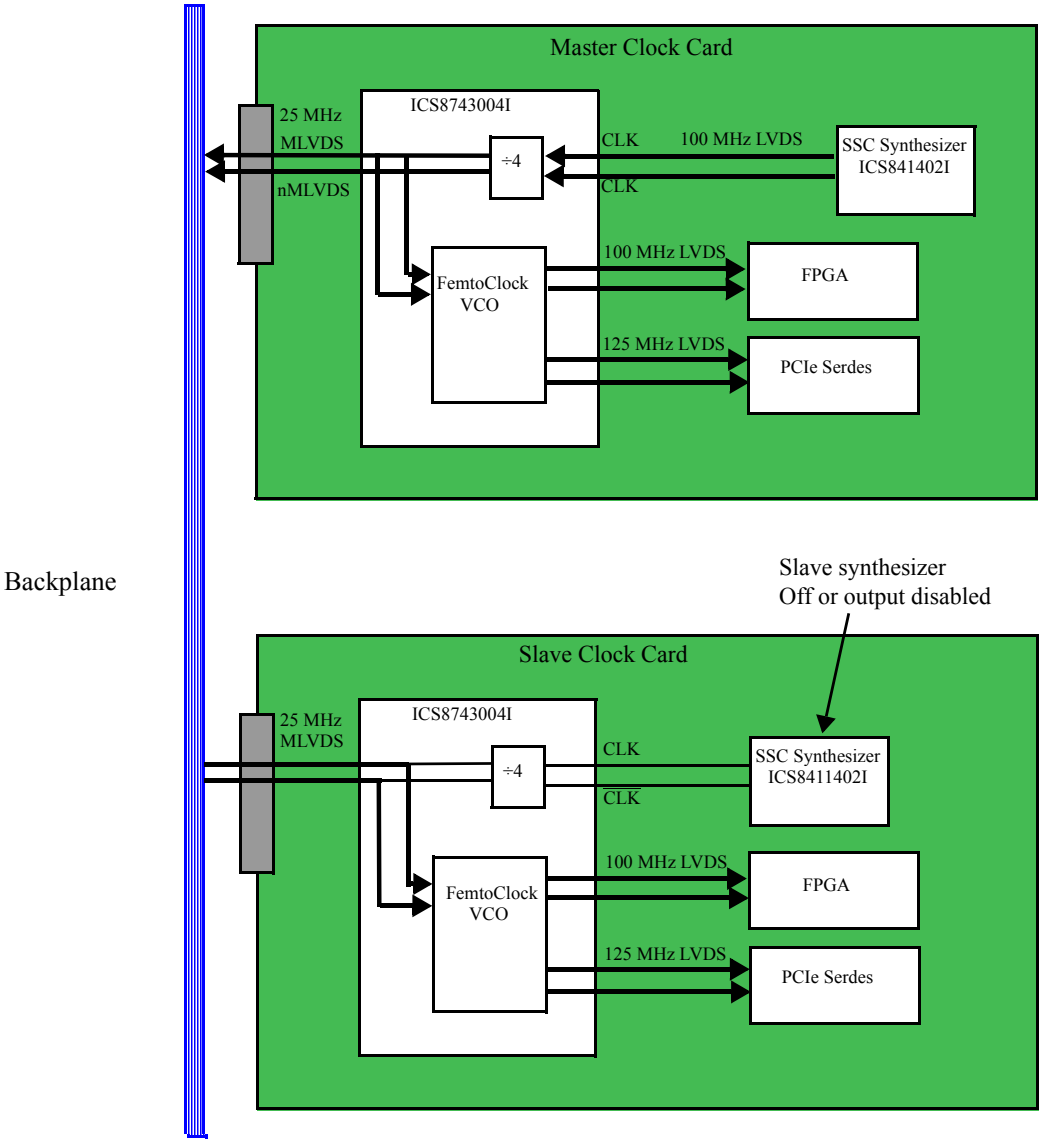


Figure 1, Example Backplane Application

Bold lines ⟶ indicate active clock path

This example shows a case where each card may be dynamically configured as a master or slave card, hence the need for an ICS8743004I and ICS841402I on each card. On the master timing card, the ICS841402I provides a 100MHz reference to the ICS8743004I CLK/nCLK input. The M-LVDS pair on the ICS8743004I is configured as an output (OE_MLVDS = Logic 1) and the internal divider is set to ÷4 to generate 25MHz M-LVDS to the backplane. The 25MHz clock is also used as a reference to the FemtoClock PLL which multiplies to a VCO frequency of 500MHz.

Each of the four output pairs may be individually set for ÷4 or ÷5 for 125MHz or 100MHz operation respectively and in this example, one output pair is set to 100MHz for the FPGA and another output pair is set to 125MHz for the PCI Express serdes. For the slave card, the M-LVDS pair is configured as an input (OE_MLVDS = LOW) and the FemtoClock PLL multiplies this reference frequency to 500MHz VCO frequency and the output dividers are set to provide 100MHz to the FPGA and 125MHz to the PCI Express Serdes as shown.

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS8743004I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 2* illustrates how a 10Ω resistor along with a 10µF and a 0.01µF bypass capacitor should be connected to each V_{DDA} pin.

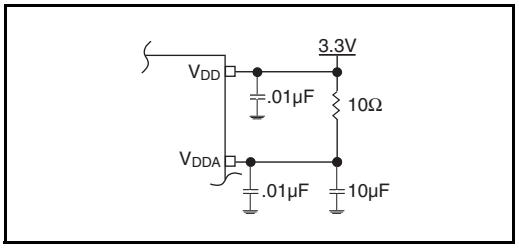


Figure 2. Power Supply Filtering

Wiring the Differential Input to Accept Single Ended Levels

Figure 3 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

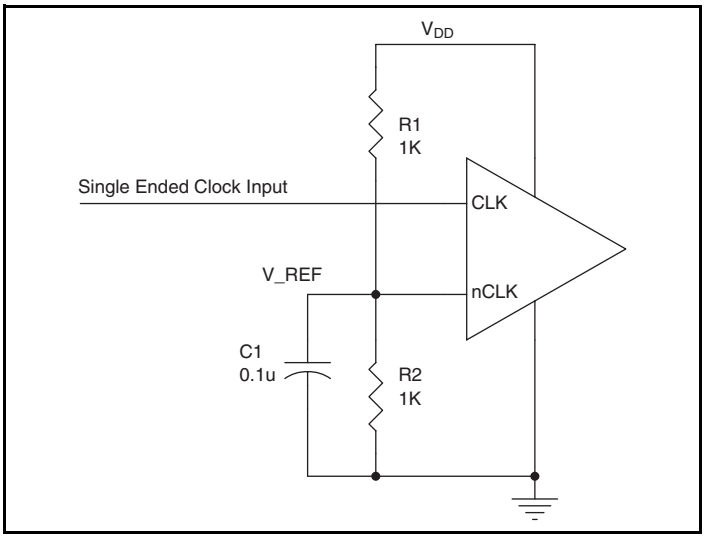


Figure 3. Single-Ended Signal Driving Differential Input

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4E* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 4A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

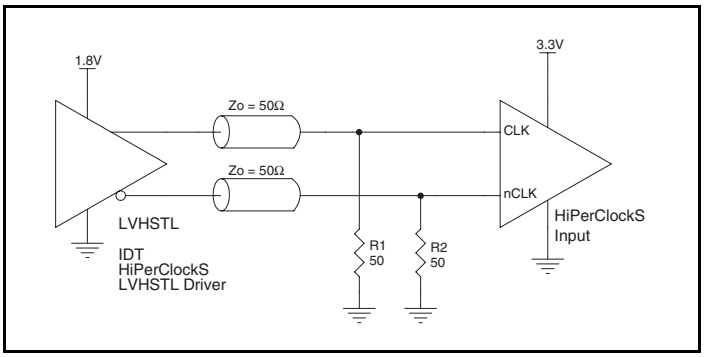


Figure 4A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

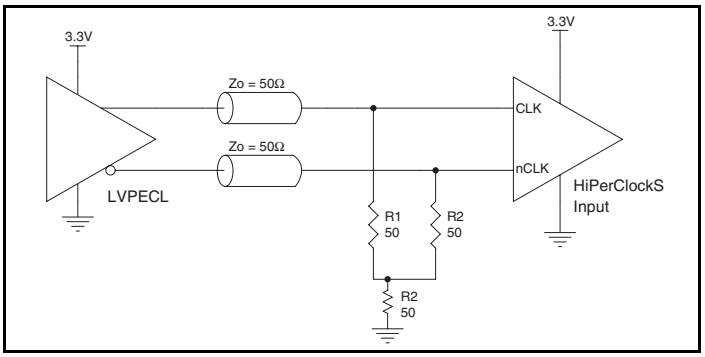


Figure 4B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

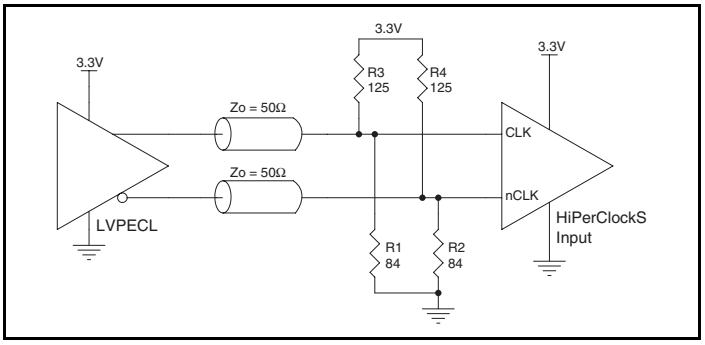


Figure 4C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

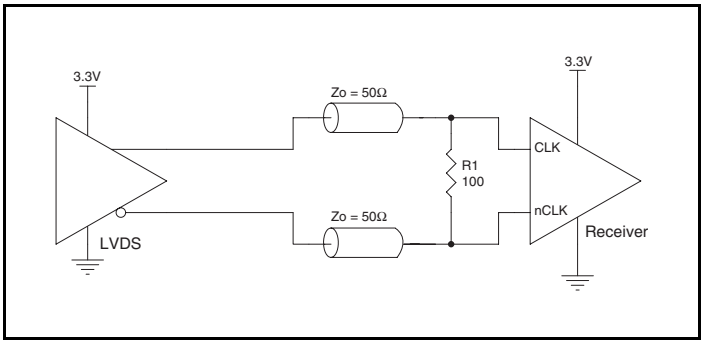


Figure 4D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

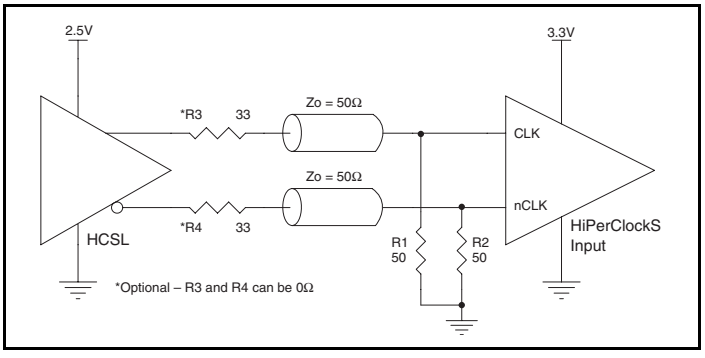


Figure 4E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadfame Base Package, Amkor Technology.

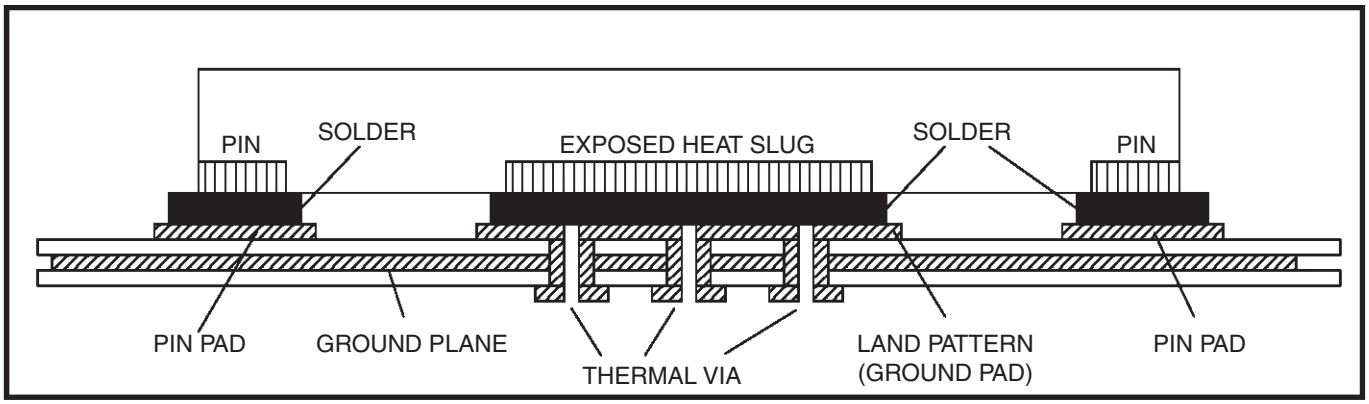


Figure 5. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

3.3V LVDS Driver Termination

A general LVDS interface is shown in *Figure 6.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input.

For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

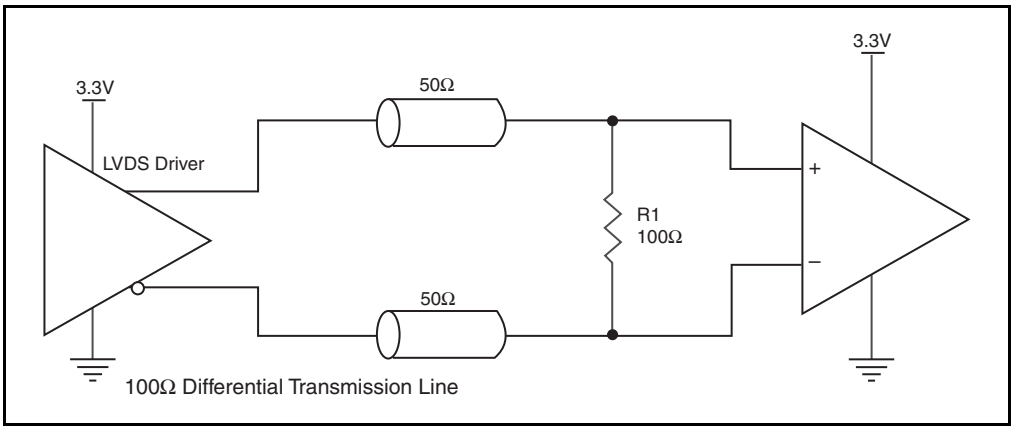


Figure 6. Typical LVDS Driver Termination

3.3V M-LVDS Driver Termination

A general M-LVDS interface is shown in *Figure 7* In a 100Ω differential transmission line environment, M-LVDS drivers require a matched load termination of 100Ω across near the receiver input.

For a multiple M-LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

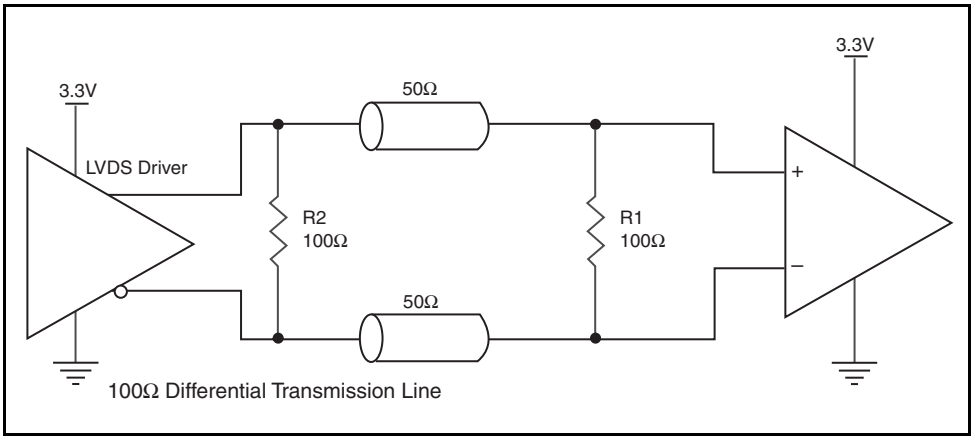


Figure 7. Typical M-LVDS Driver Termination

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 8A and 8B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

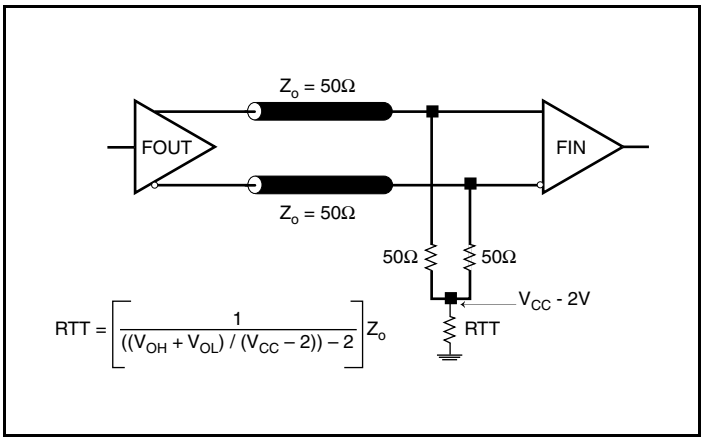


Figure 8A. 3.3V LVPECL Output Termination

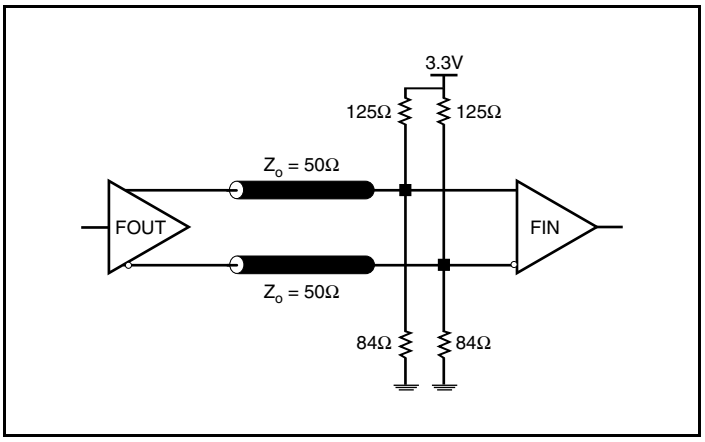


Figure 8B. 3.3V LVPECL Output Termination

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

MLVDS/nMLVDS Inputs

For applications not requiring the use of the differential input, both MLVDS and nMLVDS can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from MLVDS to ground.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

M-LVDS Outputs

All unused M-LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

Power Considerations – LVPECL Outputs

This section provides information on power dissipation and junction temperature for the ICS8743004I, for all outputs that are configured to LVPECL. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8743004I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{EE\_MAX}$ = 3.465V * 240mA = **831.6mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 30mW = **120mW**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 831.6mW + 120mW = **951.6mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 32.4°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.952W * 32.4°C/W = 115.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board.

Table 6. Thermal Resistance θ_{JA} for 40 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	32.4°C/W	28.3°C/W	25.4°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 9.*

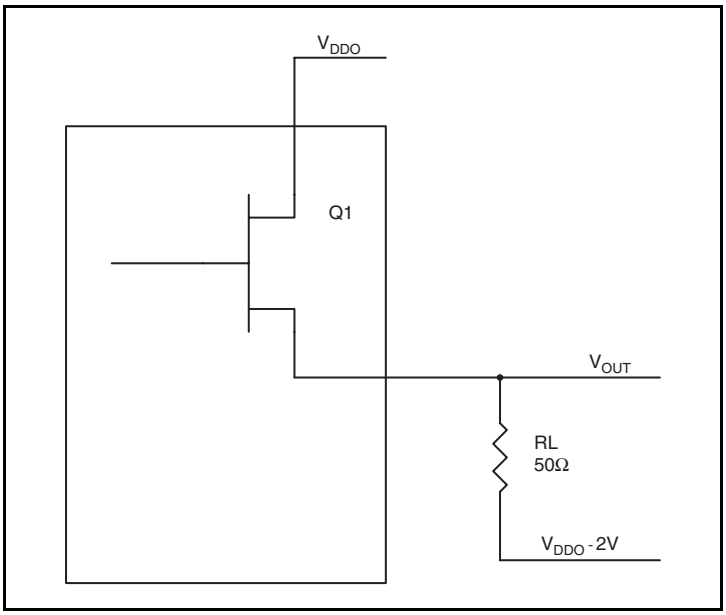


Figure 9. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{DDO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{DDO\_MAX} – 0.9V}$
  $(V_{DDO\_MAX} – V_{OH\_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{DDO\_MAX} – 1.7V}$
  $(V_{DDO\_MAX} – V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{DDO\_MAX} – 2V))/R_L] * (V_{DDO\_MAX} – V_{OH\_MAX}) = [(2V – (V_{DDO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{DDO\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{DDO\_MAX} – 2V))/R_L] * (V_{DDO\_MAX} – V_{OL\_MAX}) = [(2V – (V_{DDO\_MAX} – V_{OL\_MAX}))/R_L] * (V_{DDO\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Power Considerations – LVDS Outputs

This section provides information on power dissipation and junction temperature for the ICS8743004I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8743004I is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power (core)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (140mA + 18mA) = **547.47mW**
- Power (outputs)$_{MAX}$ = V_{DDO_MAX} * I_{DDO_MAX} = 3.465V * 140mA = **485.1mW**

Total Power$_{\_MAX}$ = 547.47mW + 485.1mW = **1032.57mW**

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2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 32.4°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.033W * 32.4°C/W = 118.5°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board.

Table 7. Thermal Resistance θ_{JA} for 40 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	32.4°C/W	28.3°C/W	25.4°C/W

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 40 Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	32.4°C/W	28.3°C/W	25.4°C/W

Transistor Count

The transistor count for ICS8743004I is: 4893

Package Outline and Package Dimensions

Package Outline - K Suffix for 40 Lead VFQFN

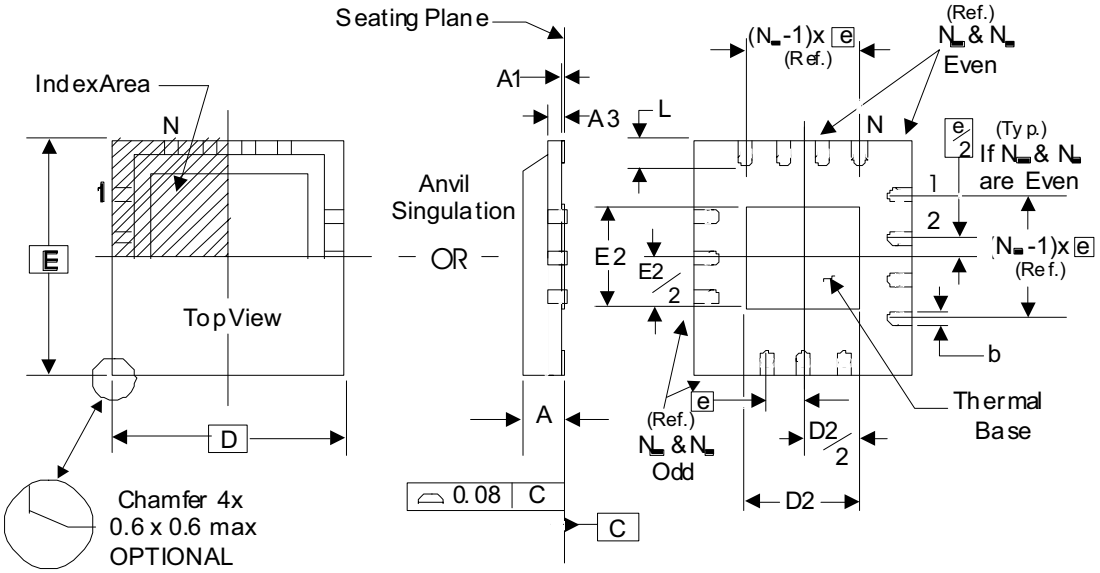

Table 9. Package Dimensions

JEDEC Variation: VJJD-2/-5 All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	40	
A	0.80	1.00
A1	0	0.05
A3	0.25 Ref.	
b	0.18	0.30
N_D & N_E	10	
D & E	6.00 Basic	
D2 & E2	1.75	4.80
e	0.50 Basic	
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 8 below