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SN820X Family Data Sheet

Wi-Fi Network Controller Module

Revision History

Revision	Date	Author	Change Description
0.1	12/09/2012	Y. Fang	Initial version
0.5	02/03/2012	Y. Fang	Preliminary version
0.6	02/20/2012	N. Nagayama	Update performance data and adjusted table format
0.7	04/20/2012	J. Gregus	Update CE compliance information
1.0	08/27/2012	Y. Fang	Formal release
1.1	01/23/2013	Y. Fang	Added Power Rail Current specification and Standby Mode Current specification
1.2	05/30/2013	R. Willett	Changed specs in Table 1 for Pin 2, 3, 4, and 30
1.3	09/20/2013	R Willett	Separated Data Sheet/User Manual and created new data sheet combining SN8200/8200 UFL and SN8205/8205 UFL
1.4	11/07/13	R. Willett	Added Acronyms list; Revised Fig. 1.1, 2.1; revised content and renumbered tables in Chap. 3: added Chapters 4 - 10 and reorganized information; amended regulatory information.
1.5	11/11/13	R Willett	Revised Operating Temperature specification on page 6; revised Table 5.1 “Absolute Maximum Ratings,” page 38.
2.0	11/25/13	R Willett	Removed references to SyChip; updated copyright, deleted Chap 11, “Disclaimer;”
2.1	12/17/13	R. Willett	Added text describing module software download in Chapter 1, page 7.
2.2	02/28/14	R. Willett	Revised text on page 42, Table 9.2.
3.0	07/25/14	R. Willett	Reformatted document to new Murata visual identity; Added Anatel certification, page 39
3.1	8/22/14	R. Willett	Revised Table 5.1 to include VDD, VBAT and VDD_WiFi.
3.2	3/21/16	R. Willett	Deleted minimum values for Receive Sensitivity on Table 4.1.1 page 34, Table 4.2.1 page 35, and Table 4.3.1 page 36; updated Murata address on page 42.

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Table of Contents

List of Figures

List of Tables

1 Introduction

1.1 Model SN820X Module Family

The SN820X Module Family is a portfolio of low power, self-contained, embedded wireless module solutions that address the connectivity demands of M2M applications. These products integrate a micro-controller, a Wi-Fi BB/MAC/RF IC, an RF front end and two clocks into small form factor modules. The module family includes 2 different micro-controller options as shown below. The modules can also be purchased with either a standard on-board chip antenna or a U.FL connector where remote antenna flexibility is required.

TABLE 1.1: SN820X WiFi Network Controller Module Family

Model #	P/N	Built-in STM	RAM Size	Flash Size
SN8200	88-00151-00	ARM Cortex M3	96KB	768KB
SN8200UFL	88-00151-02	ARM Cortex M3	96KB	768KB
SN8205	88-00158-00	ARM Cortex M3	128KB	1024KB
SN8205UFL	88-00158-02	ARM Cortex M3	128KB	1024KB

1.2 Model SN820X Module Features

- 2.4 GHz IEEE 802.11 b/g/n radio technology
- Dimensions: 30.5 × 19.4 × 2.8 mm
- Antenna configurations: On-board antenna or U.FL connector
- Transmitter power: +18 dBm @80211b
- Receiver sensitivity: -96 dBm
- MCU: ARM Cortex-M3
- Serial Interface Options: UART, SPI
- Peripheral Interface Options: ADC, DAC, I2C, I2S, GPIO
- Operating temperature range: -40 ºC to +85 ºC
- RoHS2 compliant
- MSL Level 3
- FCC/IC certified and CE compliant
- Compatible with Broadcom WICED™ SDK

1.3 Block Diagram

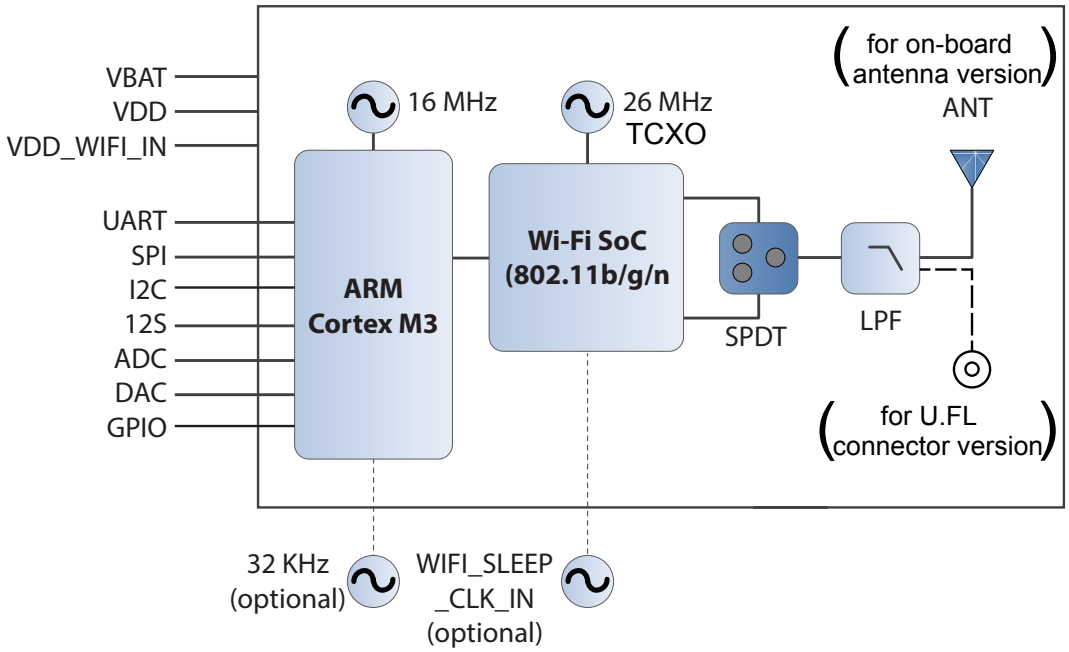


FIGURE 1.1: SN820X Block Diagram

Murata offers Serial-to-WiFi and EZ Web Wizzard software for SN820x in the SN820x EVK+. The modules are also compatible with Broadcom WICED™ SDK. The customer can obtain the WICED™ SDK from Broadcom directly. **The modules are delivered with no application firmware pre-installed.**

Finalize the firmware image, and then download the firmware to the module. For more details, please see reference [4].

1.4 Acronyms

- **ADC** Analog to Digital Converter
- **DAC** Digital to Analog Converter
- **GPIO** General-Purpose Input-Output
- **I2C** Intelligent Interface Controller
- **I2S** Integrated Interchip Sound
- **ISM** Industrial, Scientific and Medical
- **MAC** Medium Access Control
- **MSL** Moisture Sensitivity Level
- **PER** Packet Error Rate
- **ROHS** Restriction of Hazardous Substances
- **SPI** Serial Peripheral Interface
- **UART** Universal Asynchronous Receiver-Transmitter

1.5 References

[1] STM32F103RF Data Sheet, ST Microelectronics
[2] STM32F205RG, Data Sheet, ST Microelectronics
[3] SN820X Wi-Fi Network Controller Module Family User Manual, Murata
[4] AN_SN8200_002 SN820X Firmware Downloading Application Note, Murata

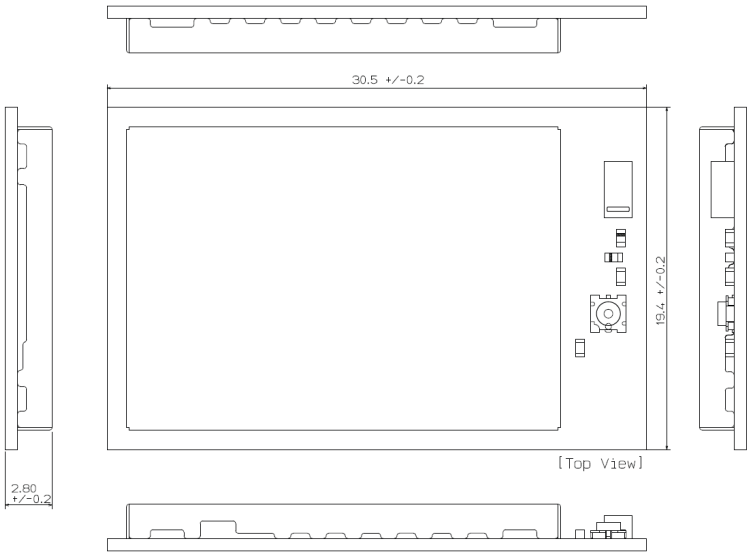
2 Mechanical Specifications

2.1 Module Dimensions

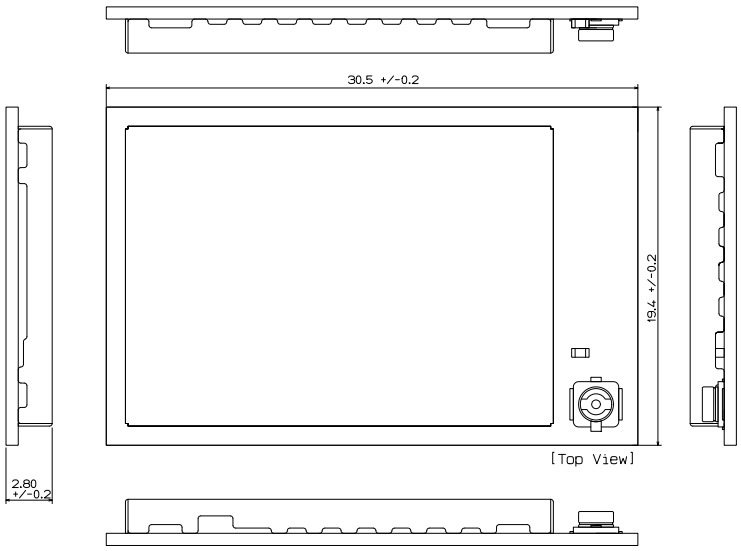
TABLE 2.1: Module Dimensions

Parameter	Typical	Units
Dimensions (LxWxH)	30.5 x 19.4 x 2.8	mm
Dimension tolerances (LxWxH)	±0.2	mm

2.2 Top and Side View



SN820X Top and Side View



SN820XUFL Top and Side View

FIGURE 2.1: SN820X and SN820XUFL Top and Side View

2.3 PCB Footprint (top view)

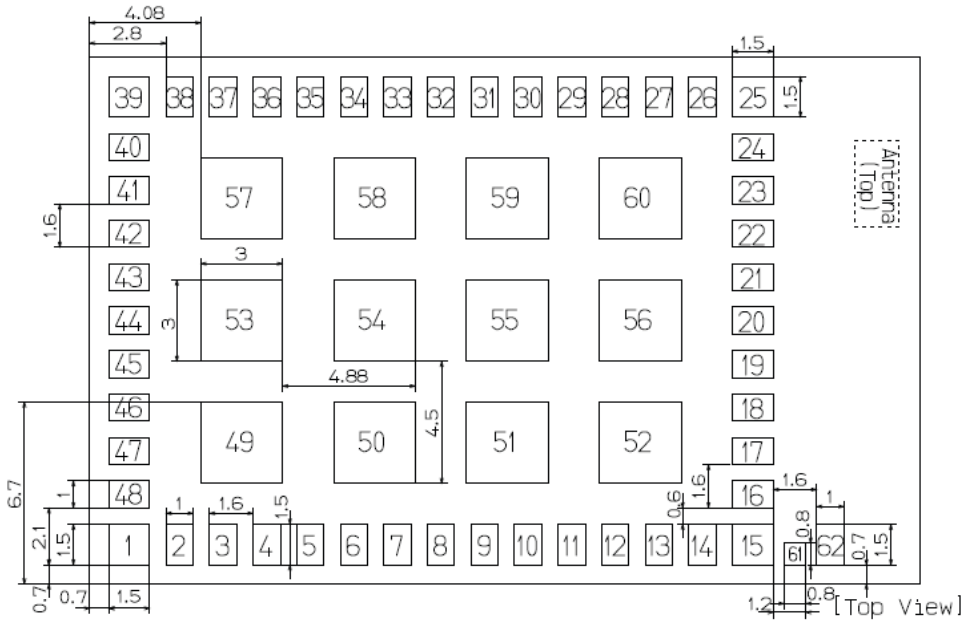


FIGURE 2.2: Detailed Pad Dimensions (top view)

2.4 Pinouts

TABLE 2.2: Pinouts

Pin #	Pin Name	I/O	Description
1	GND	-	Ground
2	OSC32_IN	I/O	Optional precision 32.768 KHz slow clock input. No connect if not used
3	OSC32_OUT	I/O	No connect
4	WIFI_VDD_EN	I/O	No connect
5	ADC3	I/O	General purpose I/O or ADC3
6	ADC4	I/O	General purpose I/O or ADC4
7	ADC5	I/O	General purpose I/O or ADC5
8	VDD	PI	DC supply for MCU and I/O
9	ADC6	I/O	General purpose I/O or ADC6
10	DAC2	I/O	General purpose I/O or DAC2
11	DAC1	I/O	General purpose I/O or DAC1
12	ADC1	I/O	General purpose I/O or ADC1
13	Reserved	-	No connect
14	Reserved	-	No connect
15	GND	-	Ground
16	GND	-	Ground
17	GND	-	Ground
18	GND	-	Ground
19	GND	-	Ground
20	GND	-	Ground
21	GND	-	Ground
22	GND	-	Ground
23	GND	-	Ground
24	GND	-	Ground
25	GND	-	Ground
26	VDD_WIFI_IN	PI	Wi-Fi power supply
27	Reserved	-	No connect
28	Reserved	-	No connect
29	Reserved	-	No connect
30	WIFI_SLEEP_CLK_IN	I	Optional precision 32.768 kHz Wi-Fi sleep clock input. Tie to GND if not used
31	GND	-	Ground
32	UART_TX	I/O	General purpose I/O or UART_TX
33	UART_RX	I/O	General purpose I/O or UART_RX
34	UART_CTS	I/O	General purpose I/O or UART_CTS
35	UART_RTS	I/O	General purpose I/O or UART_RTS
36	JTMS	I/O	General purpose I/O or JTMS

TABLE 2.2: Pinouts (Continued)

Pin #	Pin Name	I/O	Description
37	JTDI/SPI_NSS	I/O	General purpose I/O or JTDI or SPI_NSS
38	JTCK	I/O	General purpose I/O or JTCK
39	Ground	-	Ground
40	JTDO/SPI_SCK	I/O	General purpose I/O or JTDO or SPI_SCK
41	JTRST/SPI_MISO	I/O	General purpose I/O or JTRST or SPI_MISO
42	SPI_MOSI	I/O	General purpose I/O or SPI_MOSI
43	I2C_SCL	I/O	General purpose I/O or I2C_SCL
44	I2C_SDA	I/O	General purpose I/O or I2C_SDA
45	BOOT	-	Normal operation if connected to ground at power up.
46	ADC2	I/O	General purpose I/O or ADC2
47	MICRO_RST_N	I	Module reset
48	VBAT	PI	Power supply for backup circuitry when VDD is not present
49	GND	-	Ground
50	GND	-	Ground
51	GND	-	Ground
52	GND	-	Ground
53	GND	-	Ground
54	GND	-	Ground
55	GND	-	Ground
56	GND	-	Ground
57	GND	-	Ground
58	GND	-	Ground
59	GND	-	Ground
60	GND	-	Ground
61	Reserved	-	No connect
62	GND	-	Ground

TABLE 2.3: Signal Pinouts for SN820X/820XUFL

Pin	Pin name	STM32F103RF/STM32F205RG pin
5	ADC3	PA0/WKUP/ADC123_0/USART2_CTS TIM2_CH1_ETR/ TIM5_CH1 / TIM8_ETR
6	ADC4	PA1/ADC123_1/USART2_RTS TIM2_CH2 / TIM5_CH2
7	ADC5	PA2/ADC123_2/USART2_TX TIM2_CH3 / TIM5_CH3 / TIM9_CH1
9	ADC6	PA3/ADC123_3/USART2_RX TIM2_CH4 / TIM5_CH4 / TIM9_CH2
10	DAC2	PA4/ADC12_4/DAC1/USART2_CK/SPI1_NSS
11	DAC1	PA5/ADC12_5/DAC2/SPI1_SCK
12	ADC1	PA7/ADC12_7/SPI1_MOSI
32	UART_TX	PA9/UART1_TX
33	UART_RX	PA10/UART1_RX
34	UART_CTS	PA11/UART1_CTS/USB2_DM/CAN_RX
35	UART_RTS	PA12/UART1_RTS/USB2_DP/CAN_TX
36	JTMS	PA13/JTMS/SWIO
37	JTDI/SPI_NSS	PA15/JTDI/SPI3_NSS/I2S3_WS
38	JTCK	PA14/JTCK/SWCLK
40	JTDO/SPI_SCK	PB3/JTDO/SPI3_SCK/I2S3_CK
41	JTRST/SPI_MISO	PB4/JTRST/SPI3_MISO
42	SPI_MOSI	PB5/I2C1_SMBA/SPI3_MOSI/ I2S3_SD
43	I2C_SCL	PB6/I2C1_SCL TIM4_CH1
44	I2C_SDA	PB7/I2C1_SDA TIM4_CH2
46	ADC2	PA6/ADC12_6/SPI1_MISO

3 DC Electrical Specifications

The I/O pins from SN820X are based on the built-in STM32 microcontroller. The information shown in sections 3.2 through 3.8 is derived from the ST Microelectronics Data Sheet for user convenience. For original information, see reference [1] and [2] on page of References.

3.1 Typical Power Consumption

TABLE 3.1.1: SN8200/SN8200UFL and SN8205/SN8205 UFL Typical Power Consumption

Item		Condition	Values			Units
			Min	Typ	Max	
11b	Receive mode	11 Mbps		110		mA
	Transmit mode (18 dBm/ 100% Duty Cycle)			370		mA
11g	Receive mode	54 Mbps		110		mA
	Transmitmode (14.5 dBm/100% Duty Cycle)			290		mA
11n	Receive mode	MCS7		110		mA
	Transmit mode (13.5 dBm/ 100% Duty Cycle)			280		mA
Standby Mode with IEEE802.11 Power Save		DTIM 1, Telnet session established and idling		3.15		mA
Standby Mode with IEEE802.11 Power Save		DTIM 3, Telnet session established and idling		1.28		mA

3.2 GPIO Interface

The general purpose I/O (GPIO) pins available on the SN820X will connect to various external devices. GPIOs are configured as input floating by default. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. They can also be programmed to have internal pull-up or pull-down resistors. The MICRO_RST_N pin is connected to a permanent pull-up resistor, R_{PU}.

TABLE 3.2.1: Digital I/O Characteristics SN8200/SN8200UFL

	SYM	min.	typ.	max.	unit
Input Low Voltage[1]	V_{IL}	-0.3		0.28 (V_{DD}-2) +0.8	V
Input High Voltage[1]	V_{IH}	0.41 (V_{DD}-2) +1.3		V_{DD}+0.3	V
Input Low Voltage[2]	V_{IL}	-0.3		0.32 (V_{DD}2) +0.75	V
Input High Voltage[2]	V_{IH}	0.42 (V_{DD}-2) +1		V_{DD} +0.5	V
Input Low Voltage (MICRO_RST_N)	V_{IL}	-0.5		0.8	V
Input High Voltage (MICRO_RST_N)	V_{IH}	2		V_{DD} + 0.5	V
Output Low Voltage	V_{OL}			0.4	V
Output High Voltage	V_{OH}	V_{DD} - 0.4			V
Weak Pull-up Equivalent Resistor	R_{PU}	30	40	50	kΩ
Weak Pull-down Equivalent resistor	R_{PD}	30	40	50	kΩ

1 - for pins 5, 6, 7, 9, 10, 11, 12, 42, 46

2 - for pins 32 - 38, 40, 41, 43, 44

TABLE 3.2.2: Digital I/O Characteristics, SN8205/8205UFL

	SYM	min.	typ.	max.	unit
Input Low Voltage[1]	V_{IL}	-0.3		0.3 V_{DD}	V
Input High Voltage[1]	V_{IH}	0.7 V_{DD}		3.6	V
Input Low Voltage[2]	V_{IL}	-0.3		0.3 V_{DD}	V
Input High Voltage[2]	V_{IH}	0.7		3.6	V
Input Low Voltage (MICRO_RST_N)	V_{IL}	-0.5		0.8	V
Input High Voltage (MICRO_RST_N)	V_{IH}	2		V_{DD} + 0.5	V
Output Low Voltage	V_{OL}			0.4	V
Output High Voltage	V_{OH}	V_{DD} - 0.4			V
Weak Pull-up Equivalent Resistor	R_{PU}	30/8*	40/11*	50/15*	kΩ
Weak Pull-down Equivalent resistor	R_{PD}	30/8*	40/11*	50/15*	kΩ

1 - for pins 5, 6, 7, 9, 10, 11, 12, 42, 46

2 - for pins 32-38, 40, 41, 43, 44

(*) - Pin 33

3.3 Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed VOL/VOH) except PC13, PC14 and PC15 which can sink or source up to ±3mA. When using the PC13 to PC15 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

- In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in Table 3.3.1.
- The sum of the currents sourced by all the I/Os on VDD, plus the maximum Run consumption of the MCU sourced on VDD, cannot exceed the absolute maximum rating IVDD.

TABLE 3.3.1: Voltage Characteristics, SN820X

Symbol	Ratings	Min	Max	U
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA}, V_{DD})(1)	–0.3	4.0	V
V_{IN}	Input voltage on five-volt tolerant pin(2)	V_{SS}–0.3	V_{DD}+4	
	Input voltage on any other pin	V_{SS}–0.3	4.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)		2000	V

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum value must always be respected.

TABLE 3.3.2: Current Characteristics, SN8200/8200UFL

Symbol	Ratings	Max.	Uni
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	25	
$I_{INJ(PIN)}$(2)	Injected current on five volt tolerant pins(3)	-5/+0	
	Injected current on any other pin(4)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	± 25	

TABLE 3.3.3: Current Characteristics, SN8205/8205UFL

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(1)	120	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	120	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	25	
$I_{INJ(PIN)}$ (2)	Injected current on five-volt tolerant I/O(3)	-5/+0	
	Injected current on any other pin(4)	±5	
$\Sigma I_{INJ(PIN)}$(4)	Total injected current (sum of all I/O and control pins)(5)	±25	

1. All main power (V_{DD}, $V_{DDA)}$ and ground (V_{SS}, $V_{SSA)}$ pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device.
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS.}$ $I_{INJ(PIN)}$ must never be exceeded.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values)

3.4 Output Voltage Levels

Unless otherwise specified, the parameters given in Table 3.4.1 and Table 3.4.2 are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions. All I/Os are CMOS and TTL compliant.

TABLE 3.4.1: Output Voltage Characteristics, SN8200/SN8200UFL

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL port(3) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(2)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}—0.4		
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS port(3) I_{IO}=+ 8mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(2)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		2.4		

TABLE 3.4.1: Output Voltage Characteristics, SN8200/SN8200UFL (Continued)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL} (1)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OL} (2)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}—1.3		
V_{OL} (1)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO}= +6 mA 2 V < V_{DD} < 2.7 V		0.4	V
V_{OL} (2)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}—0.4		

1. The IIO current sunk by the device must always respect the absolute maximum rating specified in Table 3.4.1 and the sum of IIO (I/O ports and control pins) must not exceed IVSS.
2. The IIO current sourced by the device must always respect the absolute maximum rating specified in Table 3.4.1 and the sum of IIO (I/O ports and control pins) must not exceed IVDD.
3. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
4. Based on characterization data, not tested in production.

TABLE 3.4.2: Output Voltage Characteristics, SN8205/SN8205UFL

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL} (2)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS port(3) I_{IO}=+ 8mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}—0.4		
V_{OL} (2)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL port(3) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		2.4		
V_{OL} (2)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OL} (3)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}—1.3		
V_{OL} (2)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO}= +6 mA 2 V < V_{DD} < 2.7 V		0.4	V
V_{OL} (3)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}—0.4		

1. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (e.g. to drive an LED).
2. The IIO current sunk by the device must always respect the absolute maximum rating specified in Table 3.4.2 and the sum of IIO (I/O ports and control pins) must not exceed IVSS.
3. The IIO current sourced by the device must always respect the absolute maximum rating specified in Table 3.4.2 and the sum of IIO (I/O ports and control pins) must not exceed IVDD.
4. Based on characterization data, not tested in production.

3.5 I²C Interface Characteristics

Unless otherwise specified, the parameters given below are derived from tests performed under ambient temperature, fPCLK1 frequency and VDD supply voltage conditions. The SN8200/8200UFL and SN8205/8205UFL performance line I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins to which SDA and SCL are mapped are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDD is disabled, but is still present. The I²C characteristics are described in Table 3.5.1 and Table 3.5.2.

TABLE 3.5.1: I²C Characteristics SN8200/8200UFL

Symbol	Parameter	Standard mode		Fast mode I2C(1)		Unit
		M	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0(3)	-	0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	20 + 0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. Guaranteed by design, not tested in production.
2. fPCLK1 must be at least 2 MHz to achieve standard mode I²C frequencies. It must be at least 4 MHz to achieve the fast mode I²C frequencies and it must be a multiple of 10 MHz in order to reach the I²C fast mode maximum clock speed of 400 kHz.
3. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

TABLE 3.5.2: I²C Characteristics SN8205/8205UFL

Symbol	Parameter	Standard mode		Fast mode I2C(1		Unit
		M	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	-	0	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	20 + 0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I2C frequencies. It must be at least 4 MHz to achieve fast mode I2C frequencies, and a multiple of 10 MHz to reach the 400 kHz maximum I2C fast mode clock.
3. The maximum Data hold time has only to be met if the interface does not stretch the low period of the SCL signal.

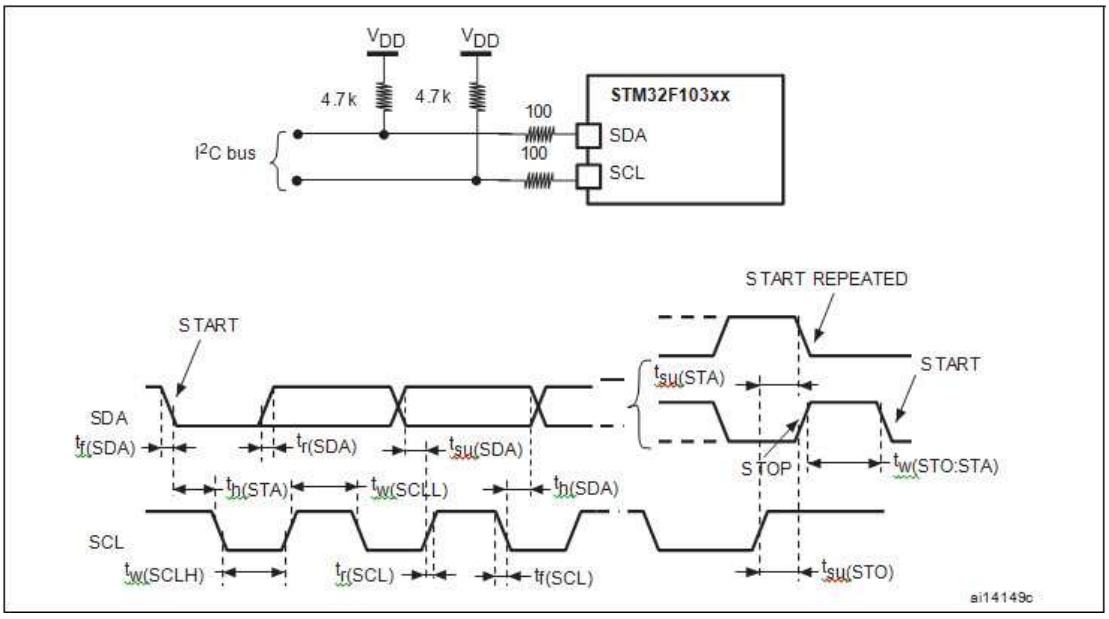


FIGURE 3.1: SN8200/8200UFL I²C bus AC Waveforms and Measurement Circuit

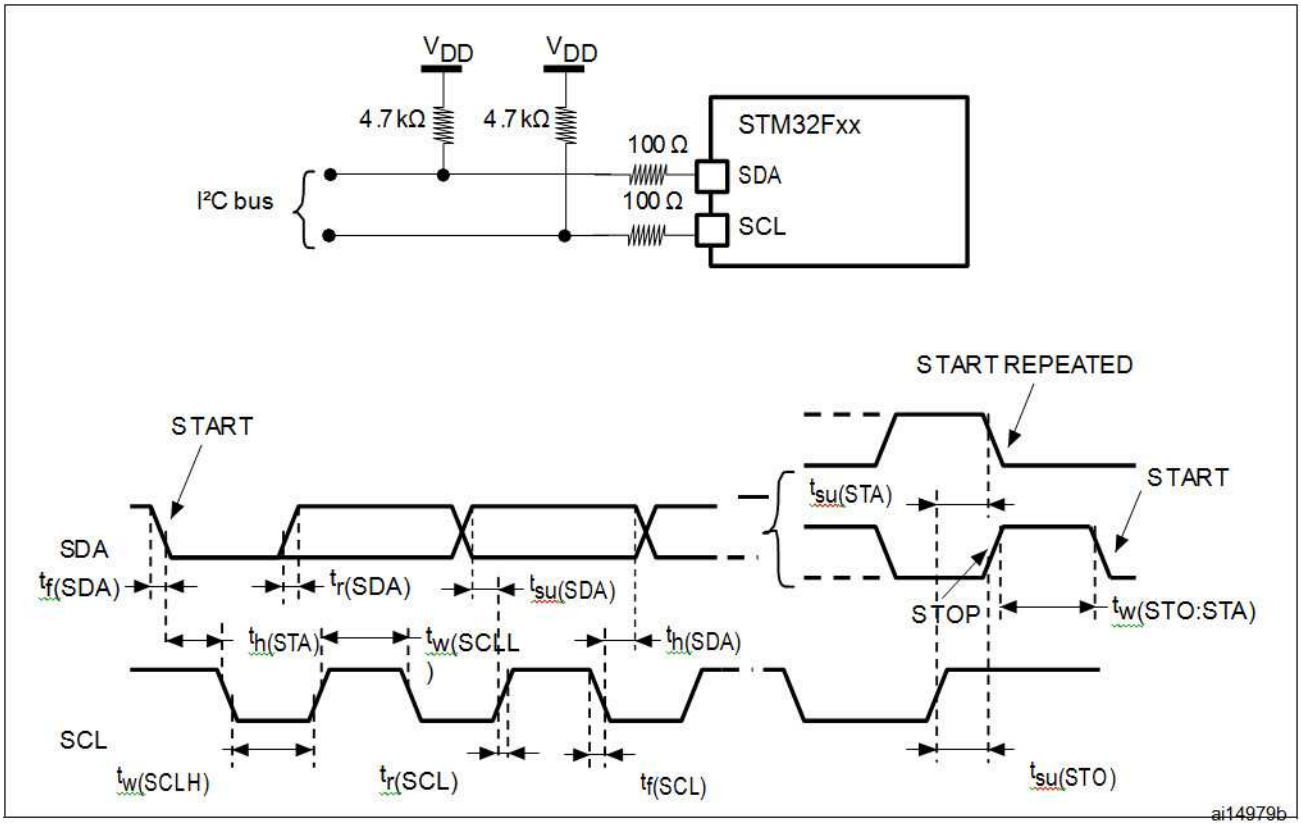


FIGURE 3.2: SN8205/8205UFL I^{2}C bus AC Waveforms and Measurement Circuit

TABLE 3.5.3: SCL Frequency (f_{PCLK1}= 36 MHz., V_{DD} = 3.3 V)[1][2] SN8200/8200UFL

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R_P = External pull-up resistance, f_{SCL} = I$_2$C speed.
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed is ±2%. These variations depend on the accuracy of the external components used to design the application.

TABLE 3.5.4: SCL Frequency (^{f}PCLK1= 30 MHz., V_{DD} = 3.3 V)(1)(2) SN8205/8205UFL

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x8019
300	0x8021
200	0x8032
100	0x0096
50	0x012C
20	0x02EE

1. R_P = External pull-up resistance, f_{SCL} = I2C speed.
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed is ±2%. These variations depend on the accuracy of the external components used to design the application.

3.6 I^{2}S SPI Characteristics

The I2S interface is multiplexed with SPI and can operate in master or slave mode. Unless otherwise specified, the parameters below for I2S derive from tests performed under ambient temperature, ^{f}PCLKx frequency and V_{DD} supply voltage conditions.

TABLE 3.6.1: SPI Characteristics SN8200/8200UFL

Symbol	Parameter	Conditions	Min	Max	Uni
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	8	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$(1)	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$(1)	NSS hold time	Slave mode	$2t_{PCLK}$	-	
$t_{w(SCLH)}$(1) $t_{w(SCLL)}$(1)	SCK high and low time	Master mode, f_{PCLK} =36MHz, presc = 4	50	60	
$t_{su(MI)}$(1)	Data input setup time	Master mode	5	-	
$t_{su(SI)}$(2)		Slave mode	5	-	
$t_{h(MI)}$(1)	Data input hold time	Master mode	5	-	
$t_{h(SI)}$(1)		Slave mode	4	-	
$t_{a(SO)}$(1)(3)	Data output access	Slave mode, f_{PCLK} = 20 MHz	0	$3t_{PCLK}$	
$t_{dis(SO)}$(1)(2)	Data output disable	Slave mode	2	10	
$t_{v(SO)}$(1)	Data output valid time	Slave mode (after enable edge)	-	25	
$t_{v(MO)}$(1)	Data output valid time	Master mode (after enable edge)	-	5	
$t_{h(SO)}$(1)	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{h(MO)}$(1)		Master mode (after enable edge)	2	-	

1. Based on characterization, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

TABLE 3.6.2: SPI Characteristics SN8205/8205UFL

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	SPI1 master/slave mode	-	30	MHz
		SPI2/SPI3 master/slave mode	-	15	
$t_{r(SCL)}$ $t_{f(SCL)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF, f_{PCLK} = 30 MHz	-	8	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$(1)	NSS setup time	Slave mode	4tPCLK	-	ns
$t_{h(NSS)}$(1)	NSS hold time	Slave mode	2tPCLK	-	
$t_{w(SCLH)}$(1)	SCK high and low time	Master mode, $f_{PCLK=3-MHz}$ presc = 2	t_{PCLK}-3	t_{PCLK}+3	
$t_{su(MI)}$ (1)	Data input setup time	Master mode	5	-	
		Slave mode	5	-	
$t_{h(MI)}$ (1)	Data input hold time	Master mode	5	-	
		Slave mode	4	-	
$t_{a(so)}$(1)(2)	Data output access time	Slave mode, f_{PCLK} = 30 MHz	0	$3t_{PCLK}$	
$t_{dis(SO)}$(1)(3)	Data output disable time	Slave mode	2	10	
$t_{v(SO)}$(1)	Data output valid time	Slave mode (after enable edge)	-	25	
$t_{v(MO)}$(1)	Data output valid time	Master mode (after enable edge)	-	5	
$t_{h(SO)}$(1)	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{(MO)}$(1)		Master mode (after enable edge)	2	-	

1. Based on characterization, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

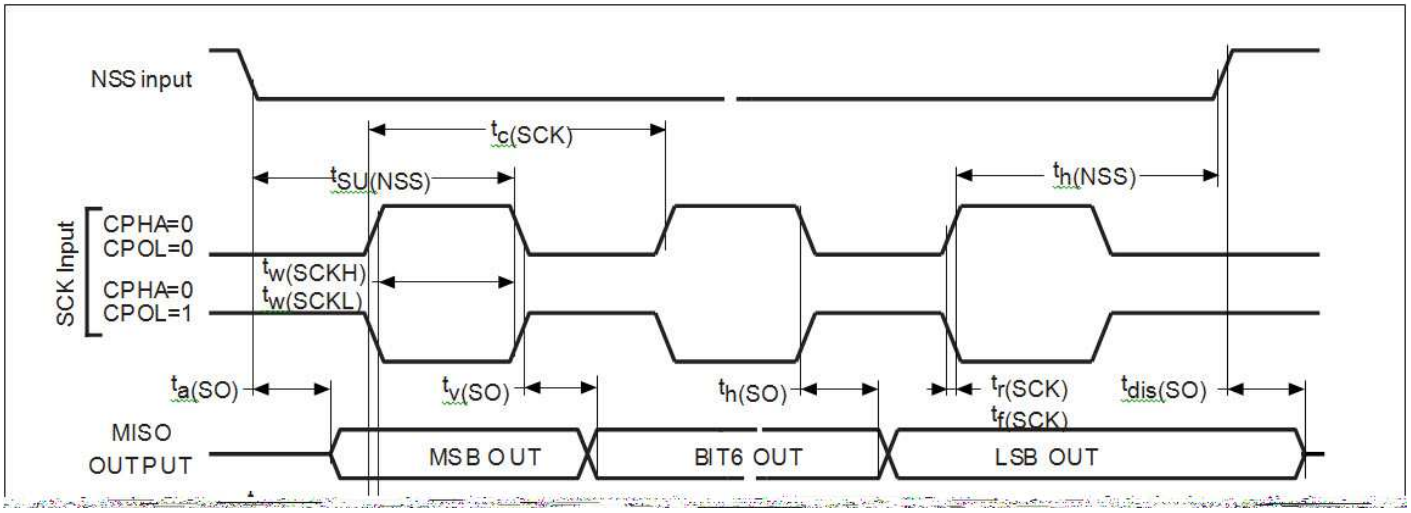


FIGURE 3.3: SPI Timing Diagram - Slave Mode and CPHA = 0, SN8200/8200UFL and SN8205/8205UFL

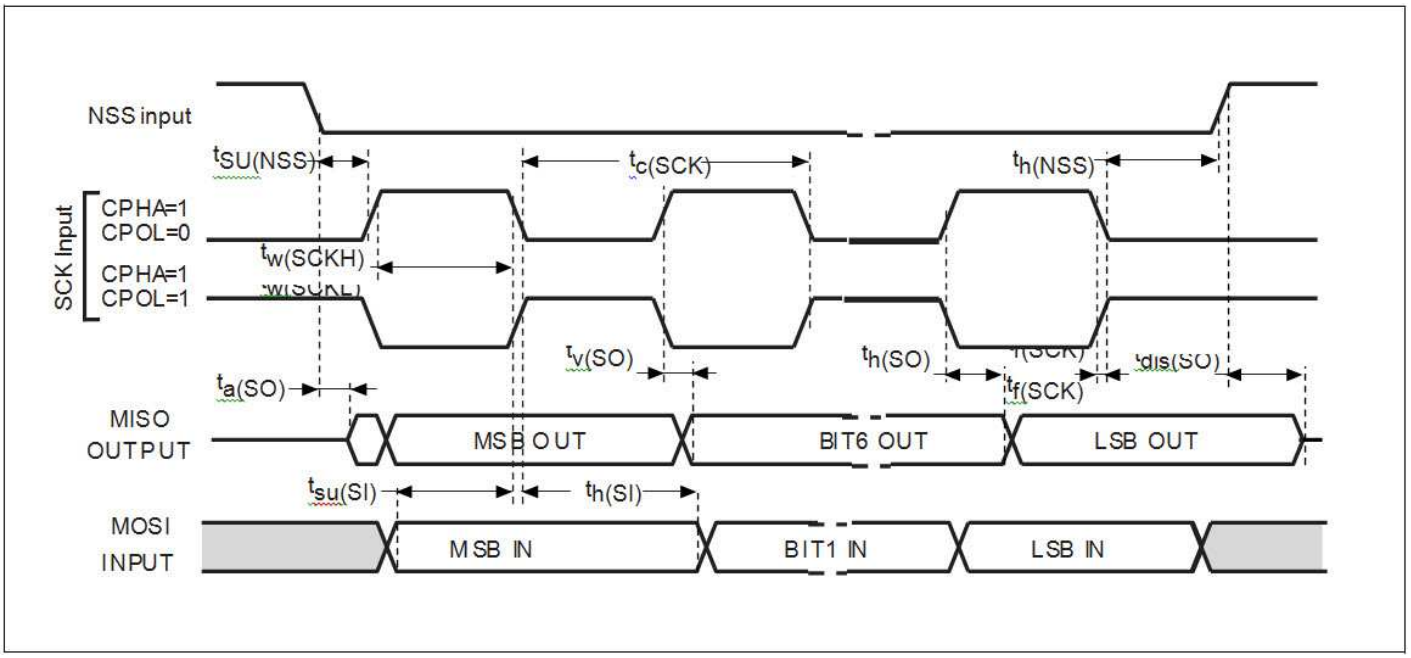


FIGURE 3.4: SPI Timing Diagram - Slave Mode and CPHA = 1[(1)]SPI Timing Diagram - Slave Mode and CPHA = 0, SN8200/8200UFL and SN8205/8205UFL

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7\ V_{DD}$.

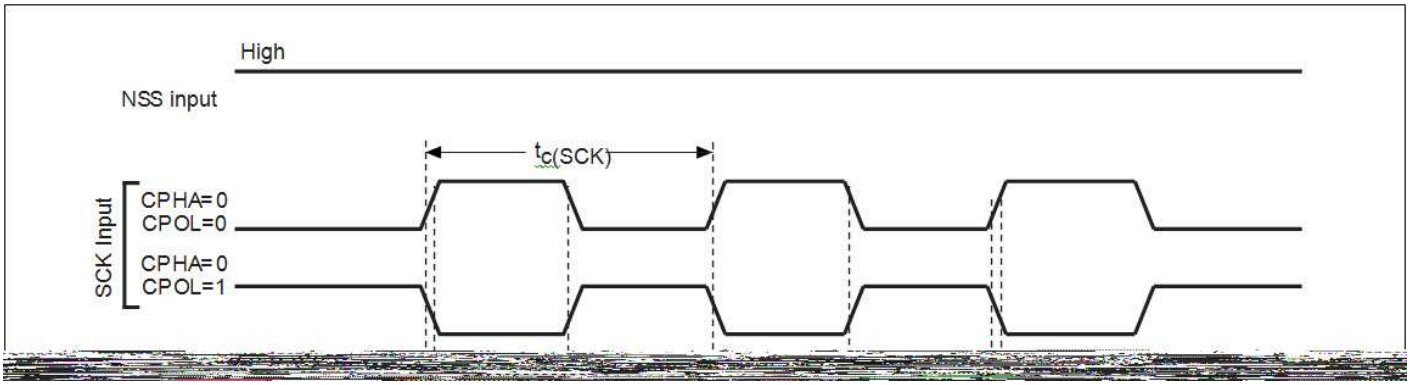


FIGURE 3.5: SPI Timing Diagram - Master Mode SN8200/8200UFL and SN8205/8205UFL

Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

3.7 12-Bit ADC Characteristics

Unless otherwise specified, the parameters given below are preliminary values derived from tests performed under ambient temperature, fPCLK2 frequency and VDDA supply voltage conditions.

NOTE: It is recommended to perform a calibration after each power-up.

TABLE 3.7.1: ADC Characteristics, SN8200/8200UFL

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply		2.4	-	3.6	V
V_{REF+}	Positive reference voltage		2.4	-	VDDA	V
I_{VREF}	Current on the VREF input pin		-	160	220(1)	µA
f_{ADC}	ADC clock frequency		0.6	-	14	MHz
f_S(2)	Sampling rate		0.05	-	1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
			-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)		0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See Equation 1 for details	-	-	50	kΩ

TABLE 3.7.1: ADC Characteristics, SN8200/8200UFL

R_{ADC}(2)	Sampling switch resistance		-	-	1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor		-	-	8	pF
t_{CAL}	Calibration time	f_{ADC} = 14 MHz	5.9			µs
			83			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.214	µs
			-	-	3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.143	µs
			-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
			1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time		0	0	1	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1		18	µs
			14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified above.

Equation 1 (SN8200/8200UFL): R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

TABLE 3.7.2: R_{AIN} max for f_{ADC} = 14 MHz(1), SN8200/8200UFL

T_S (cycles)	ts (µs)	R_{AIN} max (kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

1. Guaranteed by design, not tested in production.

TABLE 3.7.3: ADC accuracy, SN8200/8200UFL - limited test conditions(1)(2)

Symbol	Parameter	Test conditions	Typ	Max(3)	Unit
E	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3 V to 3.6 V T_A = 25 °C Measurements made after	±1.	±2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.	±1.5	
ED	Differential linearity error		±0.	±1	
EL	Integral linearity error		±0.	±1.5	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non- robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
3. Based on characterization, not tested in production.