Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

SPI EXCHANGE 4 x SPI-3 TO SPI-4
Issue 1.0

IDT88P8344

FEATURES

- **Functionality**
  - *Low speed to high speed SPI exchange device*
  - *Logical port (LP) mapping (SPI-3 <-> SPI-4) tables per direction*
  - *Per LP configurable memory allocation*
  - *Maskable interrupts for fatal errors*
  - *Fragment and burst length configurable per interface: min 16 bytes, max 256 bytes*
- **Standard Interfaces**
  - *Four OIF SPI-3: 8 or 32 bit, 19.44-133 MHz, 256 address range, 64 concurrently active LPs per interface*
  - *One OIF SPI-4 phase 2: 80 - 400 MHz, 256 address range, 256 concurrently active LPs*
  - *SPI-4 FIFO status channel options:*
    - *LVDS full-rate*
    - *LVTTL eighth-rate*
  - *Compatible with Network Processor Streaming Interface (NPSI) NPE-Framer mode of operation*
  - *SPI-4 ingress LVDS automatic bit alignment and lane de-skew over the entire frequency range*
  - *SPI-4 egress LVDS programmable lane pre-skew 0.1 to 0.3 cycle*
  - *IEEE 1149.1 JTAG*
  - *Serial or parallel microprocessor interface for control and monitoring*
- **Full Suite of Performance Monitoring Counters**
  - *Number of packets*
  - *Number of fragments*
  - *Number of errors*
  - *Number of bytes*
- **Green parts available, see ordering information**

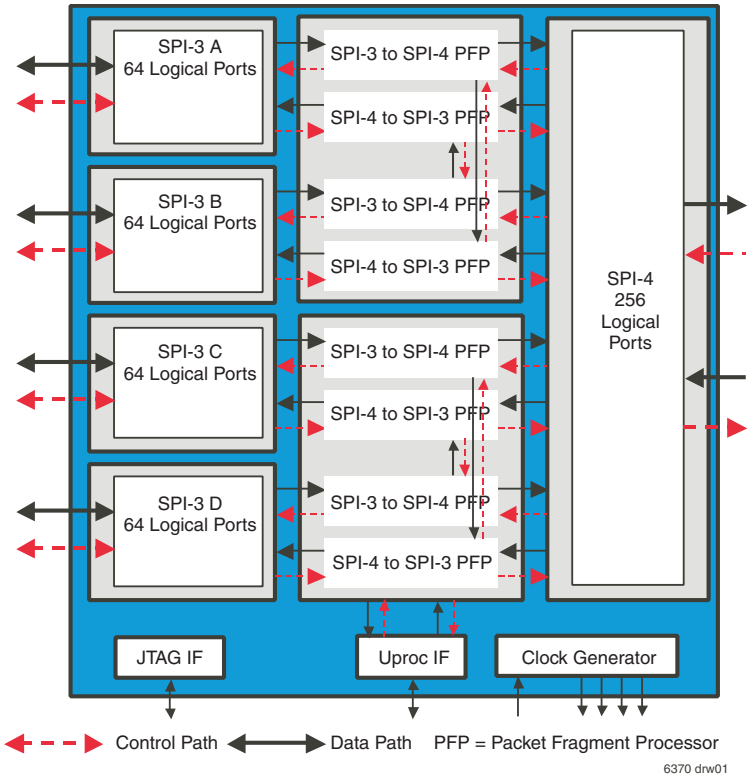
APPLICATIONS

- **Ethernet transport**
- **SONET / SDH packet transport line cards**
- **Broadband aggregation**
- **Multi-service switches**
- **IP services equipment**

DESCRIPTION

The IDT88P8344 is a SPI (System Packet Interface) Exchange with four SPI-3 interfaces and one SPI-4 interface. The data that enter on the low speed interface (SPI-3) are mapped to logical identifiers (LIDs) and enqueued for transmission over the high speed interface (SPI-4). The data that enter on the high speed interface (SPI-4) are mapped to logical identifiers (LIDs) and enqueued for transmission over a low speed interface (SPI-3). A data flow between SPI-3 and SPI-4 interfaces is accomplished with LID maps. The logical port addresses and number of entries in the LID maps may be dynamically configured. Various parameters of a data flow may be configured by the user such as buffer memory size and watermarks. In a typical application, the IDT88P8344 enables connection of multiple SPI-3 devices to a SPI-4 network processor. In other applications SPI-3 or SPI-4 devices may be connected to multiple SPI-3 network processors or traffic managers.

HIGH LEVEL FUNCTIONAL BLOCK DIAGRAM



6370 drw01

Table of Contents

Table of Contents (Continued)

List of Figures

List of Tables

List of Tables (Continued)

List of Tables (Continued)

TYPICAL APPLICATION

Exchange between secure traffic, clear traffic, 10G NPU and co-processor

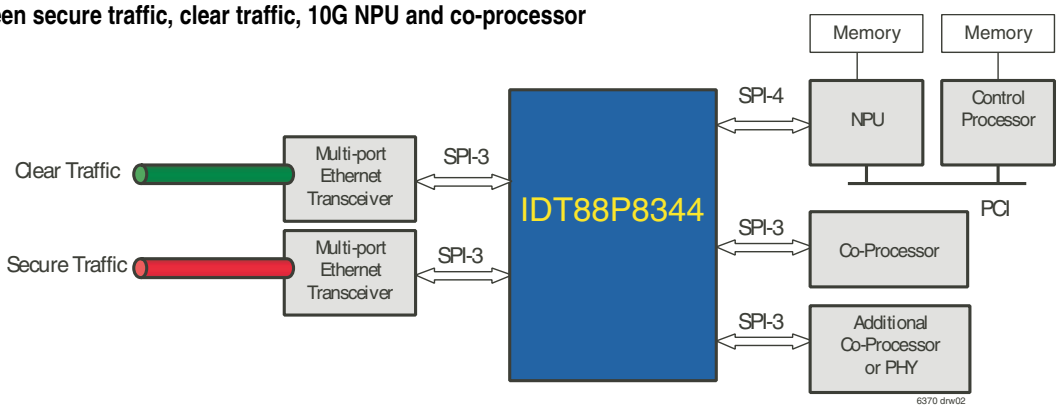


Figure 1. Typical application: NPU, PHY, and co-processor

1. INTRODUCTION

The IDT88P8344 device is a quad SPI-3 to single SPI-4 exchange with switching capabilities intended for use in VPN firewall cards, Ethernet transport, and multi-service switches. The SPI-3 and SPI-4 interfaces are defined by the Optical Internetworking Forum (OIF).

The device can be used as an exchange, a switch, or an aggregation device between network processor units, multi-gigabit framers and PHYs, and switch fabric interface devices.

Data Path Overview

Figure 2. *Data Path Diagram* shows an overview of the data path through the device.

In normal operation, there are two paths through the IDT88P8344 device: the quad SPI-3 ingress to SPI-4 egress path, and the SPI-4 ingress to quad SPI-3 egress path. SPI-3 and SPI-4 burst sizes are separately configurable.

In the SPI-3 ingress to SPI-4 egress path, data enter in fragments on the SPI-3 interface and are received by the SPI-3 interface block. The fragments are mapped to a SPI-4 address and stored in memory allocated at the SPI-3 level until such a time that the SPI-3 to SPI-4 packet fragment processor determines that they are to be transmitted on the SPI-4 interface. The data is transferred in bursts, in line with the OIF SPI-4 implementation agreement, to the SPI-4 interface block, and are transmitted on the SPI-4 interface.

In the SPI-4 ingress to SPI-3 egress path, data enter in bursts on the SPI-4 interface and are received by the SPI-4 interface block. The SPI-4 address is translated to a SPI-3 address, and the data contained in the bursts are stored in memory allocated at the SPI-3 level until such a time that the SPI-4 to SPI-3 packet fragment processor determines that they are to be transmitted on the SPI-3 interface. The data is transferred in packet fragments, in line with the OIF SPI-3 implementation agreement, to the SPI-3 interface block, and are transmitted on the SPI-3 interface.

These and additional data paths are described in more detail in the data path section of this document.

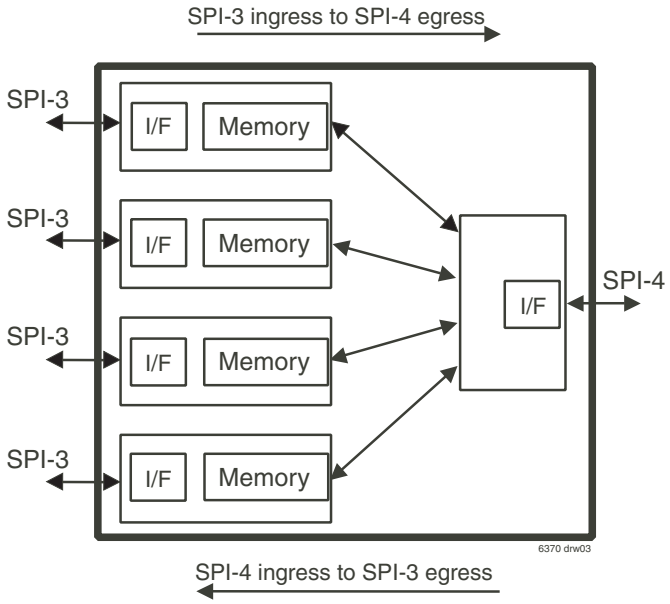


Figure 2. Data path diagram

2. PIN DESCRIPTION

SPI-3 (four instantiations)

For the SPI-3 interfaces, each pin is used differently depending whether the SPI-3 is in Link mode or in PHY mode. Each of the SPI-3 interfaces is separately configurable for either Link or PHY mode. This configuration holds for both the ingress and egress paths. The device pin is given a generic name, and mapped to the standard pin name according to the mode of the interface (Link or PHY).

TABLE 1 – I/O TYPES

I/O type	Function
I_ST	Input with Schmitt trigger with weak pull up
I-PU	Input with weak pull up
B-PU	Bidirectional I/O with weak pull up
I_PD	Input with pull down
I	Input
O	Output
O-Z	Output with tri-state
OD	Output with open drain

TABLE 2 – SPI-3 INGRESS INTERFACE PIN DEFINITION

Generic Name	Specific Name	I/O type	Description	Mode	
				Link	PHY
I_FCLK	SPI3A_I_FCLK SPI3B_I_FCLK SPI3C_I_FCLK SPI3D_I_FCLK	I-ST LVTTL	Ingress SPI-3 write clock	RFCLK	TFCLK
RVAL	SPI3A_I_RVAL SPI3B_I_RVAL SPI3C_I_RVAL SPI3D_I_RVAL	B-PU LVTTL	Receive data valid	RVAL (I)	RVAL (O)
I_ENB	SPI3A_I_ENB SPI3B_I_ENB SPI3C_I_ENB SPI3D_I_ENB	B-PU LVTTL	Ingress read enable	RENB (O)	TENB (I)
I_DAT[31:0]	SPI3A_I_DAT[31:0] SPI3B_I_DAT[31:0] SPI3C_I_DAT[31:0] SPI3D_I_DAT[31:0]	I-PU LVTTL	Ingress data bus	RDAT [31:0]	TDAT [31:0]
I_MOD[1:0]	SPI3A_I_MOD[1:0] SPI3B_I_MOD[1:0] SPI3C_I_MOD[1:0] SPI3D_I_MOD[1:0]	I-PU LVTTL	Ingress word modulus	RMOD [1:0]	TMOD [1:0]
I_PRTY	SPI3A_I_PRTY SPI3B_I_PRTY SPI3C_I_PRTY SPI3D_I_PRTY	I-PU LVTTL	Ingress parity	RPRTY	TPRTY
I_SOP	SPI3A_I_SOP SPI3B_I_SOP SPI3C_I_SOP SPI3D_I_SOP	I-PU LVTTL	Ingress start of packet	RSOP	TSOP
I_EOP	SPI3A_I_EOP SPI3B_I_EOP SPI3C_I_EOP SPI3D_I_EOP	I-PU LVTTL	Ingress end of packet	REOP	TEOP
I_ERR	SPI3A_I_ERR SPI3B_I_ERR SPI3C_I_ERR SPI3D_I_ERR	I-PU LVTTL	Ingress EOP error	RERR	TERR
I_SX	SPI3A_I_SX SPI3B_I_SX SPI3C_I_SX SPI3D_I_SX	I-PU LVTTL	Ingress start of transfer	RSX	TSX

TABLE 3 – SPI-3 EGRESS INTERFACE PIN DEFINITION

Generic Name	Specific Name	I/O type	Description	Mode	
				Link	PHY
E_FCLK	SPI3A_E_FCLK SPI3B_E_FCLK SPI3C_E_FCLK SPI3D_E_FCLK	I-ST LVTTL	Egress SPI-3 write clock	TFCLK	RFCLK
E_ENB	SPI3A_E_ENB SPI3B_E_ENB SPI3C_E_ENB SPI3D_E_ENB	B-PU LVTTL	Egress read enable	TENB (O)	RENB (I)
E_DAT[31:0]	SPI3A_E_DAT[31:0] SPI3B_E_DAT[31:0] SPI3C_E_DAT[31:0] SPI3D_E_DAT[31:0]	O-Z LVTTL	Egress data bus	TDAT [31:0]	RDAT [31:0]
E_MOD[1:0]	SPI3A_E_MOD[1:0] SPI3B_E_MOD[1:0] SPI3C_E_MOD[1:0] SPI3D_E_MOD[1:0]	O-Z LVTTL	Egress word modulus	TMOD [1:0]	RMOD [1:0]
E_PRTY	SPI3A_E_PRTY SPI3B_E_PRTY SPI3C_E_PRTY SPI3D_E_PRTY	O-Z LVTTL	Egress parity	TPRTY	RPRTY
E_SOP	SPI3A_E_SOP SPI3B_E_SOP SPI3C_E_SOP SPI3D_E_SOP	O-Z LVTTL	Egress start of packet	TSOP	RSOP
E_EOP	SPI3A_E_EOP SPI3B_E_EOP SPI3C_E_EOP SPI3D_E_EOP	O-Z LVTTL	Egress end of packet	TEOP	REOP
E_ERR	SPI3A_E_ERR SPI3B_E_ERR SPI3C_E_ERR SPI3D_E_ERR	O-Z LVTTL	Egress EOP error	TERR	RERR
E_SX	SPI3A_E_SX SPI3B_E_SX SPI3C_E_SX SPI3D_E_SX	O-Z LVTTL	Egress start of transfer	TSX	RSX

TABLE 4 – SPI-3 STATUS INTERFACE PIN DEFINITION

Generic Name	Specific Name	I/O type	Description	Mode	
				Link	PHY
DTPA[3:0]	SPI3A_DTPA[3:0] SPI3B_DTPA[3:0] SPI3C_DTPA[3:0] SPI3D_DTPA[3:0]	B-PU LVTTL	Direct transmit packet available	DTPA (I)	DTPA (O)
STPA	SPI3A_STPA SPI3B_STPA SPI3C_STPA SPI3D_STPA	B-PU LVTTL	Selected-PHY transmit packet available	STPA (I)	STPA (O)
PTPA	SPI3A_PTPA SPI3B_PTPA SPI3C_PTPA SPI3D_PTPA	B-PU LVTTL	Polled-PHY transmit packet available	PTPA (I)	PTPA (O)
ADR[7:0]	SPI3A_ADR[7:0] SPI3B_ADR[7:0] SPI3C_ADR[7:0] SPI3D_ADR[7:0]	B-PU LVTTL	Polled transmit PHY address	ADR (O)	ADR (I)

SPI-4 (one instantiation)

For the SPI-4 interface, each pin is used differently depending whether the SPI-4 is in Link mode or in PHY mode. The pin is given a generic name, shown in the Name column, and mapped to the OIF standard pin name according to the mode of operation of the interface (Link to PHY).

TABLE 5 – SPI-4 INGRESS INTERFACE DEFINITION

Generic Name	Specific Name	I/O type	Description	Mode	
				Link	PHY
I_DCLK (P & N)	SPI4_I_DCLK_P SPI4_I_DCLK_N	I LVDS	Ingress data clock	RDCLK	TDCLK
I_DAT[15:0] (P & N)	SPI4_I_DAT_P[15:0] SPI4_I_DAT_N[15:0]	I LVDS	Ingress data bus	RDAT	TDAT
I_CRTL (P & N)	SPI4_I_CTRL_P SPI4_I_CTRL_N	I LVDS	Ingress control word	RCTL	TCTL
I_SCLK_L (P & N)	SPI4_I_SCLK_P SPI4_I_SCLK_N	O LVDS	Ingress status clock	RSCLK	TSCLK
I_STAT_L[1:0] (P & N)	SPI4_I_STAT_P[1:0] SPI4_I_STAT_N[1:0]	O LVDS	Ingress status info	RSTAT	TSTAT
I_SCLK_T	SPI4_I_SCLK_T	O LVTTL	Ingress status clock	RSCLK	TSCLK
I_STAT_T[1:0]	SPI4_I_STAT_T[1:0]	O LVTTL	Ingress status info	RSTAT	TSTAT
BIAS	BIAS	Analog	Use an external 3K Ohm 1% resistor to VSS	----------	----------
LVDS_STA	LVDS_STA	I-PU	LVDS(high)/LVTTL (low) status selection (See Note below)	----------	----------

NOTE:
1. A hardware reset or software reset must be performed after changing the level of this pin.

TABLE 6 – SPI-4 EGRESS INTERFACE DEFINITION

Generic Name	Specific Name	I/O type	Description	Mode	
				Link	PHY
E_DCLK (P & N)	SPI4_E_DCLK_P SPI4_E_DCLK_N	O LVDS	Egress data clock	TDCLK	RDCLK
E_DAT[15:0] (P & N)	SPI4_E_DAT_P[15:0] SPI4_E_DAT_N[15:0]	O LVDS	Egress data bus	TDAT[15:0]	RDAT[15:0]
E_CRTL (P & N)	SPI4_E_CTRL_P SPI4_E_CTRL_N	O LVDS	Egress control word	TCTL	RCTL
E_SCLK_L (P & N)	SPI4_E_SCLK_P SPI4_E_SCLK_N	I LVDS	Egress status clock	TSCLK	RSCLK
E_STAT_L[1:0] (P & N)	SPI4_E_STAT_P[1:0] SPI4_E_STAT_N[1:0]	I LVDS	Egress status info	TSTAT[1:0]	RSTAT[1:0]
E_SCLK_T	SPI4_E_SCLK_T	I-ST LVTTL	Egress status clock	TSCLK	RSCLK
E_STAT_T[1:0]	SPI4_E_STAT_T[1:0]	I-PU LVTTL	Egress status info	TSTAT	RSTAT[1:0]

Parallel microprocessor Interface

The Parallel microprocessor interface is configurable to work in Intel or Motorola modes. Be sure to connect SPI_EN to a logic low when using the parallel microprocessor interface mode.

TABLE 7 – PARALLEL MICROPROCESSOR INTERFACE

Name	I/O type	Description
MPM	I-PU CMOS	Microprocessor mode: 0=Motorola Mode, 1=Intel mode (sampled after reset)
CSB	I-ST CMOS	Chip select; active low
RDB	I-ST CMOS	RDB: Read control, active low (in Intel mode), or DSB: Data strobe, active low (in Motorola mode)
WRB	I-ST CMOS	WRB: Write control; active low; (in Intel mode), or R/WB: Read/write control; when high, read is active; when low, write is active; (in Motorola mode)
ADD[5:0]	I-PU CMOS	Address bus
DBUS[7:0]	B-PU CMOS	Data bus
INTB	OD CMOS	Interrupt, active low, open drain
SPI_EN	I-PU CMOS	Logic low selects parallel microprocessor interface (internally pulled up, sampled after reset)

TABLE 8 – SERIAL MICROPROCESSOR INTERFACE (SERIAL PERIPHERAL INTERFACE MODE)

Four pins multiplexed with parallel microprocessor pins. Be sure to connect SPI_EN to a logic high when using the serial microprocessor interface mode.

Name	I/O type	Parallel microprocessor pin used	Serial Peripheral Interface Pin Use Description
SDI	I-ST CMOS	WRB	Serial data in, rise edge sampling
SDO	B-PU CMOS	DBUS[0]	Serial data out, falling edge driving
CSB	I-ST CMOS	CSB	Chip select, active low. SDO is tri-stated when CSB is high
SCLK	I-ST CMOS	RDB	Input clock
INTB	OD CMOS	----------	Interrupt, active low, open drain
SPI_EN	I-PU CMOS	----------	Dedicated input. High selects SPI microprocessor interface (internally pulled up)

TABLE 9 – MISCELLANEOUS

Name	I/O type	Description
REF_CLK	I-ST CMOS	Master clock input
OCLK[3:0]	O LVTTL	Clock outputs that can be used for SPI-3, phase-shifted to avoid simultaneously switching outputs
CLK_SEL[3:0]	I-PU CMOS	Clock select inputs for internal PLL, internal MCLK, and OCLK[3:0] outputs
TIMEBASE	B-PU CMOS	Timeout signal for counters
GPIO[4:0]	B-PU CMOS	General purpose I/O or internal state monitor pins
TDI	I-PU CMOS	JTAG data in (internally pulled up)
TDO	O-Z CMOS	JTAG data out
TCK	I-ST CMOS	JTAG clock
TMS	I-PU CMOS	JTAG mode (internally pulled up)
TRSTB	I-PU CMOS	JTAG reset, active low (internally pulled up). Pull down for normal operation.
RESETB	I-PD CMOS	Master hardware reset, active low

NOTE:

1. Inputs with internal pull-ups do not need external pull-ups unless connected to PCB trace (except TRSTB).

3. EXTERNAL INTERFACES

The external interfaces provided on the IDT88P8344 device are four SPI-3 interfaces, one SPI-4 interface, a serial or parallel microprocessor interface, a JTAG interface, and a set of GPIO pins. Each of the interfaces is defined in the relevant standard.

The following information contains a set of the highlights of the features supported from the relevant standards, and a description of additional features implemented to enhance the usability of these interfaces for the system architect.

3.1 SPI-3

Refer to OIF SPI-3 document (see 13. Glossary for a reference) for full details of the implementation agreement.

- Four instantiations of SPI-3 interface; each interface independently configurable
- Device supports a 8-bit and 32-bit data bus structure.
- Clock rate is minimum 19.44 to maximum 133 MHz
- Link, single port PHY, and single device multi port PHY modes supported
- Byte level and packet level transfer control mechanisms supported
  - Four DTPA signals supported, mapped to LP addresses 0 – 3, for STPA in byte-level mode
  - Eight ADR signals supported for PTPA in packet-level mode
- Address range 0 to 255 with support for 64 simultaneously active logical ports
- Fragment length (section) configurable from 16 to 256 bytes in 16 byte multiples
- Configurable standard and non-standard bit ordering

SPI-3 implementation features

The following are implemented per SPI-3 interface, and there are four instantiations per device.

- Link / PHY layer device
- Packet / byte level FIFO status information
- Physical port enable
- Width of data bus (32 bit or 8 bit)
- Parity selection (odd or even)
- Enable parity check

3.1.1 SPI-3 ingress

The following are implemented per SPI-3 interface, and there are 4 instantiations per device.

- SPI-3 LP to Link Identifier (LID) map
- 256 entries, one per SPI-3 LP address
- LP enable control
- Only 64 of these entries are to be in the active state simultaneously

Backpressure enable

- Link mode only
- Enables the assertion of the I_ENB when at least one active LID can not accept data
- If not enabled, the I_ENB signal will never be asserted in Link mode, possibly leading to fragments being discarded.

Minimum packet length

- Packets shorter than the minimum length will be optionally counted in the short packet counter.
- Range 0 – 255 in 1 byte increments

Maximum packet length

- Packets longer than the maximum length will be optionally counted in the long packet counter.
- Range 0 – 16,383 in 1 byte increments

Backpressure threshold

- Number of free segments allocated below which backpressure will be triggered for the LP

SPI-3 ingress interface

Multiple independent data streams can be transmitted over the physical SPI-3 port. Each of those data streams is identified by a SPI-3 logical port (LP). Data from a transfer on a SPI-3 logical port and the associated descriptor fields are synchronized to the configurable internal buffer segment pool.

Normal operation

Refer to [13. Glossary] for details about the SPI-3 interface.

- A SPI-3 interface (a physical port) is enabled by the SPI-3_ENABLE flag in the SPI-3 configuration register. A disabled interface tri-states all output pins and does not respond to any input signals.
- The interface is configured in PHY or Link layer mode by the LINK flag in the SPI-3 general configuration register.
- The interface supports a SPI-3 logical port number range [0..255], note that at most 64 logical ports can be configured.
- The SPI-3 interface supports data transport over either a 32 bit data interface or over one single 8 bit interface (data[7:0]) only. The selection is defined by the BUSWIDTH flag in the SPI-3 general configuration register.
- The SPI-3 interface is configured in byte mode or packet mode by the PACKET flag in the SPI-3 general configuration register.
- The SPI-3 interface supports over-clocking.
- Parity checking over data[31:0] is enabled by the PARITY_EN flag in the Table 50, SPI-3 general configuration register (register_offset=0x00). The parity type is defined by the EVEN_PARITY flag. Parity check results over the in-band port address and the data of a transfer are forwarded towards the packet fragment processor.
- SPI Exchange supports zero clock interval spacing between transfers.

SPI-3 ingress interface errors

Given an I_FCLK within specification, the SPI-3 will not dead lock due to any combination or sequence on the SPI-3 interface. The SPI Exchange detects for incorrect SOP / EOP sequences on a logical port. The following sequences are detected:

Successive SOP (SOP- SOP sequence rather than SOP –EOP –SOP-EOP)

Successive EOP (EOP- EOP sequence rather than SOP –EOP –SOP-EOP)

Detection of an illegal sequence results in the generation of an SPI-3 illegal SOP sequence event or SPI-3 illegal EOP sequence even generated. The event is associated to the physical port. The event is directed towards the PMON & DIAG module.

A clock available process detects a positive I_FCLK within a 64 MCLK clock cycle period. The result of this process is reported in the I_FCLK_AV flag in the Table 52 SPI-3 ingress fill level register (Block_base 0x0200 + Register_offset 0x02).

A status change from the clock available status to the clock not available status generates a maskable SPI-3 ingress clock unavailable interrupt indication, SPI3_ICLK_UN, in Table 62-Non LID associated interrupt indication register (Block_Base 0x0C00 + Register_offset 0x0C).

SPI-3 ingress Link mode

Refer to [Glossary] for details about the SPI-3 interface.

- The PHY pushes data into the device in blocks from 1 up to 256 bytes.
- The SPI Exchange provides backpressure for the SPI-3 ingress physical interface by the I_ENB signal. The I_ENB is asserted when at least one active LID can not accept data. This feature is enabled by the BACKPRESSURE_EN flag in the SPI-3 ingress configuration register (register_offset = 0x01). When the flag is cleared the I_ENB signal will not be asserted, hence no backpressure can be generated.

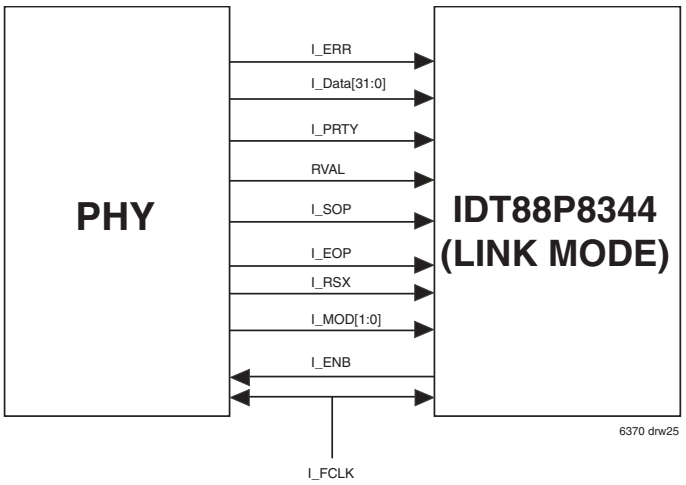


Figure 3. Link mode SPI-3 ingress interface

SPI-3 ingress PHY mode

The SPI Exchange indicates to the Link layer it has buffer space available by proper response to either Link layer polling (packet mode) or direct indication on DTPA signals (byte mode). The selection is made by the PACKET flag in the SPI-3 configuration register.

- In packet mode the device responds to polling (by Link layer device)
- In byte mode the direct status indication is limited to 4 addresses (fixed ports [3:0])

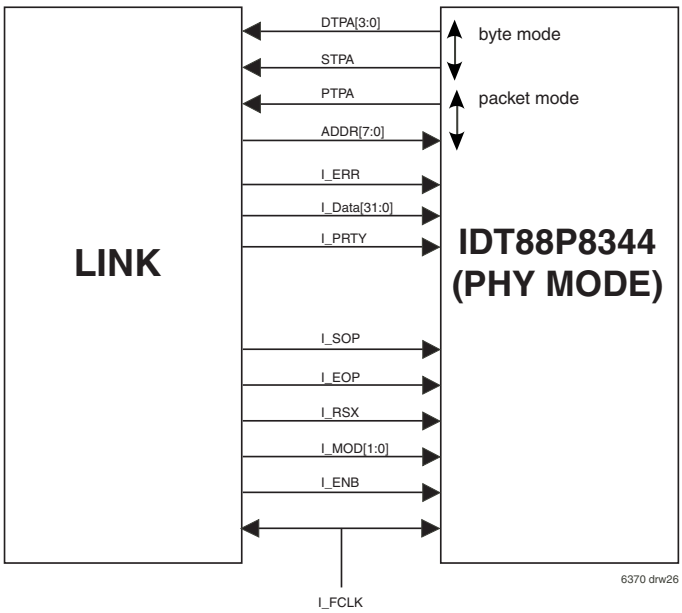


Figure 4. PHY mode SPI-3 ingress interface

3.1.2 SPI-3 egress

- All fragments will be of a programmable equal length with the exception of EOP fragment which may be shorter

LID to LP map

- 64 entries, one per LID, for each SPI-3 egress port
- LP enable control

Multiple burst enable

- Allows more than one burst to be sent to an LP.

Poll length

- For use when in Link mode and when using the packet level mode
- Causes polling of the PHY for the logical ports associated to LIDs ranging from [0 up to POLL_LENGTH] to find logical ports that can accept data
- Range is 0-63

Loopback enable

- Enables loopback from SPI-3 physical interface to same SPI-3 physical interface for test purposes

Data memory egress control

The SPI-3 egress port descriptor table (block_base 0x1700) for both paths out of the data memory. The function of the SPI-3 egress port descriptor table (block_base 0x1700) is to define where data goes after exiting the main data memory. There are four options configurable:

- SPI-3
- SPI-4
- Capture
- Discard

Maximum number of memory segments

- Defines the largest BUFFER available to a LP / LID
- Each segment is 256 bytes
- Range 1 – 508 in increments of one segment

SPI-3 egress interface configuration

- SPI Exchange allows for a pause at least two cycles of E_FCLK between successive transfers.
- SPI Exchange allows for over clocking for a higher clock frequency supported as opposed to the one defined by the SPI-3 implementation agreement.
- The Link mode is selected by the Link flag in the SPI-3 general configuration register.
- The interface operates in PACKET mode or BYTE mode as defined by the PACKET flag in the SPI-3 general configuration register.
- SPI Exchange generates even or odd parity over E_DATA[7/31:0] on the E_PRTY signal as defined by the EVEN flag in the Table 50, SPI-3 general configuration register (register_offset=0x00).
- SPI Exchange optionally generates two dummy cycles after assertion of the STX signal. The option is enabled by the STX_SPACING flag in the Table 50, SPI-3 general configuration register (register_offset=0x00).
- SPI Exchange optionally generates two dummy cycles after assertion of an EOP signal. The option is enabled by the EOP_SPACING flag in the Table 50, SPI-3 general configuration register (register_offset=0x00).

SPI-3 egress interface errors

A clock available process detects an E_FCLK cycle within a 64 MCLK clock cycle period. The result of this process is reported in the E_FCLK_AV flag in Table 58, *SPI-3 egress fill level register (Block_base 0x0700 + Register_offset=0x03)*.

A status change from the clock available status to the clock not available status generates a maskable SPI-3 egress clock unavailable interrupt indication, SPI3_ECLK_UN, in Table 62-Non LID associated interrupt indication register (Block_Base 0x0C00 + Register_offset 0x0C).

SPI-3 egress Link mode

The SPI Exchange receives status information from the PHY. The PHY indicates its ability to receive data. Status information for all logical ports is directed towards the packet fragment processor.

Status information is received from the PHY.

- In packet mode, the SPI Exchange polls the PHY for the logical ports associated to LIDs ranging from 0 up to POLL_LENGTH to find logical ports that can accept data. The POLL_LENGTH field is defined in the SPI-3 egress configuration register.
- In byte mode the SPI Exchange allows for direct status detection.

This status information is directly forwarded to the packet fragment processor if enabled by the BURST_EN flag. When the BURST_EN flag is cleared the only one packet fragment per LP is allowed into the SPI-3 egress buffers.

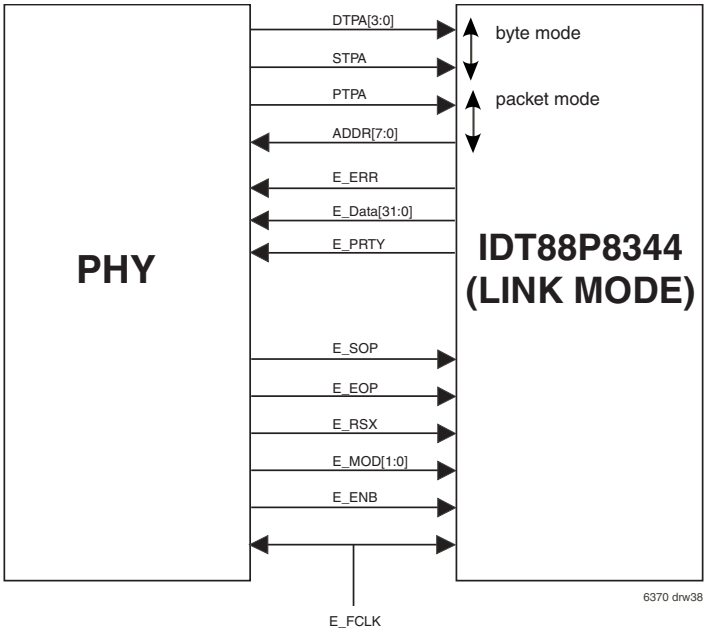


Figure 5. Link mode SPI-3 egress interface

SPI-3 egress PHY mode

In PHY mode, the SPI Exchange sends data to the attached Link-mode device as long as the E_ENB signal is asserted. The SPI-3 packet fragment processor transfers data to the SPI-3 egress buffers.

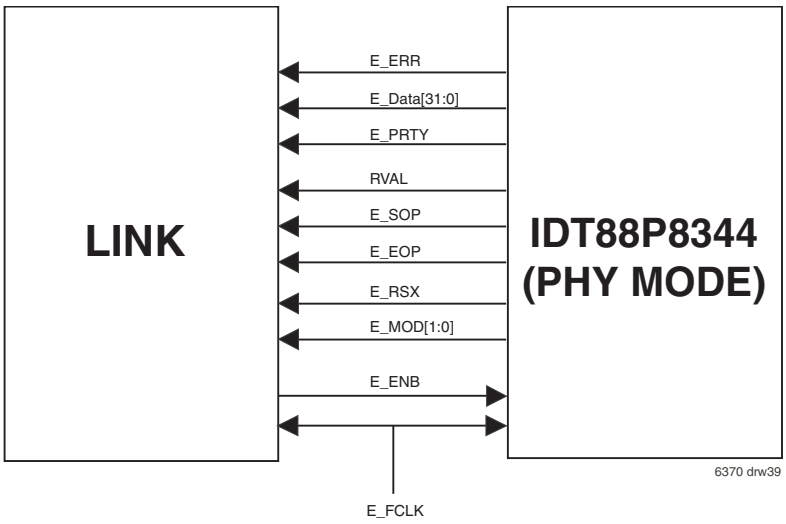


Figure 6. PHY mode SPI-3 egress interface

3.2 SPI-4

Refer to OIF SPI-4 document (see Glossary) for full details of the implementation agreement.

- Clock rate is 80 - 400 MHz (160 - 800MHz DDR)
- Link and PHY modes supported
- Address range 0 to 255 with support for 256 simultaneously active logical ports
- MAXBURST parameters configurable 16-256 bytes in 16 byte multiples
- 256 entry calendar
- LVTTL and LVDS status signals supported

The following are implemented for the SPI-4 interface:

- Link / PHY layer device
- Physical port active

3.2.1 SPI-4 ingress

The SPI-4 ingress includes

- Bit alignment
- Word alignment/ de-skew
- Transfer decode and dispatch
- PFP interface
- Status frame generation

SPI-4 ingress configurable parameters

SPI-4 LID map

- 256 entries, one per SPI-4 LP
- SPI-3 physical interface identifier
- Physical port enable

Word / bit synchronization

- LVDS clock data alignment and LVDS data de-skew

Minimum packet length

- Packets shorter than the minimum length will be optionally counted in the short packet counter.
- Range 0 – 255 in 1 byte increments

Maximum packet length

- Packets longer than the maximum length will be optionally counted in the long packet counter.
- Range 0 – 16,383 in 1 byte increments

Free segment backpressure threshold

- Number of free buffer segments allocated to trigger backpressure for the LP

Data sampling

The I_LOW field in the Table 89 SPI-4 ingress configuration register (Block_base 0x0300 + Register_offset 0x00) selects an operating mode between 80 MHz and 200 MHz or between 200 MHz and 400 MHz.

Each lane is over-sampled by a factor of five. The over-sampled data is generated by a locked tapped delay line and clocked in to a register at the clock rate. The current samples c(n) and the previously generated samples provide samples for the eye computation. The optimized sampling point will be selected based on the eye computation. The tap selector is updated if necessary at the end of the eye pattern measurement interval. The tap selector moves no more than one tap at a time as a result of the eye pattern measurement.

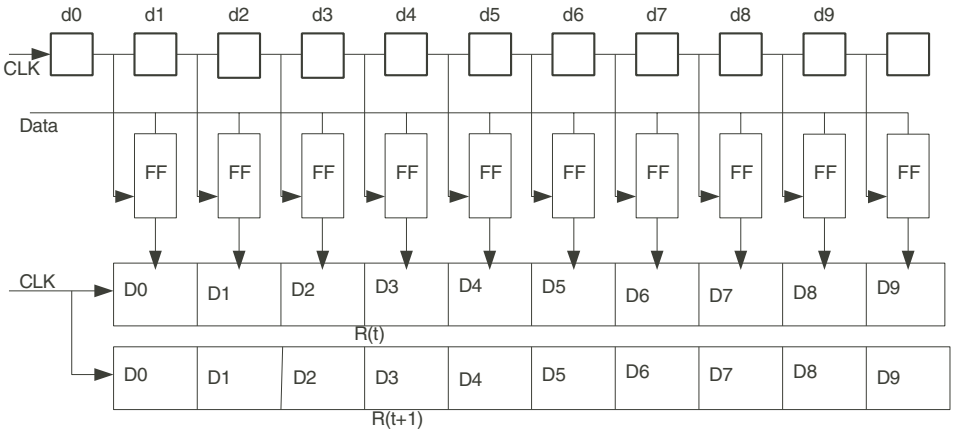


Figure 7. Data sampling diagram

Eye measurement

C[0]= Rt.D2^Rt.D3
C[1]= Rt.D3^Rt.D4
.....
C[7]= Rt.D9^Rt+1.D0
C[8]= Rt+1.D0^Rt+1.D1
C[9]= Rt+1.D1^Rt+1.D2

Accumulation results during a window defined by W are stored in the diagnostics table.

The latest result can be read out for diagnostic purposes.

Output tap selection

The sampling tap is automatically selected based on the eye measurement.

Manual phase selection

The automatic phase adjustment can be overruled by the processor when the FORCE flag is set see Table 99, SPI-4 ingress bit alignment control register (register_offset 0x11). The PHASE_ASSIGN field see Table 113, SPI-4 ingress manual alignment phase/result register (0x0C to 0x1F) now defines the selected phase.

Word alignment

The de-skew block searches for the Training Control Word 0x0FFF. If the Training Control Word is found, then training data is expected to follow the Training Control Word. The orthogonal training data will be used to align the word.

A de-skew control bit (I_DSC in Table 89-SPI-4 ingress configuration register at Block_base 0x0300 + Register_offset 0x00) is used to protect against a random data error during de-skew. If I_DSC=1, then two consecutive de-skew results are required. It is recommended to set I_DSC to 1.

For diagnostics, an out of range offset between lines is provided. If the offset is more than two bits between the earliest and latest samples, I_DSK_OOR is set to a logic one. I_DSK_OOR is cleared to a logic zero when the offset is in range.

Transfer decode and dispatch

In the *OUT_OF_SYNCH* state, the de-skew block will decode the transfer, and check the DIP-4 for validation.

A number of consecutive error free DIP-4 ingress bursts will lead to a transition to the IN_SYNCH. The number is defined by the I_INSYNC_THR field in Table 89-SPI-4 ingress configuration register (Block_base 0x0300 + Register_offset 0x00).

In the *IN_SYNCH* state, the PFP decodes the status transfer, check the DIP-4, and dispatches the data.

A number of consecutive DIP-4 errors will lead to the OUT_OF_SYNCH state. The number is defined by the I_OUTSYNC_THR field in Table 89-SPI-4 ingress configuration register (Block_base 0x0300 + Register_offset 0x00).

A number of consecutive training patterns will lead to OUT_OF_SYNCH. The number is defined by the STRT_TRAIN field in the Table 100 SPI-4 ingress start up training threshold register (Block_base 0x0300 + Register_offset 0x12). This feature is disabled if STRT_TRAIN=0.

Control word and data

A control word is distinguished by the SPI-4 RTCL signal. (logic one = control word).

DIP-4 check

For the DIP-4 check algorithm refer to the OIF SPI-4 document [Glossary]. In both IN_SYNCH and OUT_OF_SYNCH states, only control word previous and following data is checked. Any transition on synch status will be captured. In IN_SYNCH state, each DIP-4 error is captured and counted.

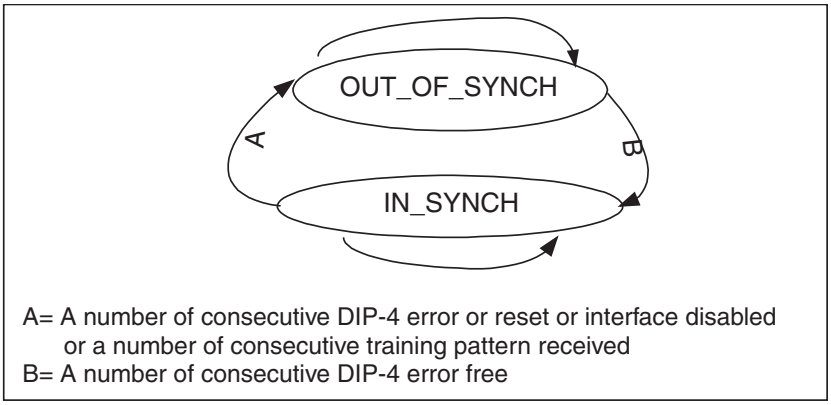


Figure 8. SPI-4 ingress state diagram

Transfer decode

The SPI-4 ingress control word contains various fields. Refer to the OIF SPI-4 document [Glossary] for details. If reserved control word, BIT[15:12]=0011, 0001, 0101, or 0111 is detected, a BUS_ERROR event is generated. If a payload control word is not followed by a data word, or a data word does not follow a payload control word, a BUS_ERROR event is generated. If abort is detected, the next packet will be tagged with an error.

Data dispatch

The port address field of a payload control word is extracted as a search key. The search key is used to search the dispatch info in Table 86, SPI-4 ingress LP to LID map (256 entries, one per LP). If the searched port is active, transfer data is sent to the associated PFP with SOP, EOP, LENGTH, PACKET_ERROR. If the searched port is inactive, a SPI4_INACTIVE_TRANSFER event is generated. A SPI-4 inactive transfer event with it's associated LP will be captured in the Table 40, SPI-4 status register (0x22 in the direct accessed space).

SPI-4 ingress status channel

Calendar structure and swapping

The SPI Exchange supports one or two sets of calendars. If I_CSW_EN field in the Table 89, SPI-4 ingress configuration register (0x00)=1, two sets of calendars are supported. A calendar selection word must be placed following the framing bit. Refer to the OIF SPI-4 document [see Glossary] for more details.

SPI-4 ingress status channel frame generation

The status frame can be one of the following cases:

- All '11' when LVTTL is in the out of synch state
- Training pattern when LVDS is in the out of synch state or in periodic training

- Normal status information when in the IN_SYNCH state

The normal status information is generated based on ingress buffer full information and PFP buffer segment fill level.

For information on DIP-2 generation and training pattern refer to the OIF SPI-4 document [Glossary].

DIP-2 error insertion

A number of consecutive DIP-2 errors can be generated. The I_DIP_E_NUM field in Table 97, SPI-4 ingress diagnostics register (register_offset 0x0F) specifies the number of errors to be generated. A logic one written to I_ERROR_INS will activate the I_DIP_E_NUM field and trigger error insertion. The I_ERROR_INS field self clears when the number of errors have been generated.

LVTTL and LVDS status interface selection

The LVDS_STA pin selects which FIFO status interface is being used for SPI-4. HIGH = LVDS status interface, LOW = LVTTL status interface.

3.2.2 SPI-4 egress

The SPI-4 egress includes

- Status channel synchronization
- Status updating
- Data transfer
- Periodic training
- PFP interface

SPI-4 egress configurable parameters

All parameters as listed in the 0IF SPI-4 document [see Glossary]
CALENDAR_LEN: 4 to 1,024 in increments of 4
CALENDAR_M: 1 to 256 in increments of 1
MaxBurst1 (MaxBurst_S): 16 to 256 in increments of 16
MaxBurst2 (MaxBurst_H): 16 to 256 in increments of 16
Alpha: 1 to 256 in increments of 1
DATA_MAX_T: 1 to 4,294,967,040 in increments of 1
FIFO_MAX_T: 1 to 16,777,215 in increments of 1

Calendar and shadow calendar

- 256 entries
- E_CSW_EN field in Table 104, SPI-4 egress configuration register_0 (register_offset 0x00) bit for manual reconfiguration swap

Multiple burst enable

- Allows more than one burst to be sent to an LP. Feature included to relieve systems with long latency between updates.

SPI-4 egress LID to LP map

- 256 entries, one per SPI-4 LP
- Enable bit

3.2.3 SPI-4 startup handshake

TABLE 10 – BOTH ATTACHED DEVICES START FROM RESET STATUS

Ingress	egress
Out of synch, send status training	Out of synch, send data training
In synch, send status frame	Out of synch, send data training
In synch, send status frame	In synch, send data/idle

TABLE 11 – INGRESS OUT OF SYNCH, EGRESS IN SYNCH

Ingress	Egress
Out of synch, send status training	In synch, send data/idle
Out of synch, send status training	Out of synch, send data training
In synch, send status frame	Out of synch, send data training
In synch, send status frame	In synch, send data/idle

TABLE 12 – INGRESS IN SYNCH, EGRESS OUT OF SYNCH

Ingress	Egress
In synch, send status frame	Out of synch, send data training
Out of synch, send status training	Out of synch, send data training
In synch, send status frame	Out of synch, send data training
In synch, send status frame	In synch, send data/idle

SPI-4 egress status channel

Status channel bit alignment

The bit alignment algorithm for the status channel is the same as was described for the data channel.

Status Channel Frame synchronization

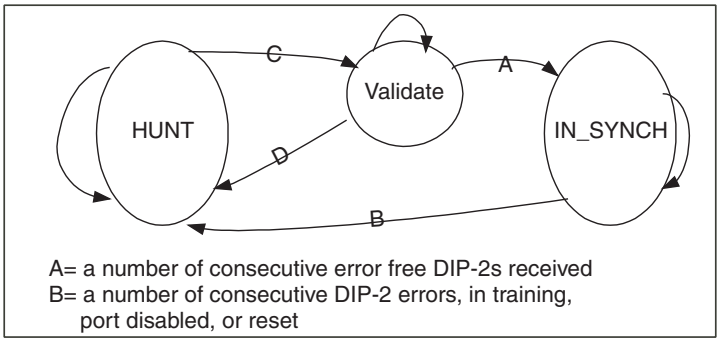


Figure 9. SPI-4 egress status state diagram

The status channel frame module has 3 states: HUNT, VALIDATE and IN_SYNCH.

In the HUNT state, the status channel frame module searches for status frame, status clear and status freeze.

In the VALIDATE state, the status channel frame module checks DIP-2.

In the IN_SYNCH state, the status channel frame module checks DIP-2, and updates status.

HUNT state

- In the HUNT state, per Link status is fixed to 'satisfied'.
- In HUNT state, the PFP searches frame continuously. It transitions to the VALIDATE state if a single valid frame is found accompanied by a single valid training pattern. A frame is considered to be found if : 1) only one frame word is at the beginning of a frame, 2) the calendar selection word, if enabled, is matched, and 3) the DIP-2 calculation matched the received DIP-2.

VALIDATE state

In the validate state, based on the frame found while in the HUNT state, the DIP-2 is checked.

If a single DIP-2 error is found, transition to the HUNT state.

After a number of consecutive DIP-2 calculations proves to be error free, transition to the IN_SYNCH state. The number is defined by the E_INSYNC_THR field in Table 104-SPI-4 egress configuration register_0 (Block_base 0x0700 + Register_offset 0x00).

In the validate state, the training pattern is not checked.

IN_SYNCH state

In the IN_SYNCH state, training frame and status frame are checked.

DIP-2 is checked for status frame. Each mismatched DIP-2 will generate a DIP-2 error event, each event will be captured and counted.

After a number of consecutive DIP-2 errors, transition to the HUNT state. (Clear status in HUNT mode). The number is defined by the E_OUTSYNC_THR field in Table 104-SPI-4 egress configuration register_0 (Block_base 0x0700 + Register_offset 0x00).

The reception of twelve consecutive training patterns forces a transition to HUNT mode. If less than twelve consecutive training patterns are received, synch will not be lost, and status frame starts at the end of training.

Twelve consecutive '11' patterns force a transition to the HUNT state.

Status updating occurs without waiting for the end of a status frame.

Status channel de-skew

The LVDS status channel deskew uses the same algorithm as the as the data channel.

LVTTL or LVDS status channel option

The LVDS_STA pin selects the interface type. A logic high enables the LVDS status interface. A logic low enables the LVTTL status interface.

Data channel

Data transfer and training

At any cycle, the contents on the interface can be one of the following:

- Control word: Payload control word, or idle control word or training control word.
- Data word: Payload data word or training data word.

In the HUNT or the VALIDATE state, the training pattern is sent.

In the IN_SYNCH state, data from is taken from the buffer segments and egressed to the SPI-4 interface. The switch between data burst, IDLE, and training must obey the following rules:

- Send IDLE if no data to transmit
- SOP must not occur less than 8 cycles apart.
- periodic training after current transfer finished

Payload control word generation:

- Bit 15, Control word type=1
- Bit [14:13] EOPS per [see Glossary: SPI-4]. If an error tag is in the descriptor, abort.
- Bit [12] SOP refer to [see Glossary: SPI-4]
- Eight Bit Address. Mapping table defined in Table 101, SPI-4 egress LID to LP map (256 entries)
- DIP-4 bit refer to [see Glossary]

Payload data word

- Bit order refer to [see Glossary: SPI-4]
- If only one byte is valid, 8 LSB (B7 to B0) is set to 0x00.

No status channel option

Once the NOSTAT bit is set, the status channel is ignored. Refer to Table 104, SPI-4 egress configuration register_0 (register_offset 0x00).

Status in default value.

No DIP error check.

No status updating, the received status fixed to STARVING.

Data channel works same as in IN_SYNCH state.

3.3 Microprocessor interface

- Parallel microprocessor interface
  - 8 bit data bus for parallel operation
  - Byte access
  - Direct accessed space
  - Indirect access space is used for most registers
  - Read operations to a reserved address or reserved bit fields return 0
  - Write operations to reserved addresses or bit fields are ignored
- Serial microprocessor interface
  - Compliance to Motorola serial processor interface (SPI) specification
  - Byte access
  - Direct accessed space
  - Indirect access space is used for most registers
  - Read operations to a reserved address or reserved bit fields return 0
  - Write operations to reserved addresses or bit fields are ignored

General purpose I/O

Five general purpose I/O pins are provided. The direction is independently controlled by the DIR_OUT field in the GPIO register (Table 123 GPIO Register (0x20)). The logical level on a pin is controlled by the LEVEL field in the GPIO register if DIR_OUT=1, or sensed if DIR_OUT=0. The LEVEL bit monitors the logic level of any bit selected from the indirect access space if MONITOR_EN is set high. A bit in the indirect access space can be selected for monitoring by the by the ADDRESS and BIT fields in the GPIO Link table (Table 124, *GPIO Monitor Table (5 entries 0x21-0x25 for GPIO[0] through GPIO[4])*).

All GPIO pins must be programmed into or out of monitor mode at the same time.

Interrupt scheme

Events are captured in interrupt status registers. Interrupt status flags are cleared by an microprocessor write cycle. A logical one must be written to clear the flag(s) targeted. A two level interrupt scheme is provided comprising a primary level and a secondary level.

The primary level identifies the secondary interrupts sources with a pending interrupt. This information is reflected in the primary interrupt register. Interrupt status can be enabled by associated flags both in the primary and secondary level of the interrupt scheme.

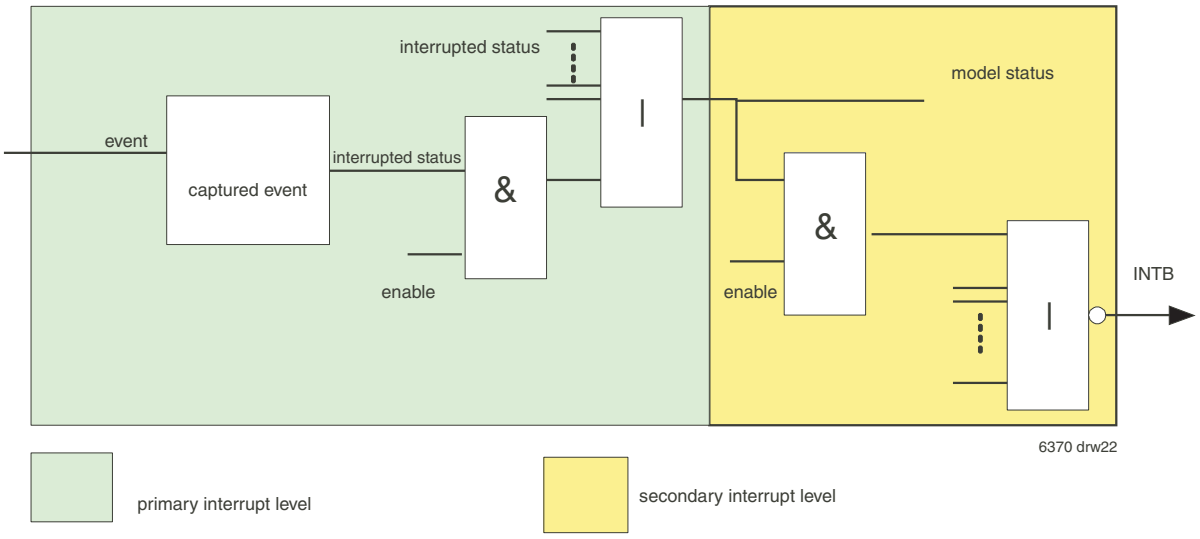


Figure 10. Interrupt scheme

4. DATAPATH AND FLOW CONTROL

The following sections describe the datapaths through the device. The datapaths shown are as follows:

- SPI-3A <-> SPI-4
- SPI-3B <-> SPI-4
- SPI-3C <-> SPI-4
- SPI-3D <-> SPI-4
- SPI-3A <-> SPI-3B
- SPI-3C <-> SPI-3D
- SPI-3A <-> microprocessor interface
- SPI-3B <-> microprocessor interface
- SPI-3C <-> microprocessor interface
- SPI-3D <-> microprocessor interface
- SPI-4 <-> microprocessor interface

Where <-> indicates a bidirectional data path.

The IDT88P8344 supports four SPI-3 interfaces and a single SPI-4 interface. All SPI-3 interfaces can operate independently in a PHY or Link mode. Refer to Figure 11, *Definition of Data Flows* for the main data flows in the device. Independent logical data flows are transported over each of the physical ports. Those logical flows are identified by logical port addresses on the physical port and by a Link identification (LID) map in the core of the IDT88P8344.

DATA BUFFER ALLOCATION

Flexibility has been provided to the user for data buffer allocation. The device has 128 KByte of on chip memory per SPI-3 port per direction – a total of 1MByte of on-chip data memory.

The 128 KByte SPI-3 buffers (8 instantiations per device) are divided into 256 byte segments. The segments are controlled by a packet fragment processor. The user configures the maximum number of segments per LP to allocate to a port and the number of segments allocated from the buffer segment pool that will trigger the flow control mechanism. There is no limitation on the reallocation of freed segments among logical ports, as would be present if the memory had been allocated by a simple address mechanism.

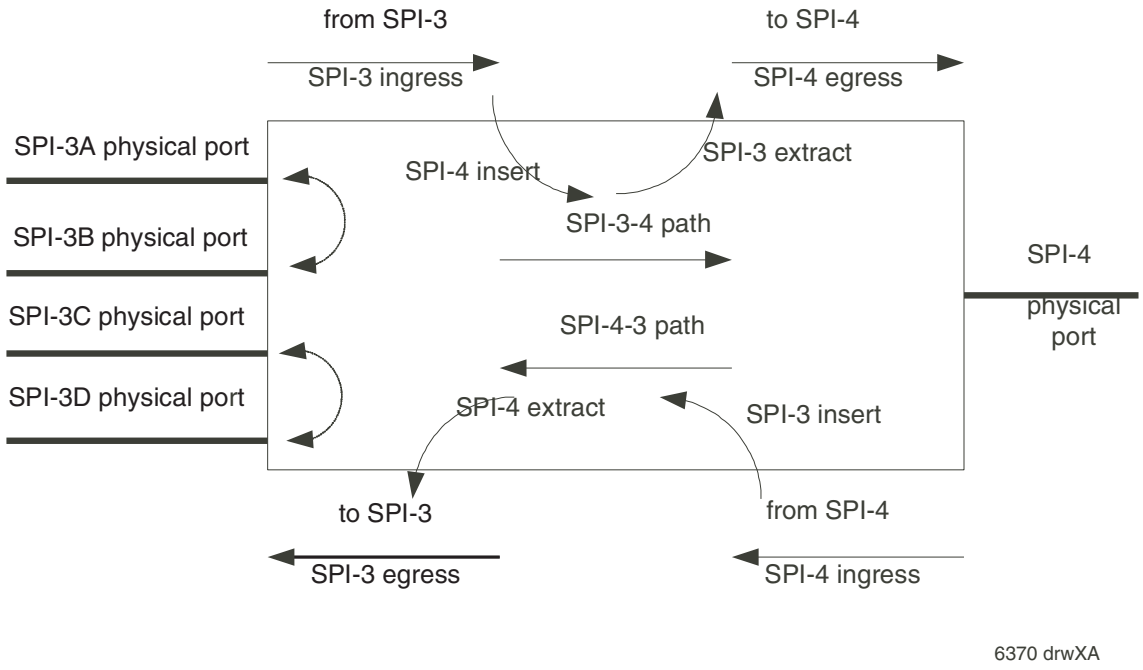


Figure 11. Definition of data flows

DATAPATH CONFIGURATION

A logical view of datapath configuration using Packet Fragment Processors is shown in Figure 12, *Logical View of Datapath Configuration Using PFPs*. Two PFPs are associated with each SPI-3 port, one for ingress and one for egress. Logical ports are mapped internally into Logical Identifiers ("LIDs", "LID Map") for the control of each per-LID data flow to each physical port, logical port, memory queue size, and backpressure threshold (watermark), by programming the LID register files.

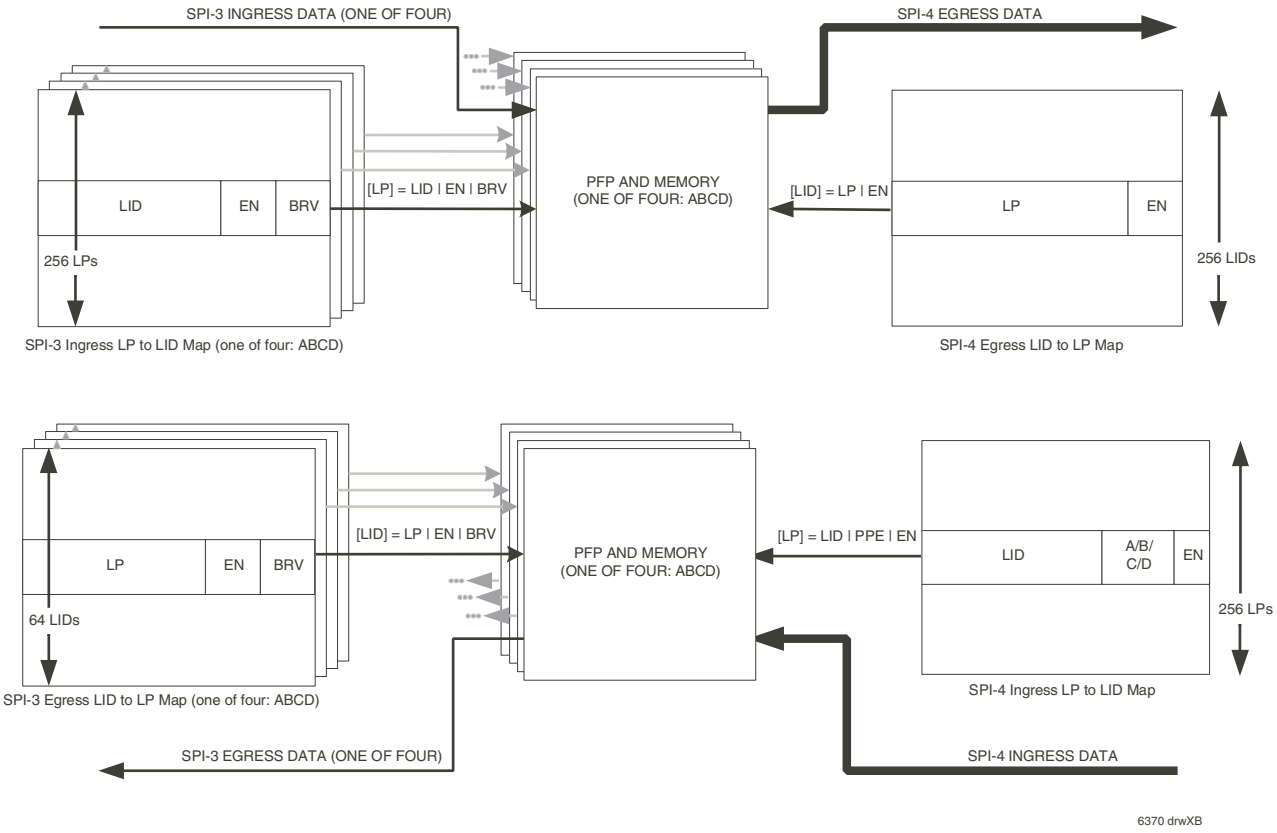


Figure 12. Logical view of datapath configuration using PFPs

LID - Logical Identifier
EN - LID enable flag
BRV - Bit reversal
LP - Logical port
PFP - Packet fragment processor

4.1 SPI-3 to SPI-4 datapath and flow control

Four packet fragment processor modules from SPI-3 to SPI-4 are provided. One packet fragment processor module is associated with one SPI-3 ingress interface. All four packet fragment processor modules connect to a single SPI-4 interface.

Packet fragments from the SPI-3 ingress are received into the SPI-3 ingress port buffers. A packet fragment processor transfers complete packet fragments from the SPI-3 ingress port buffers to memory segments previously reserved on a per-LP basis in the buffer segment pool. The SPI-3 ingress port buffer watermark and the per-LP free buffer segment threshold information is combined to produce SPI-3 ingress FIFO status towards the attached device. Packets or packet fragments received on one SPI-3 ingress logical port can be forwarded to any one of:

A logical port on the egress SPI-4 interface.

A logical port on an associated SPI-3 interface (between physical port interfaces A and B, and between C and D only).

The microprocessor interface, using the capture buffer.

The connection on the logical port level is performed through an intermediate mapping to a Link Identification number (LID).

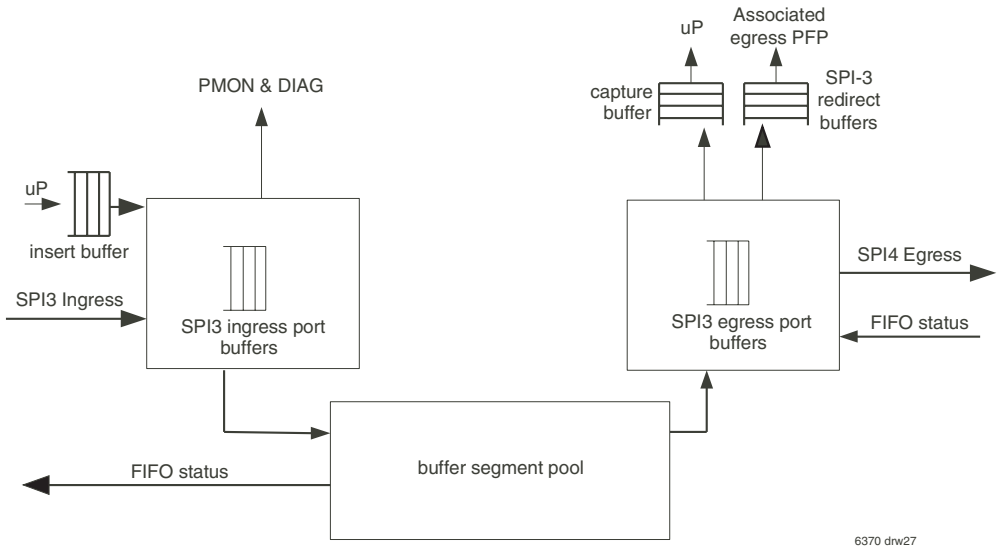


Figure 13. SPI-3 ingress to SPI-4 egress packet fragment processor

SPI-3 ingress PFP functions

The packet fragment processor(PFP) receives status information about the SPI-3 ingress buffers and the microprocessor insert buffer. The PFP processes SPI-3 ingress buffers in high priority and the insert buffer with low priority. The PFP copies data into the buffer segment , requests new buffer segments, and generates entries in the SPI4-egress queue.

SPI-3 ingress buffer processing

The PFP verifies whether a SPI-3 ingress buffer is occupied. If the SPI-3 ingress buffer is not occupied the PFP processes the insert buffer.

Normal operation

In loopback mode, all of the SPI-3 ingress buffers of a physical SPI-3 port are copied into the SP-3 egress buffers of that same port. This is a test mode only, as no non-loopback traffic can be transferred at this time.

In non – loop back mode (normal operation) the SPI-3 ingress buffers are forwarded to the LID process by the PFP.

The LID process generates a set of events for an associated LID. The events that are directed towards the PMON&DIAG module are:

- SPI-3 error tagged packet event (errored packets)
- SPI-3 EOP event (all packets)
- SPI-3 fragment event (all fragments) with an associated length field