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Features

- 80C51 Core
  - 12 or 6 Clocks per Instruction (X1 and X2 Modes)
  - 256 Bytes Scratchpad RAM
  - Dual Data Pointer
  - Two 16-bit Timer/Counters: T0 and T1
- T83C5121 with 16 Kbytes Mask ROM
- T85C5121 with 16 Kbytes Code RAM
- T89C5121 with 16 Kbytes Code RAM and 16 Kbytes EEPROM
- On-chip Expanded RAM (XRAM): 256 Bytes
- Versatile Host Serial Interface
  - Full-duplex Enhanced UART (EUART) with Dedicated Baud Rate Generator (BRG): Most Standard Speeds up to 230K bits/s at 7.36 MHz
  - Output Enable Input
  - Multiple Logic Level Shifters Options (1.8V to V_{CC})
  - Automatic Level Shifter Option
- Multi-protocol Smart Card Interface
  - Certified with Dedicated Firmware According to ISO 7816, EMV2000, GIE-CB, GSM 11.12V and WHQL Standards
  - Asynchronous Protocols T = 0 and T = 1 with Direct and Inverse Modes
  - Baud Rate Generator Supporting All ISO7816 Speeds up to D = 32/F = 372
  - Parity Error Detection and Indication
  - Automatic Character Repetition on Parity Errors
  - Programmable Timeout Detection
  - Card Clock Stop High or Low for Card Power-down Mode
  - Support Synchronous Card with C4 and C8 Programmable Outputs
  - Card Detection and Automatic De-activation Sequence
  - Step-up/down Converter with Programmable Voltage Output: 5V, 3V (± 8% at 60 mA) and 1.8V (±8% at 20 mA)
  - Direct Connection to Smart Card Terminals:
    Short Circuit Current Limitation
    Logic Level Shifters
    4 kV ESD Protection (MIL/STD 833 Class 3)
- Alternate Card Support with CLK, I/O and RST According to GSM 11.12V Standard
- 2x I/O Ports: 6 I/O Port1 and 8 I/O Port3
- 2x LED Outputs with Programmable Current Sources: 2, 4, or 10 mA
- Hardware Watchdog
- Reset Output Includes
  - Hardware Watchdog Reset
  - Power-on Reset (POR)
  - Power-fail Detector (PFD)
- 4-level Priority Interrupt System with 7 Sources
- 7.36 to 16 MHz On-chip Oscillator with Clock Prescaler
- Absolute CPU Maximal Frequency: 16 MHz in X1 mode, 8MHz in X2 mode
- Idle and Power-down Modes
- Voltage Operation: 2.85V to 5.4V
- Low Power Consumption
  - 8 mA Operating Current (at 5.4V and 3.68 MHz)
  - 150 mA Maximum Current with Smart Card Power-on (at 16 MHz X1 Mode)
  - 30 µA Maximum Power-down Current at 3.0V (without Smart Card)
  - 100 µA Maximum Power-down Current at 5.4V (without Smart Card)
- Temperature Range
  - Commercial: 0 to +70°C Operating Temperature
  - Industrial: -40 to +85°C Operating Temperature
- Packages
  - SSOP24
  - QFN32
  - PLCC52

8-bit Microcontroller with Multi-protocol Smart Card Interface

T83C5121
T85C5121
T89C5121
AT83C5121
AT85C5121
AT89C5121

Rev. 4164G–SCR–07/06

Description

T8xC5121 is a high performance CMOS ROM/CRAM derivative of the 80C51 CMOS single chip 8-bit microcontrollers.

T8xC5121 retains the features of the Atmel 80C51 with extended ROM capacity (16 Kbytes), 512 bytes of internal RAM, a 4-level interrupt system, two 16-bit timer/counters (T0/T1), a full duplex enhanced UART (EUART) with baud rate generator (BRG) and an on-chip oscillator.

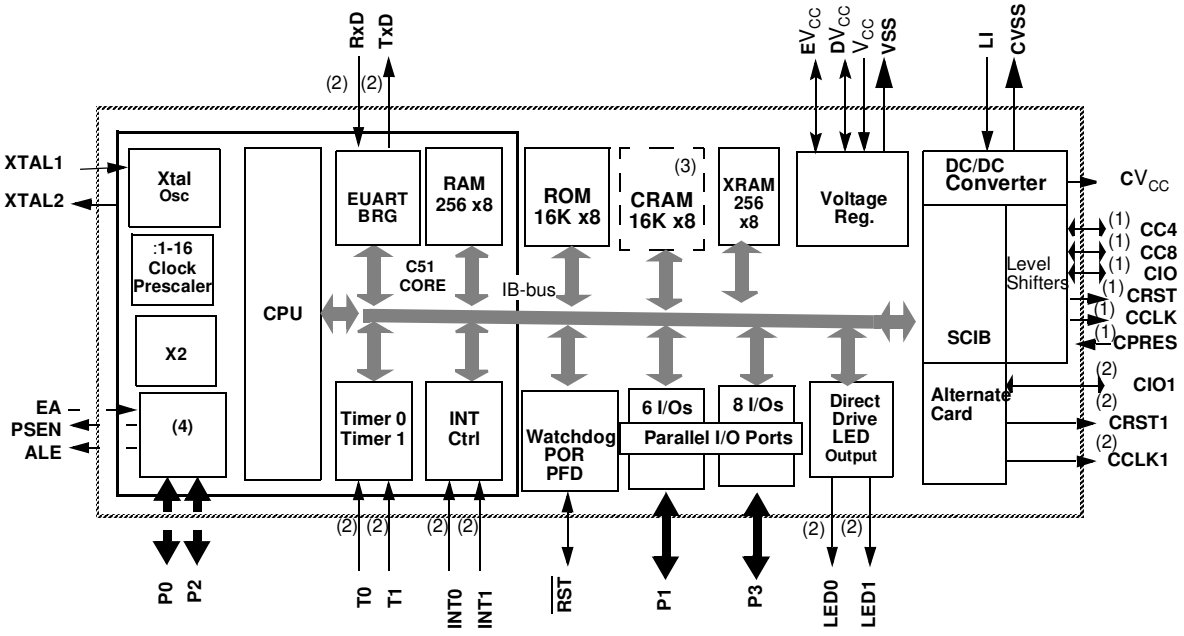
In addition, the T8xC5121 have, a Multi protocol Smart Card Interface, a dual data pointer, 2 programmable LED current sources (2-4-10 mA) and a hardware Watchdog.

T89C5121 Flash RAM version and T85C5121 Code RAM version can be loaded by In-System Programming (ISP) software residing in the on-chip ROM from a low-cost external serial EEPROM or from R232 interface.

T8xC5121 have 2 software-selectable modes of reduced activity for further reduction in power consumption.

Block Diagram

Figure 1. Block Diagram



Notes:
1. Alternate function of Port 1
2. Alternate function of Port 3
3. Only for the Code RAM version
4. Only for PLCC52

Pin Description

Figure 2. 24-pin SSOP Pinout

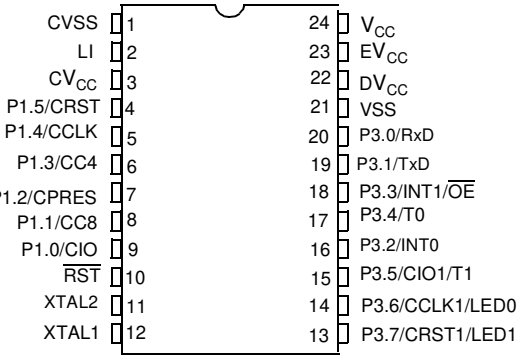


Figure 3. QFN32 Pinout

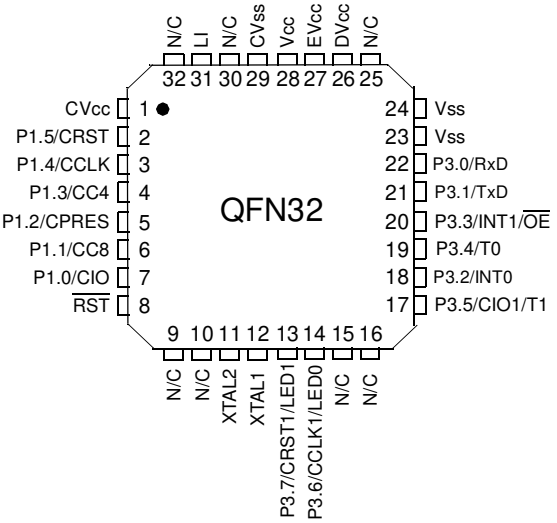
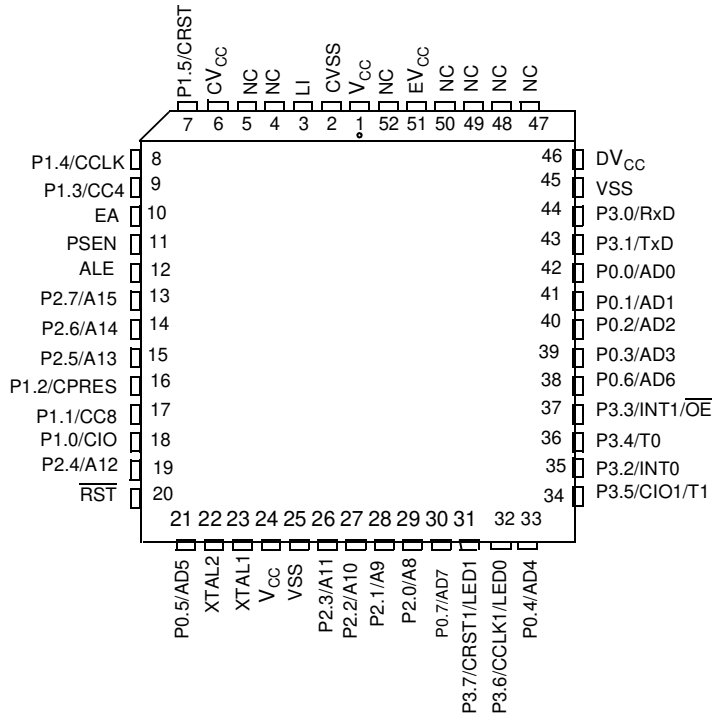


Figure 4. PLCC52 Pinout



Signals

All the T8xC5121 signals are detailed in Table 1.

The port structure is described in Section “Port Structure Description”.

Table 1. Ports Description

Port	Signal Name	Alternate	Internal Power Supply	ESD	Type	Description
P1.0	CIO		CV_{CC}	4 kV	I/O	**Smart card interface function** Card I/O.
					I/O	**Input/Output function** P1.0 is a bi-directional I/O port .
					I	**Reset configuration** Input .
P1.1	CC8		CV_{CC}	4 kV	O	**Smart card interface function** Card contact 8
					O	**Output function** P1.1 is a Push-pull port.
					I	**Reset configuration** Input
P1.2	CPRES		V_{CC}	4 kV	I	**Smart card interface function** Card presence
					I/O	**Input/Output function** P1.2 is a bi-directional I/O port with internal pull-ups- (External Pull-up configuration can be selected).
					I	**Reset configuration** Input (high level due to internal pull-up)
P1.3	CC4		CV_{CC}	4 kV	O	**Smart card interface function** Card contact 4
					O	**Output function** P1.3 is a Push-pull port.
					I	**Reset configuration** Input (high level due to internal pull-up)
P1.4	CCLK		CV_{CC}	4 kV	O	**Smart card interface function** Card clock
					I/O	**Input/Output function** P1.4 is a a Push-pull port.
					O	**Reset configuration** Output at low level
P1.5	CRST		CV_{CC}	4 kV	O	**Smart card interface function** Card reset
					I/O	**Input/Output function** P1.5 is a a Push-pull port.
					O	**Reset configuration** Output at low level

Table 1. Ports Description (Continued)

Port	Signal Name	Alternate	Internal Power Supply	ESD	Type	Description
P3.0	RxD		EV_{CC}		I	**UART function** Receive data input
					I/O	**Input/Output function** P3.0 is a bi-directional I/O port with internal pull-ups.
					I	**Reset configuration** Input (high level)
P3.1	TxD		EV_{CC}		O	**UART function** Transmit data output OE active at low or high level depending of PMSOEN bits in SIOCON Reg.
					I/O	**Input/Output function** P3.1 is a bi-directional I/O port with internal pull-ups.
					Z	**Reset configuration** High impedance due to PMOS switched OFF
P3.2	INT0		DV_{CC}		I	**External interrupt 0** $\overline{INT0}$ input set IE0 in the TCON register. If bit IT0 in this register is set, bits IE0 are set by a falling edge on $\overline{INT0}$. If bit IT0 is cleared, bits IE0 is set by a low level on $\overline{INT0}$.
					I/O	**Input/Output function** P3.2 is a bi-directional I/O port with internal pull-ups.
					I	**Timer 0: Gate input** INT0 serves as external run control for Timer 0 when selected in TCON register.
					I	**Reset configuration** Input (high level)
P3.3	INT1	OE	EV_{CC}		I	**External Interrupt 1** $\overline{INT1}$ input set OEIT in ISEL Register, IE1 in the TCON register. If bit IT1 in this register is set, bits OEIT and IE1 are set by a falling edge on $\overline{INT1}$. If bit IT1 is cleared, bits OEIT and IE1 is set by a low level on $\overline{INT1}$
					I	**UART function** Output enable. A low or high level (depending OELEV bit in ISEL Register) on this pin disables the PMOS transistors of TxD (P3.1) and T0 (P3.4). This function can be disabled by software
					I/O	**Input/Output function** P3.3 is a bi-directional I/O port with internal pull-ups.
					I	**Timer 1 function: Gate input** INT1 serves as external run control for Timer 1 when selected in TCON register.
					I	**Reset configuration** Input (high level)
P3.4		T0	EV_{CC}		O	**UART function** OE active at low or high level depending of PMSOEN bits in SIOCON Reg.

Table 1. Ports Description (Continued)

Port	Signal Name	Alternate	Internal Power Supply	ESD	Type	Description
					I/O	**Input/Output function** P3.4 is a bi-directional I/O port with internal pull-ups.
					I	**Timer 0 function: External clock input** When Timer 0 operates as a counter, a falling edge on the T0 pin increments the count.
					Z	**Reset configuration** High impedance due to PMOS switched OFF
P3.5	CIO1		DV_{CC}		I/O	**Alternate card function** Card I/O
					I/O	**Input/Output function** P3.5 is a bi-directional I/O port with internal pull-ups.
					I	**Timer 1 function: External clock input** When Timer 1 operates as a counter, a falling edge on the T1 pin increments the count.
					I	**Reset configuration** Input (high level due to internal pull-up)
P3.6	CCLK1	LED0	DV_{CC}		O	**Alternate card function** Card clock
					O	**LED function** These pins can be directly connected to the cathode of standard LED without external current limiting resistors. The typical current of each output can be programmed by software to 2, 4 or 10 mA (LEDCON register).
					I/O	**Input/Output function** P3.6 is a LED port.
					I	**Reset configuration** Input at high level
P3.7	CRST1		DV_{CC}		O	**Alternate card function** Card reset
P3.7	CRST1	LED1	DV_{CC}		O	**LED function** These pins can be directly connected to the cathode of standard LED without external current limiting resistors. The typical current of each output can be programmed by software to 2, 4 or 10 mA (LEDCON register).
					I/O	**Input/Output function** P3.7 is a a LED port.
					I	**Reset configuration** Input at high level

Table 1. Ports Description (Continued)

Port	Signal Name	Alternate	Internal Power Supply	ESD	Type	Description
RST			V_{CC}		I/O	**Reset input** Holding this pin low for 64 oscillator periods while the oscillator is running resets the device. The Port pins are driven to their reset conditions when a voltage lower than V_{IL} is applied, whether or not the oscillator is running. This pin has an internal pull-up resistor which allows the device to be reset by connecting a capacitor between this pin and VSS.This capacitor is optional thanks to the internal POR which output a Reset as long as Vcc has not reached the POR threshold level Asserting $\overline{RST}$ when the chip is in Idle mode or Power-down mode returns the chip to normal operation. The output is active for at least 12 oscillator periods when an internal reset occurs.
XTAL1			V_{CC}		I	**Input to the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin.
XTAL2			V_{CC}		O	**Output of the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, XTAL2 may be left unconnected.
V_{CC}					PWR	**Supply voltage** V_{CC} is used to power the internal voltage regulators and internal I/O's.
LI					PWR	**DC/DC input** LI must be tied to V_{CC} through an external coil (typically 4, 7 µH) and provide the current for the pump charge of the DC/DC converter.
CV_{CC}					PWR	**Card Supply voltage** CV_{CC} is the programmable voltage output for the Card interface. It must be connected to an external decoupling capacitor.
DV_{CC}					PWR	**Digital Supply voltage** DV_{CC} is used to supply the digital core and internal I/Os. It is internally connected to the output of a 3V regulator and must be connected to an external decoupling capacitor.
EV_{CC}			V_{CC}		PWR	**Extra supply voltage** EV_{CC} is used to supply the level shifters of UART interface I/O pins. It must be connected to an external decoupling capacitor. This reference voltage is generated internally (automatically or not), or it can be connected to an external voltage reference.
CVSS					GND	**DC/DC ground** CVSS is used to sink high shunt currents from the external coil.
VSS					GND	**Ground**

Table 1. Ports Description (Continued)

Port	Signal Name	Alternate	Internal Power Supply	ESD	Type	Description
ONLY FOR PLCC52 version						
P0[7:0]	AD[7:0]		V_{CC}		I/O	**Input/Output function Port 0** P0 is an 8-bit open-drain bi-directional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. To avoid any parasitic current consumption, Floating P0 inputs must be pulled to V_{CC} or V_{SS}.
					I/O	**Address/Data low** Mutiplexed Address/Data LSB for external access
P2[7:0]	A[15:8]		V_{CC}		I/O	**Input/Output function Port 2** P2 is an 8-bit open-drain bi-directional I/O port with internal pull-ups
					O	**Address high** Address Bus MSB for external access
P3.6	WR		DV_{CC}		O	**Write signal** Write signal asserted during external data memory write operation
P3.7	RD		DV_{CC}		I	**Read signal** Read signal asserted during external data memory read operation
ALE			V_{CC}		O	**Address latch enable output** The falling edge of ALE strobes the address into external latch
PSEN	PSEN		V_{CC}		O	**Program strobe enable**
EA	EA		V_{CC}		I	**External access enable** This pin must be held low to force the device to fetch code from external program memory starting at address 0000h. It is latched during reset and cannot be dynamically changed during operation.

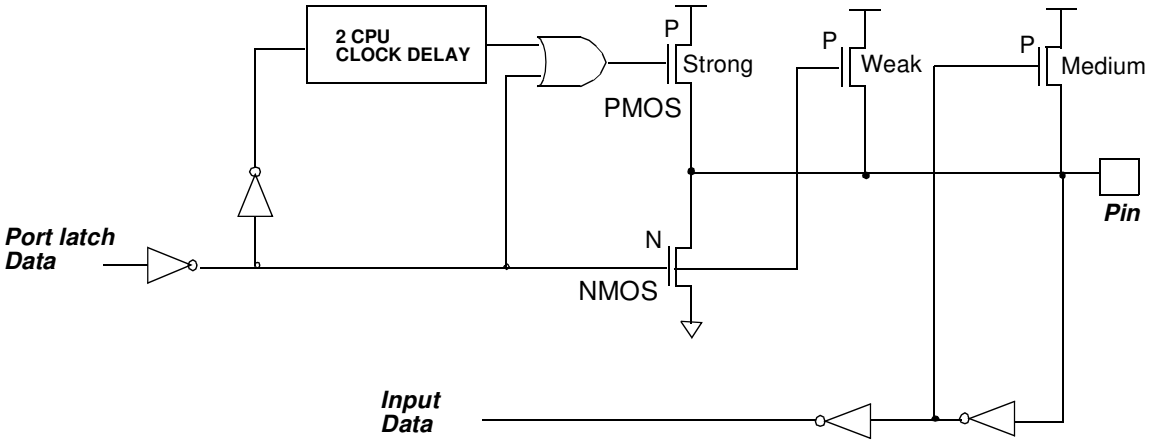
Port Structure Description

The different ports structures are described as follows.

Quasi Bi-directional Output Configuration

The default port output configuration for standard I/O ports is the quasi bi-directional output that is common on the 80C51 and most of its derivatives. This output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low. When the port outputs a logic low state, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open drain output except that there are three pull-up transistors in the quasi bi-directional output that serve different purposes. One of these pull-ups, called the weak pull-up, is turned on whenever the port latch for the pin contains a logic 1. The weak pull-up sources a very small current that will pull the pin high if it is left floating. A second pull-up, called the medium pull-up, is turned on when the port latch for the pin contains a logic 1 and the pin itself is also at a logic 1 level. This pull-up provides the primary source current for a quasi bi-directional pin that is outputting a 1. If a pin that has a logic 1 on it is pulled low by an external device, the medium pull-up turns off, and only the weak pull-up remains on. In order to pull the pin low under these conditions, the external device has to sink enough current to overpower the medium pull-up and take the voltage on the port pin below its input threshold.

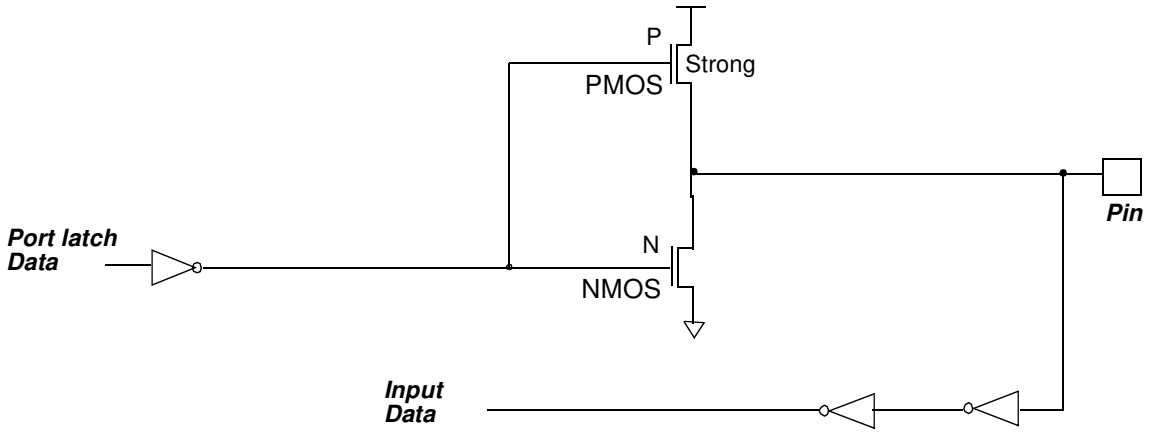
Figure 5. Quasi Bi-directional Output Configuration



Push-pull Output Configuration

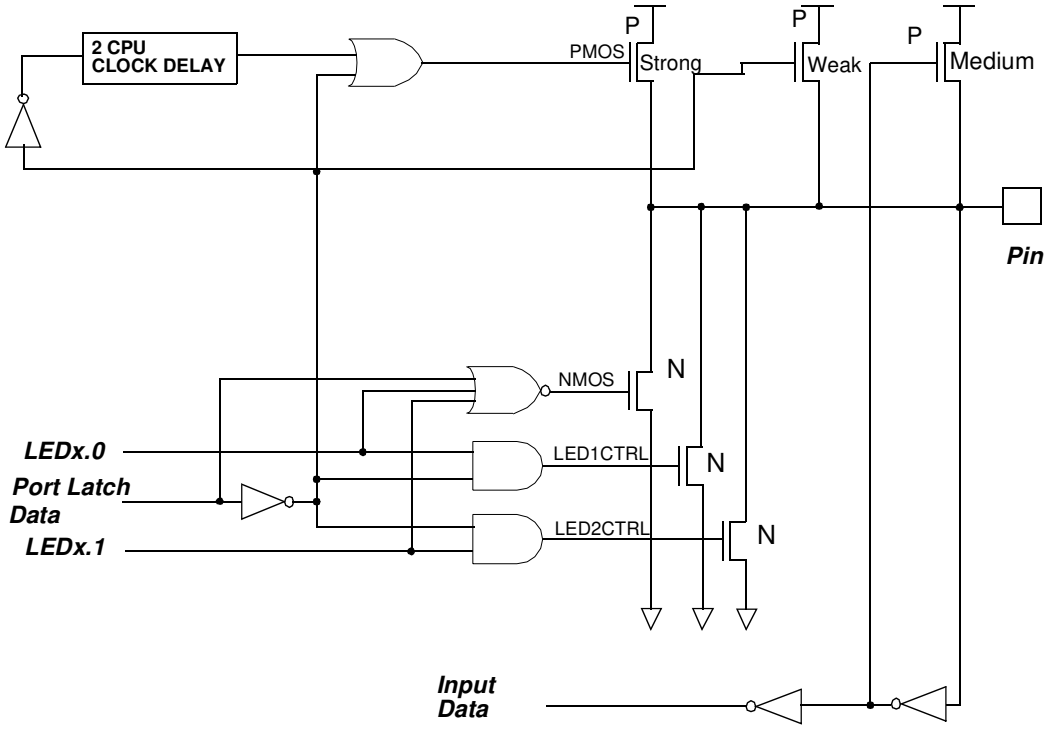
The Push-pull output configuration has the same pull-down structure as the quasi bi-directional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The Push-pull mode may be used when more source current is needed from a port output. The Push-pull port configuration is shown in Figure 5.

Figure 6. Push-pull Output Configuration



LED Output Configuration The input only configuration is shown in Figure 7.

Figure 7. LED Source Current Configuration



Note: The port can be configured in quasi bi-directional mode and the level of current can be programmed by means of LEDCON0 and LEDCON1 registers before switching the led on by writing a logical 0 in Port latch.

SFR Mapping

The Special Function Registers (SFR) of the T8xC5121 belongs to the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP
- I/O port registers: P0, P1, P2, P3
- Timer 0 registers: TCON, TH0, TH1, TMOD, TL0, TL1
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON, BRL, BDRCON
- Power and clock control registers: PCON, CKRL, CKCON0, CKCON1, DCCKPS
- Interrupt system registers: IE0, IPL0, IPH0, IE1,IPL1, IPH1, ISEL
- Watchdog Timer 0: WDTRST, WDTPRG
- Others: AUXR, AUXR1, RCON
- Smart Card Interface: SCSR, SCCON/SCETU0, SCISR/SCETU1, SCIER/SCIIR, SCTBUF/SCRBUF, SCGT0/SCWT0, SCGT1/SCWT1, SCICR/SCWT2
- Port configuration: SIOCON, LEDCON

Table 2. SFR Addresses and Reset Values

	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h									FFh
F0h	B 0000 0000	LEDCON XXXX 0000							F7h
E8h									EFh
E0h	ACC 0000 0000								E7h
D8h									DFh
D0h	PSW 0000 0000	RCON XXXX OXXX							D7h
C8h									CFh
C0h									C7h
B8h	IPL0 XXX0 0000	SADEN 0000 0000	ISEL 0000 0100					DCCKPS XXXX XX11	BFh
B0h	P3 1111 1111	IE1 XXXX 0XXX	IPL1 XXXX 0XXX	IPH1 XXXX 0XXX	0 SCWT0 * 1000 0000	0 SCWT1 * 0010 0101	0 SCWT2 * 0000 0000	IPH0 XXX0 0000	B7h
					1 SCGT0 * 0000 1100	1 SCGT1* 0000 0000	1 SCICR * 0000 0000		
A8h	IE0 0XX0 0000	SADDR 0000 0000	SCTBUF* 0000 0000	SCSR XXX0 1000	0 SCCON * 0X000	0 SCISR* 10X0 0000	0 SCIIR* 0X00 0000	CKCON1 XXXX 0XXX	AFh
			SCRBUF 0000 000		1 SCETU0 0111 0100	1 SCETU1 0XXX	1 SCIER * 0X00 0000		
A0h	P2 1111 1111		AUXR1 XXX XXX0				WDTRST XXXX XXXX	WDTPRG XXXX X0000	A7h
98h	SCON XXX0 0000	SBUF XXXX XXXX	BRL 0000 0000	BDRCON XXX0 0000					9Fh
90h	P1 XX11 1111	SIOCON 00XX 0000						CKRL XXXX 111X	97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR 00XX XX00	CKCON0 X0X0 X000	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000	20			PCON 00XX XX00	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Reserved

SCRS Bit (SCSR.0)	(*)
0	SFR value
1	SFR value

PowerMonitor

The PowerMonitor function supervises the evolution of the voltages feeding the microcontroller, and if needed, suspends its activity when the detected value is out of specification.

It is guaranteed to start up properly when T8xC5121 is powered up and prevents code execution errors when the power supply becomes lower than the functional threshold.

This section describes the functions of the PowerMonitor.

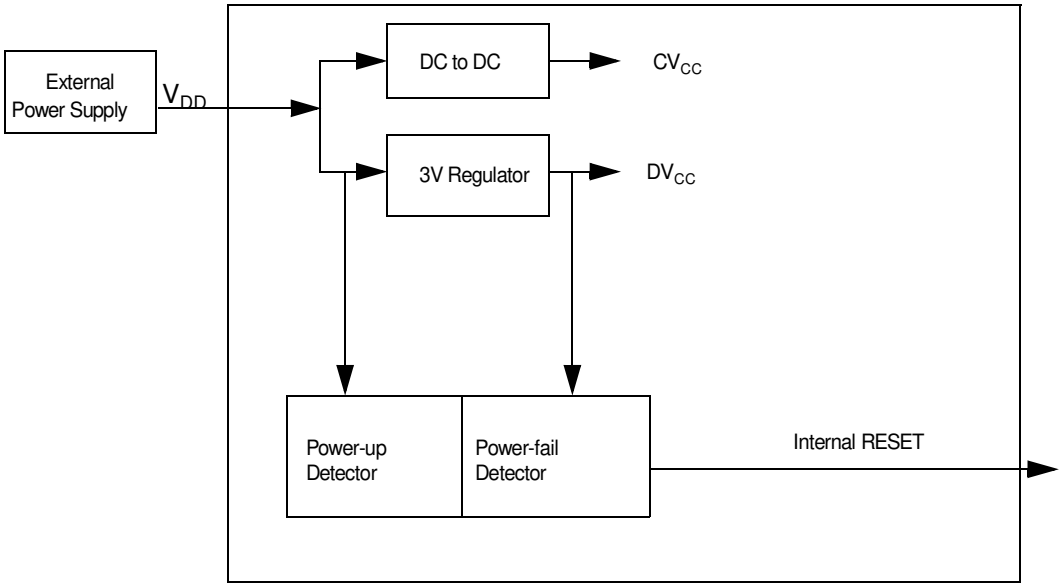
Description

In order to start up and to properly maintain the microcontroller operation, V_{DD} has to be stabilized in the V_{DD} operating range and the oscillator has to be stabilised with a nominal amplitude compatible with logic threshold.

This control is carried out during three phases which are the power-up, normal operation and stop. It complies with the following requirements:

- It guarantees an operational Reset when the microcontroller is powered
- and a protection if the power supply goes out from the functional range of the microcontroller.

Figure 8. PowerMonitor Block Diagram



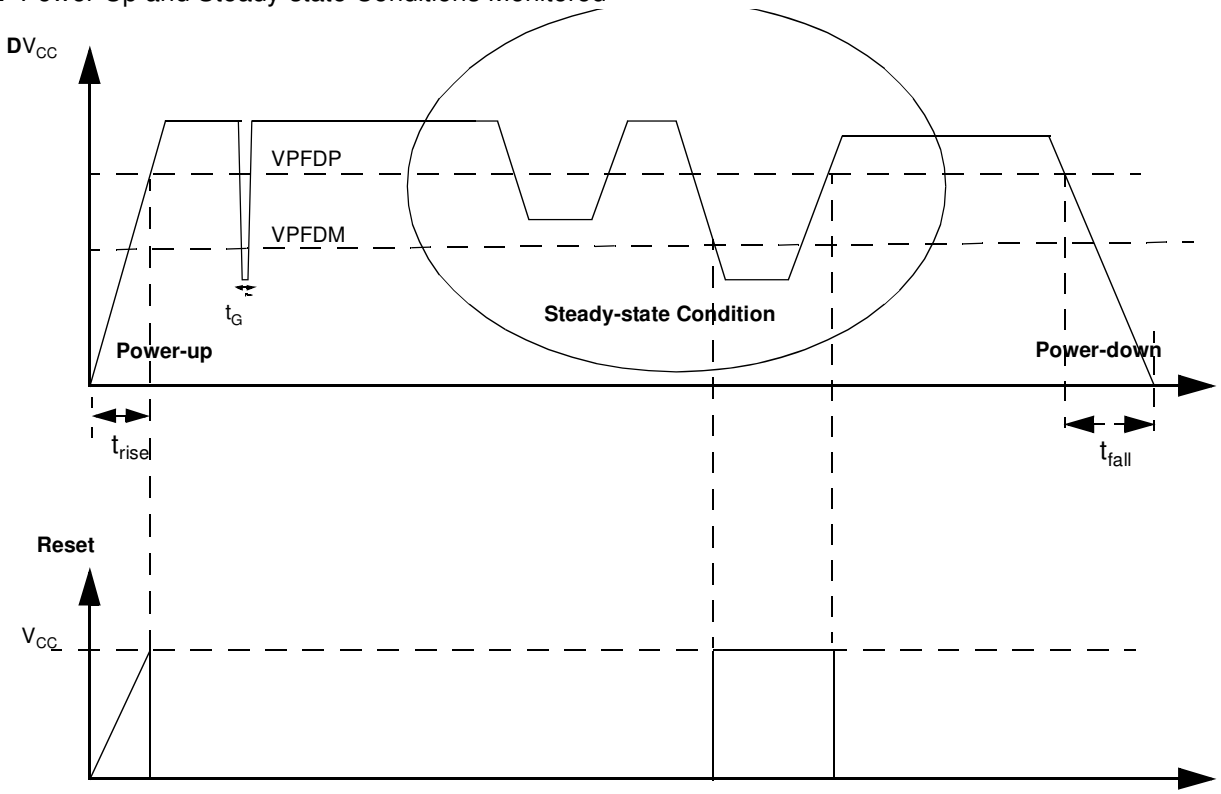
PowerMonitor Diagram

The target of the PowerMonitor is to survey the power supply in order to detect any voltage drops which are not in the target specification. This PowerMonitor block checks two kind of situations that occur:

- During the power-up condition, when V_{DD} is reaching the product specification
- During a steady-state condition, when V_{DD} is stable but disturbed by any undesirable voltage drops.

Figure 9 shows some configurations that can be met by the PowerMonitor.

Figure 9. Power-Up and Steady-state Conditions Monitored



Such device when it is integrated in a microcontroller, forces the CPU in reset mode when V_{DD} reaches a voltage condition which is out of the specification.

The thresholds and their functions are:

- V_{PFDP}: the output voltage of the regulator has reached a minimum functional value at the power-up. The circuit leaves the RESET mode.
- V_{PFDM}: the output voltage of the regulator has reached a low threshold functional value for the microcontroller. An internal RESET is set.

Glitch filtering prevents the system from RESET when short duration glitches are carried on V_{DD} power supply.

The electrical parameters V_{PFDP}, V_{PFDM}, t_{rise}, t_{fall}, t_G are specified in the DCparameters section.

Power Monitoring and Clock Management

For applications where power consumption is a critical factor, three power modes are provided:

- Idle mode
- Power-down mode
- Clock Management (X2 feature and Clock Prescaler)
- 3V Regulator Modes (pulsed or not pulsed)

Idle Mode

An instruction that sets PCON.0 causes the last instruction to be executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer 0, and Serial Port functions. The CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bit GF0 can be used to give an indication if an interrupt occurred during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

Power-down Mode

Entering Power-down Mode

To save maximum power, a Power-down mode can be invoked by software (refer to Table 3, PCON register).

In Power-down mode, the oscillator is stopped and the instruction that invoked Power-down mode is the last instruction executed. The internal RAM and SFRs retain their value until the Power-down mode is terminated. V_{CC} can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from Power-down. To properly terminate Power-down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

Only external interrupts $\overline{INT0}$ and $\overline{INT1}$ are useful to exit from Power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input.

Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 10. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and Power-Down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed.

Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put it into Power-down mode.

Exit from Power-down Mode

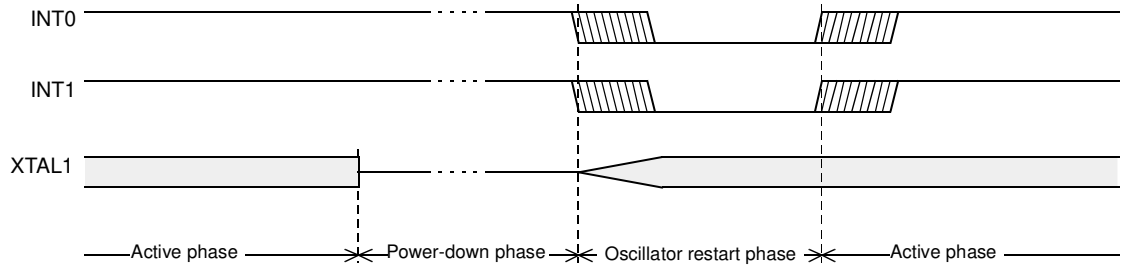
Exiting from Power-down by external interrupt does not affect the SFRs and the internal RAM content.

The ports status under Power-down is the status which was valid before entering this mode.

The INT1 interrupt is a multiplexed input (see Interrupt paragraph) with CPRES (Card detection) and Rxd (UART Rx). So these three inputs can be used to exit from Power-down mode. The configurations which must be set are detailed below:

- Rxd input:
  - RXEN (ISEL.0) must be set
  - EX1 (IE0.2) must be set
  - A low level detected during more than 100 microseconds exit from Power-down
- CPRES input:
  - PRSEN (ISEL.1) must be set
  - EX1 (IEO.2) must be set
  - EA (IE0.7) must be set
  - In the INT1 interrupt vector, the CPLEV Bit (ISEL.7) must be inverted and PRESIT Bit (ISEL.5) must be reset.

Figure 10. Power-down Exit Waveform



Exiting from Power-down by reset redefines all the SFRs, exiting from Power-down by external interrupt does no affect the SFRs.

Exiting from Power-down by either reset or external interrupt does not affect the internal RAM content.

Note: If idle mode is activated with Power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.

SCI Control

Prior to entering Power-down mode, a de-activation of the Smart Card system must be performed.

LED Control

Prior to entering Power-down mode, if the LED mode output is used, the medium pull-up must be disconnected by setting the LEDPD bit in the PCON Register (PCON 3).

Low Power Mode

Only in Power-down mode, in order to reduce the power consumption, the user can choose to select this low-power mode.

The activation reference is the following.

- First select the Low-power mode by setting the LP bit in the AUXR Register (AUXR. 6)
- The activation of Power-down can then be done.

Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated.

Only in case of PLCC52 version, in order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0 (See Table 4). As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

Power Modes Control Registers

Table 3. PCON Register

PCON (S:87h)
Power Configuration Register

7	6	5	4	3	2	1	0
SMOD1	**SMOD0**	**-**	**-**	**LEDPD**	**GF0**	**PD**	**IDL**

Bit Number	Bit Mnemonic	Description
7	SMOD1	**Double Baud Rate bit** Set to double the Baud Rate when Timer 1 is used and mode 1, 2 or 3 is selected in SCON register.
6	SMOD0	**SCON Select bit** When cleared, read/write accesses to SCON.7 are to SM0 bit and read/write accesses to SCON.6 are to SM1 bit. When set, read/write accesses to SCON.7 are to FE bit and read/write accesses to SCON.6 are to OVR bit. SCON is Serial Port Control register.
5		**Reserved**
4		**Reserved**
3	LEDPD	**LED Control Power-Down Mode bits** When cleaned the I/O pull-up is the standard C51 pull-up control. When set the medium pull-up is disconnected.
2	GF0	**General-purpose flag 0** One use is to indicate wether an interrupt occurred during normal operation or during Idle mode.
1	PD	**Power-down Mode bit** Cleared by hardware when an interrupt or reset occurs. Set to activate the Power-down mode. If IDL and PD are both set, PD takes precedence.
0	IDL	**Idle Mode bit** Cleared by hardware when an interrupt or reset occurs. Set to activate the Idle mode. If IDL and PD are both set, PD takes precedence.

Reset Value = X0XX XX00b

Table 4. AUXR Register

AUXR (S:8Eh)
Auxiliary Register

7	6	5	4	3	2	1	0
-	LP	-	-	-	-	EXTRAM	AO

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	LP	**Low Power mode selection** Clear to select standard mode Set to select low consumption mode
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	EXTRAM	**EXTRAM select** **(ONLY for PLCC52 version)** Clear to map XRAM datas in internal XRAM memory. Set to map XRAM datas in external XRAM memory.
0	AO	**ALE Output bit** **(ONLY for PLCC52 version)** Clear to restore ALE operation during internal fetches. Set to disable ALE operation during internal fetches.

Reset Value = 00XX XX00b

Table 5. IE0 Register

IE0
Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	**-**	**-**	**ES**	**ET1**	**EX1**	**ET0**	**EX0**

Bit Number	Bit Mnemonic	Description
7	EA	**Enable All interrupt bit** Clear to disable all interrupts. Set to enable all interrupts. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its interrupt enable bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	ES	**Serial port Enable bit** Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	**Timer 1 overflow interrupt Enable bit** Clear to disable Timer 1 overflow interrupt. Set to enable Timer 1 overflow interrupt.
2	EX1	**External interrupt 1 Enable bit** Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	**Timer 0 overflow interrupt Enable bit** Clear to disable Timer 0 overflow interrupt. Set to enable Timer 0 overflow interrupt.
0	EX0	**External interrupt 0 Enable bit** Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0XX0 0000b

Table 6. ISEL Register

ISEL (S:BAh)
Interrupt Enable Register

7	6	5	4	3	2	1	0
CPLEV	**-**	**RXIT**	**PRESIT**	**OELEV**	**OEEN**	**RXEN**	**PRESEN**

Bit Number	Bit Mnemonic	Description
7	CPLEV	**Card presence detection level** This bit indicates which CPRES level will bring about an interrupt Set this bit to indicate that Card Presence IT will appear if CPRES is at high level. Clear this bit to indicate that Card Presence IT will appear if CPRES is at low level.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	PRESIT	**Card presence detection interrupt flag** Set by hardware Must be cleared by software
4	RXIT	**Received data interrupt flag** Set by hardware Must be cleared by software
3	OELEV	**OE/INT1 signal active level** Set this bit to indicate that high level is active. Clear this bit to indicate that low level is active.
2	OEEN	**OE/INT1 interrupt disable bit** Clear to disable INT1 interrupt Set to enable INT1 interrupt
1	PRESEN	**Card presence detection interrupt enable bit** Clear to disable the card presence detection interrupt coming from SCIB. Set to enable the card presence detection interrupt coming from SCIB.
0	RXEN	**Received data Interrupt enable bit** Clear to disable the RxD interrupt. Set to enable the RxD interrupt

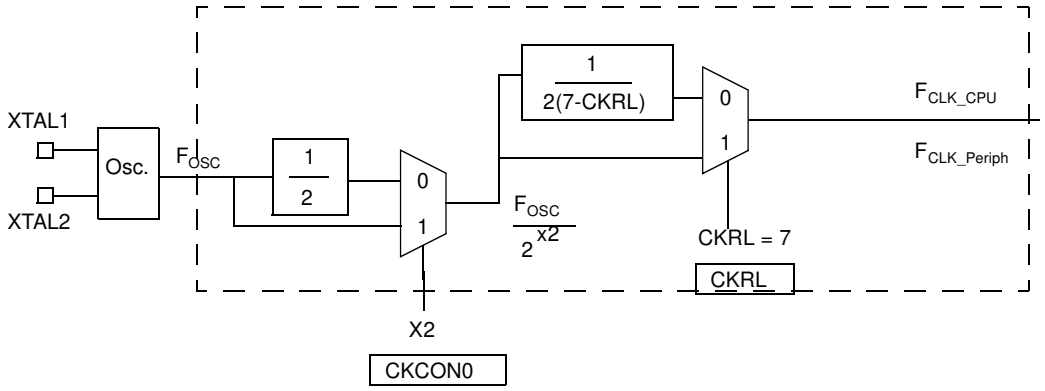
Reset Value = 0X00 0000b

Clock Management

In order to optimize the power consumption and the execution time needed for a specific task, an internal prescaler feature and a X2 feature have been implemented between the oscillator and the CPU.

Functional Block Diagram

Figure 11. Clock Generation Diagram



If CKRL<>7 then:

$$F_{CLK-CPU} = \frac{F_{OSC}}{2^{(x2)}} x \frac{1}{2(7-CKRL)}$$

If CKRL = 7 then:

$$F_{CLK-CPU} = \frac{Fosc}{2^{x2}}$$

CKRL	Prescalor Factor
7	1
6	2
5	4
4	6
3	8
2	10
1	12
0	14

X2 Feature

The T8xC5121 core needs only 6 clock periods per machine cycle. This feature called "X2" provides the following advantages:

- Divides frequency crystals by 2 (cheaper crystals) while keeping same CPU power.
- Saves power consumption while keeping same CPU power (oscillator power saving).
- Saves power consumption by dynamically dividing the operating frequency by 2 in operating and idle modes.
- Increases CPU power by 2 while keeping same crystal frequency.

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

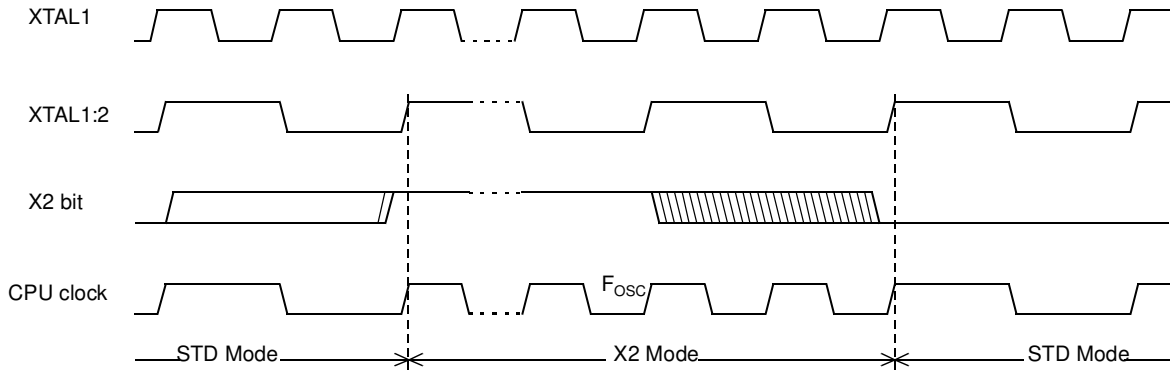
Description

The clock for the whole circuit and peripherals is first divided by two before being used by the CPU core and the peripherals.

This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio from 40 to 60%.

As shown in Figure 11, X2 bit is validated on the rising edge of the XTAL1÷2 to avoid glitches when switching from X2 to standard mode. Figure 12 shows the switching mode waveforms.

Figure 12. Mode Switching Waveforms



The X2 bit in the CKCON0 register (see Table 9) allows to switch (if CKRL=7) from 12 clock periods per instruction to 6 clock periods and vice versa.

The T0X2, T1X2, UartX2, and WdX2 bits in the CKCON0 register (see Table 9) and SCX2 bit in the CKCON1 register (see Table 10) allow to switch from standard peripheral speed (12 clock periods per peripheral clock cycle) to fast peripheral speed (6 clock periods per peripheral clock cycle). These bits are active only in X2 mode.

More information about the X2 mode can be found in the application note "How to Take Advantage of the X2 Features in TS80C51 Microcontroller?".

Clock Prescaler

Before supplying the CPU and the peripherals, the main clock is divided by a factor 2 to 30 to reduce the CPU power consumption. This factor is controlled with the CKRL register.

Table 7. Examples of Factors

XTAL (MHz)	X2 CPU CKCON0	CKRL Value	Prescaler Factor	F_{CLK_CPU}, F_{CLK_Periph} (MHz)
16	0 (reset mode)	07h	1	8
16	1 (X2 mode)	07h	1	16
16	1	07h	1	16
16	0	07h	1	8
16	0	06h	2	4
16	1	06h	2	8

Clock Control Registers

Clock Prescaler Register

This register is used to reload the clock prescaler of the CPU and peripheral clock.

Table 8. CKRL Register

CKRL - Clock Reload Register (97h)

7	6	5	4	3	2	1	0
-	-	-	-	CKRL	CKRL	CKRL	-

Bit Number	Bit Mnemonic	Description
7 - 4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3 - 1	CKRL	**Clock Reload Register** Prescaler value XXXX 000Xb: CKRL=7 and Division factor equals 14 XXXX 110Xb: CKRL=6 and factor equals 2 XXXX 111Xb: CKRL=7 and division factor equals 1
0	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.

Reset Value = XXXX 111Xb

Table 9. CKCON0 Register

CKCON0 - Clock Control Register (8Fh)

7	6	5	4	3	2	1	0
-	WDX2	-	SIX2	-	T1X2	T0X2	X2

Bit Number	Bit Mnemonic	Description
7	-	**Reserved**
6	WDX2	**Watchdog clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect) Cleared to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
5	-	**Reserved**
4	SIX2	**Enhanced UART clock (Mode 0 and 2)** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
3	-	**Reserved**
2	T1X2	**Timer 1 clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle
1	T0X2	**Timer 0 clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle
0	X2	**CPU clock** Clear to select 12 clock periods per machine cycle (Standard mode) for CPU and all the peripherals. Set to select 6 clock periods per machine cycle (X2 mode) and to enable the individual peripherals "X2" bits.

Reset Value = X0X0 X000b