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# Device Overview

The 89HPES32NT24AG2 is a member of the IDT family of PCI Express® switching solutions. The PES32NT24AG2 is a 32-lane, 24-port system interconnect switch optimized for PCI Express Gen2 packet switching in high-performance applications, supporting multiple simultaneous peer-to-peer traffic flows. Target applications include multi-host or intelligent I/O based systems where inter-domain communication is required, such as servers, storage, communications, and embedded systems.

# Features

◆ **High Performance Non-Blocking Switch Architecture**
 – 32-lane, 24-port PCIe switch with flexible port configuration
 – Integrated SerDes supports 5.0 GT/s Gen2 and 2.5 GT/s Gen1 operation
 – Delivers up to 32 GBps (256 Gbps) of switching capacity
 – Supports 128 Bytes to 2 KB maximum payload size
 – Low latency cut-through architecture
 – Supports one virtual channel and eight traffic classes

◆ **Port Configurability**
 – Four x8 stacks
  • Two x8 stacks, each configurable as:
   • One x8 port
   • Two x4 ports
   • Four x2 ports
   • Eight x1 ports
   • Several combinations of the above lane widths
  • Two x8 stacks, each configurable as:
   • One x8 port
   • Two x4 ports
   • Four x2 ports
   • Several combinations of the above lane widths
 – Automatic per port link width negotiation
  (x8 → x4 → x2 → x1)
 – Crosslink support
 – Automatic lane reversal
 – Per lane SerDes configuration
  • De-emphasis
  • Receive equalization
  • Drive strength

◆ **Innovative Switch Partitioning Feature**
 – Supports up to 8 fully independent switch partitions
 – Logically independent switches in the same device
 – Configurable downstream port device numbering
 – Supports dynamic reconfiguration of switch partitions

 • Dynamic port reconfiguration — downstream, upstream, non-transparent bridge
 • Dynamic migration of ports between partitions
 • Movable upstream port within and between switch partitions

◆ **Non-Transparent Bridging (NTB) Support**
 – Supports up to 8 NT endpoints per switch, each endpoint can communicate with other switch partitions or external PCIe domains or CPUs
 – 6 BARs per NT Endpoint
  • Bar address translation
  • All BARs support 32/64-bit base and limit address translation
  • Two BARs (BAR2 and BAR4) support look-up table based address translation
 – 32 inbound and outbound doorbell registers
 – 4 inbound and outbound message registers
 – Supports up to 64 masters
 – Unlimited number of outstanding transactions

◆ **Multicast**
 – Compliant with the PCI-SIG multicast
 – Supports 64 multicast groups
 – Supports multicast across non-transparent port
 – Multicast overlay mechanism support
 – ECRC regeneration support

◆ **Integrated Direct Memory Access (DMA) Controllers**
 – Supports up to 2 DMA upstream ports, each with 2 DMA channels
 – Supports 32-bit and 64-bit memory-to-memory transfers
  • Fly-by translation provides reduced latency and increased performance over buffered approach
  • Supports arbitrary source and destination address alignment
  • Supports intra- as well as inter-partition data transfers using the non-transparent endpoint
 – Supports DMA transfers to multicast groups
 – Linked list descriptor-based operation
 – Flexible addressing modes
  • Linear addressing
  • Constant addressing

◆ **Quality of Service (QoS)**
 – Port arbitration
  • Round robin
 – Request metering
  • IDT proprietary feature that balances bandwidth among switch ports for maximum system throughput

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– High performance switch core architecture
  • Combined Input Output Queued (CIOQ) switch architecture with large buffers

◆ **Clocking**
– Supports 100 MHz and 125 MHz reference clock frequencies
– Flexible port clocking modes
  • Common clock
  • Non-common clock
  • Local port clock with SSC (spread spectrum setting) and port reference clock input

◆ **Hot-Plug and Hot Swap**
– Hot-plug controller on all ports
  • Hot-plug supported on all downstream switch ports
– All ports support hot-plug using low-cost external I$^2$C I/O expanders
– Configurable presence-detect supports card and cable applications
– GPE output pin for hot-plug event notification
  • Enables SCI/SMI generation for legacy operating system support
– Hot-swap capable I/O

◆ **Power Management**
– Supports D0, D3hot and D3 power management states
– Active State Power Management (ASPM)
  • Supports L0, L0s, L1, L2/L3 Ready, and L3 link states
  • Configurable L0s and L1 entry timers allow performance/power-savings tuning
– SerDes power savings
  • Supports low swing / half-swing SerDes operation
  • SerDes associated with unused ports are turned off
  • SerDes associated with unused lanes are placed in a low power state

◆ **Reliability, Availability, and Serviceability (RAS)**
– ECRC support
– AER on all ports
– SECDED ECC protection on all internal RAMs
– End-to-end data path parity protection
– Checksum Serial EEPROM content protected
– Ability to generate an interrupt (INTx or MSI) on link up/down transitions

◆ **Initialization / Configuration**
– Supports Root (BIOS, OS, or driver), Serial EEPROM, or SMBus switch initialization
– Common switch configurations are supported with pin strapping (no external components)
– Supports in-system Serial EEPROM initialization/programming

◆ **On-Die Temperature Sensor**
– Range of 0 to 127.5 degrees Celsius
– Three programmable temperature thresholds with over and under temperature threshold alarms
– Automatic recording of maximum high or minimum low temperature

◆ **9 General Purpose I/O**

◆ **Test and Debug**
– Ability to inject AER errors simplifies in system error handling software validation
– On-chip link activity and status outputs available for several ports
– Per port link activity and status outputs available using external I$^2$C I/O expander for all remaining ports
– Supports IEEE 1149.6 AC JTAG and IEEE 1149.1 JTAG

◆ **Standards and Compatibility**
– PCI Express Base Specification 2.1 compliant
– Implements the following optional PCI Express features
  • Advanced Error Reporting (AER) on all ports
  • End-to-End CRC (ECRC)
  • Access Control Services (ACS)
  • Device Serial Number Enhanced Capability
  • Sub-System ID and Sub-System Vendor ID Capability
  • Internal Error Reporting
  • Multicast
  • VGA and ISA enable
  • L0s and L1 ASPM
  • ARI

◆ **Power Supplies**
– Requires three power supply voltages (1.0V, 2.5V, and 3.3V)

◆ **Packaged in a 23mm x 23mm 484-ball Flip Chip BGA with 1mm ball spacing**

## Product Description

With Non-Transparent Bridging functionality and innovative Switch Partitioning feature, the PES32NT24AG2 allows true multi-host or multi-processor communications in a single device. Integrated DMA controllers enable high-performance system design by off-loading data transfer operations across memories from the processors. Each lane is capable of 5 GT/s link speed in both directions and is fully compliant with PCI Express Base Specification 2.1.

A non-transparent bridge (NTB) is required when two PCI Express domains need to communicate to each other. The main function of the NTB block is to initialize and translate addresses and device IDs to allow data exchange across PCI Express domains. The major functionalities of the NTB block are summarized in Table 1.
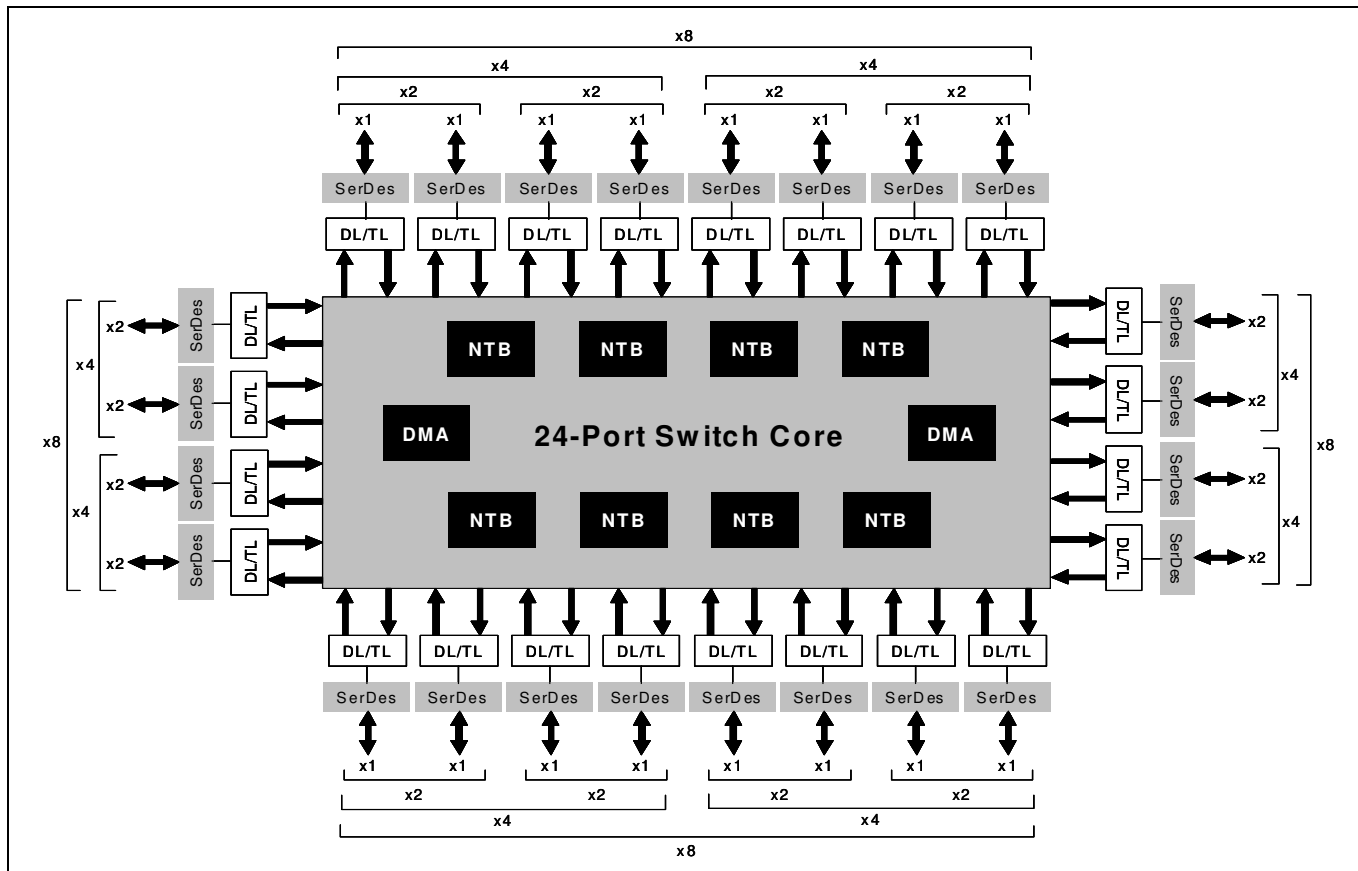
# Block Diagram



Figure 1  PES32NT24AG2 Block Diagram

| Function | Number | Description |
|---|---|---|
| NTB ports | Up to 8 | Each device can be configured to have up to 8 NTB functions and can support up to 8 CPUs/roots. |
| Mapping table entries | Up to 64 for entire device | Each device can have up to 64 masters ID for address and ID translations. |
| Mapping windows | Six 32-bits or three 64-bits | Each NT port has six BARs, where each BAR opening an NT window to another domain. |
| Address translation | Direct-address and lookup table trans-lations | Lookup-table translation divides the BAR aperture into up to 24 segments, where each segment has independent translation programming and is associated with an entry in a look-up table. |
| Doorbell registers | 32 bits | Doorbell register is used for event signaling between domains, where an outbound doorbell bit sets a corresponding bit at the inbound doorbell in the other domain. |
| Message registers | 4 inbound and out-bound registers of 32-bits | Message registers allow mailbox message passing between domains -- message placed in the inbound register will be seen at the outbound register at the other domain. |

Table 1  Non-Transparent Bridge Function Summary

### SMBus Interface

The PES32NT24AG2 contains two SMBus interfaces. The slave interface provides full access to the configuration registers in the PES32NT24AG2, allowing every configuration register in the device to be read or written by an external agent. The master interface allows the default configuration register values of the PES32NT24AG2 to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander.

Each of the two SMBus interfaces contain an SMBus clock pin and an SMBus data pin. In addition, the slave SMBus has SSMBADDR1 and SSMBADDR2 pins. As shown in Figure 2, the master and slave SMBuses may only be used in a split configuration. In the split configuration, the master and slave SMBuses operate as two independent buses; thus, multi-master arbitration is not required. The SMBus master interface does not support SMBus arbitration. As a result, the switch's SMBus master must be the only master in the SMBus lines that connect to the serial EEPROM and I/O expander slaves.
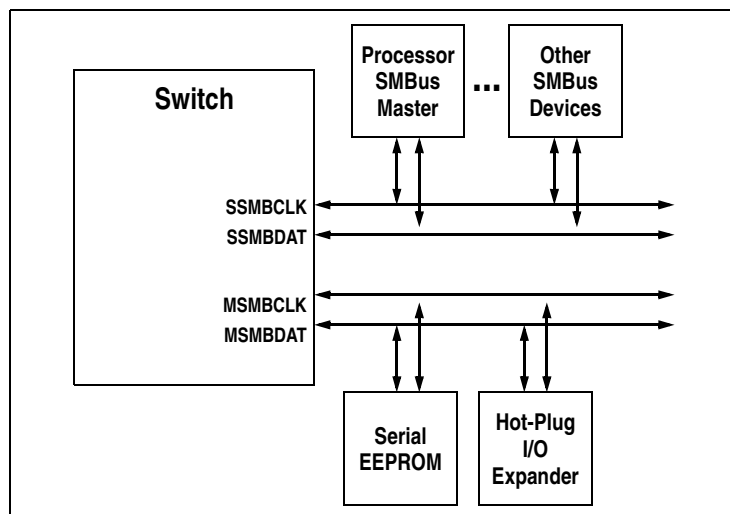
**Figure 2  Split SMBus Interface Configuration**

### Hot-Plug Interface

The PES32NT24AG2 supports PCI Express Hot-Plug on each downstream port (ports 1 through 23). To reduce the number of pins required on the device, the PES32NT24AG2 utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES32NT24AG2 generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES32NT24AG2. In response to an I/O expander interrupt, the PES32NT24AG2 generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

### General Purpose Input/Output

The PES32NT24AG2 provides 9 General Purpose I/O (GPIO) pins that may be individually configured as general purpose inputs, general purpose outputs, or alternate functions. All GPIO pins are shared with other on-chip functions. These alternate functions may be enabled via software, SMBus slave interface, or serial configuration EEPROM.

## Pin Description

The following tables list the functions of the pins provided on the PES32NT24AG2. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an "N" are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level. Differential signals end with a suffix "N" or "P." The differential signal ending in "P" is the positive portion of the differential pair and the differential signal ending in "N" is the negative portion of the differential pair.

| Signal | Type | Name/Description |
|---|---|---|
| PE00RN[1:0]<br>PE00RP[1:0] | I | **PCI Express Port 0 Serial Data Receive.** Differential PCI Express receive pairs for port 0. |
| PE00TN[1:0]<br>PE00TP[1:0] | O | **PCI Express Port 0 Serial Data Transmit.** Differential PCI Express transmit pairs for port 0. |
| PE01RN[1:0]<br>PE01RP[1:0] | I | **PCI Express Port 1 Serial Data Receive.** Differential PCI Express receive pairs for port 1. |
| PE01TN[1:0]<br>PE01TP[1:0] | O | **PCI Express Port 1 Serial Data Transmit.** Differential PCI Express transmit pairs for port 1. |
| PE02RN[1:0]<br>PE02RP[1:0] | I | **PCI Express Port 2 Serial Data Receive.** Differential PCI Express receive pairs for port 2. |
| PE02TN[1:0]<br>PE02TP[1:0] | O | **PCI Express Port 2 Serial Data Transmit.** Differential PCI Express transmit pairs for port 2. |
| PE03RN[1:0]<br>PE03RP[1:0] | I | **PCI Express Port 3 Serial Data Receive.** Differential PCI Express receive pairs for port 3. |
| PE03TN[1:0]<br>PE03TP[1:0] | O | **PCI Express Port 3 Serial Data Transmit.** Differential PCI Express transmit pairs for port 3. |
| PE04RN[1:0]<br>PE04RP[1:0] | I | **PCI Express Port 4 Serial Data Receive.** Differential PCI Express receive pairs for port 4. |
| PE04TN[1:0]<br>PE04TP[1:0] | O | **PCI Express Port 4 Serial Data Transmit.** Differential PCI Express transmit pairs for port 4. |
| PE05RN[1:0]<br>PE05RP[1:0] | I | **PCI Express Port 5 Serial Data Receive.** Differential PCI Express receive pairs for port 5. |
| PE05TN[1:0]<br>PE05TP[1:0] | O | **PCI Express Port 5 Serial Data Transmit.** Differential PCI Express transmit pairs for port 5. |
| PE06RN[1:0]<br>PE06RP[1:0] | I | **PCI Express Port 6 Serial Data Receive.** Differential PCI Express receive pairs for port 6. |
| PE06TN[1:0]<br>PE06TP[1:0] | O | **PCI Express Port 6 Serial Data Transmit.** Differential PCI Express transmit pairs for port 6. |
| PE07RN[1:0]<br>PE07RP[1:0] | I | **PCI Express Port 7 Serial Data Receive.** Differential PCI Express receive pairs for port 7. |
| PE07TN[1:0]<br>PE07TP[1:0] | O | **PCI Express Port 7 Serial Data Transmit.** Differential PCI Express transmit pairs for port 7. |
| PE08RN[0]<br>PE08RP[0] | I | **PCI Express Port 8 Serial Data Receive.** Differential PCI Express receive pair for port 8. |
| PE08TN[0]<br>PE08TP[0] | O | **PCI Express Port 8 Serial Data Transmit.** Differential PCI Express transmit pair for port 8. |
| PE09RN[0]<br>PE09RP[0] | I | **PCI Express Port 9 Serial Data Receive.** Differential PCI Express receive pair for port 9. |
| PE09TN[[0]<br>PE09TP[0] | O | **PCI Express Port 9 Serial Data Transmit.** Differential PCI Express transmit pair for port 9. |
| PE10RN[0]<br>PE10RP[0] | I | **PCI Express Port 10 Serial Data Receive.** Differential PCI Express receive pair for port 10. |

**Table 2 PCI Express Interface Pins (Part 1 of 3)**

| Signal | Type | Name/Description |
|--------|------|------------------|
| PE10TN[0]<br>PE10TP[0] | O | **PCI Express Port 10 Serial Data Transmit.** Differential PCI Express transmit pair for port 10. |
| PE11RN[0]<br>PE11RP[0] | I | **PCI Express Port 11 Serial Data Receive.** Differential PCI Express receive pair for port 11. |
| PE11TN[0]<br>PE11TP[0] | O | **PCI Express Port 11 Serial Data Transmit.** Differential PCI Express transmit pair for port 11. |
| PE12RN[0]<br>PE12RP[0] | I | **PCI Express Port 12 Serial Data Receive.** Differential PCI Express receive pair for port 12. |
| PE12TN[0]<br>PE12TP[0] | O | **PCI Express Port 12 Serial Data Transmit.** Differential PCI Express transmit pair for port 12. |
| PE13RN[0]<br>PE13RP[0] | I | **PCI Express Port 13 Serial Data Receive.** Differential PCI Express receive pair for port 13. |
| PE13TN[0]<br>PE13TP[0] | O | **PCI Express Port 13 Serial Data Transmit.** Differential PCI Express transmit pair for port 13. W |
| PE14RN[0]<br>PE14RP[0] | I | **PCI Express Port 14 Serial Data Receive.** Differential PCI Express receive pair for port 14. |
| PE14TN[0]<br>PE14TP[0] | O | **PCI Express Port 14 Serial Data Transmit.** Differential PCI Express transmit pair for port 14. |
| PE15RN[0]<br>PE15RP[0] | I | **PCI Express Port 15 Serial Data Receive.** Differential PCI Express receive pair for port 15. |
| PE15TN[0]<br>PE15TP[0] | O | **PCI Express Port 15 Serial Data Transmit.** Differential PCI Express transmit pair for port 15. |
| PE16RN[0]<br>PE16RP[0] | I | **PCI Express Port 16 Serial Data Receive.** Differential PCI Express receive pair for port 16. |
| PE16TN[0]<br>PE16TP[0] | O | **PCI Express Port 16 Serial Data Transmit.** Differential PCI Express transmit pair for port 16. |
| PE17RN[0]<br>PE17RP[0] | I | **PCI Express Port 17 Serial Data Receive.** Differential PCI Express receive pair for port 17. |
| PE17TN[0]<br>PE17TP[0] | O | **PCI Express Port 17 Serial Data Transmit.** Differential PCI Express transmit pair for port 17. |
| PE18RN[0]<br>PE18RP[0] | I | **PCI Express Port 18 Serial Data Receive.** Differential PCI Express receive pair for port 18. |
| PE18TN[0]<br>PE18TP[0] | O | **PCI Express Port 18 Serial Data Transmit.** Differential PCI Express transmit pair for port 18. |
| PE19RN[0]<br>PE19RP[0] | I | **PCI Express Port 19 Serial Data Receive.** Differential PCI Express receive pair for port 19. |
| PE19TN[0]<br>PE19TP[0] | O | **PCI Express Port 19 Serial Data Transmit.** Differential PCI Express transmit pair for port 19. |
| PE20RN[0]<br>PE20RP[0] | I | **PCI Express Port 20 Serial Data Receive.** Differential PCI Express receive pair for port 20. |
| PE20TN[0]<br>PE20TP[0] | O | **PCI Express Port 20 Serial Data Transmit.** Differential PCI Express transmit pair for port 20. |
| PE21RN[0]<br>PE21RP[0] | I | **PCI Express Port 21 Serial Data Receive.** Differential PCI Express receive pair for port 21. |

**Table 2  PCI Express Interface Pins  (Part 2 of 3)**

| Signal | Type | Name/Description |
|---|---|---|
| PE21TN[0]<br>PE21TP[0] | O | **PCI Express Port 21 Serial Data Transmit.** Differential PCI Express transmit pair for port 21. |
| PE22RN[0]<br>PE22RP[0] | I | **PCI Express Port 22 Serial Data Receive.** Differential PCI Express receive pair for port 22. |
| PE22TN[0]<br>PE22TP[0] | O | **PCI Express Port 22 Serial Data Transmit.** Differential PCI Express transmit pair for port 22. |
| PE23RN[0]<br>PE23RP[0] | I | **PCI Express Port 23 Serial Data Receive.** Differential PCI Express receive pair for port 23. |
| PE23TN[0]<br>PE23TP[0] | O | **PCI Express Port 23 Serial Data Transmit.** Differential PCI Express transmit pair for port 23. |

**Table 2  PCI Express Interface Pins  (Part 3 of 3)**

| Signal | Type | Name/Description |
|---|---|---|
| GCLKN[1:0]<br>GCLKP[1:0] | I | **Global Reference Clock.** Differential reference clock input pairs. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic. The frequency of the differential reference clock is determined by the GCLKFSEL signal.<br>Note: Both pairs of the Global Reference Clocks must be connected to and derived from the same clock source. Refer to the Overview section of Chapter 2 in the PES32NT24xG2 User Manual for additional details. |
| P00CLKN<br>P00CLKP | I | **Port Reference Clock**. Differential reference clock pair associated with port 0. |
| P02CLKN<br>P02CLKP | I | **Port Reference Clock**. Differential reference clock pair associated with port 2. |
| P04CLKN<br>P04CLKP | I | **Port Reference Clock**. Differential reference clock pair associated with port 4. |
| P06CLKN<br>P06CLKP | I | **Port Reference Clock**. Differential reference clock pair associated with port 6. |
| P08CLKN<br>P08CLKP | I | **Port Reference Clock**. Differential reference clock pair associated with port 8. |
| P12CLKN<br>P12CLKP | I | **Port Reference Clock**. Differential reference clock pair associated with port 12. |
| P16CLKN<br>P16CLKP | I | **Port Reference Clock**. Differential reference clock pair associated with port 16. |
| P20CLKN<br>P20CLKP | I | **Port Reference Clock**. Differential reference clock pair associated with port 20. |

**Table 3  Reference Clock Pins**

| Signal | Type | Name/Description |
|--------|------|-----------------|
| MSMBCLK | I/O | **Master SMBus Clock.** This bidirectional signal is used to synchronize transfers on the master SMBus. It is active and generating the clock only when the EEPROM or I/O Expanders are being accessed. |
| MSMBDAT | I/O | **Master SMBus Data.** This bidirectional signal is used for data on the master SMBus. |
| SSMBADDR[2,1] | I | **Slave SMBus Address.** These pins determine the SMBus address to which the slave SMBus interface responds. |
| SSMBCLK | I/O | **Slave SMBus Clock.** This bidirectional signal is used to synchronize transfers on the slave SMBus. |
| SSMBDAT | I/O | **Slave SMBus Data.** This bidirectional signal is used for data on the slave SMBus. |

**Table 4  SMBus Interface Pins**

| Signal | Type | Name/Description |
|--------|------|-----------------|
| GPIO[0] | I/O | General Purpose I/O.<br>This pin can be configured as a general purpose I/O pin.<br>1st Alternate function pin name: PART0PERSTN<br>1st Alternate function pin type: Input/Output<br>1st Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.<br>2nd Alternate function pin name: P16LINKUPN<br>2nd Alternate function pin type: Output<br>2nd Alternate function: Port 16 Link Up Status output. |
| GPIO[1] | I/O | General Purpose I/O.<br>This pin can be configured as a general purpose I/O pin.<br>1st Alternate function pin name: PART1PERSTN<br>1st Alternate function pin type: Input/Output<br>1st Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.<br>2nd Alternate function pin name: P16ACTIVEN<br>2nd Alternate function pin type: Output<br>2nd Alternate function: Port 16 Link Active Status Output. |
| GPIO[2] | I/O | General Purpose I/O.<br>This pin can be configured as a general purpose I/O pin.<br>1st Alternate function pin name: PART2PERSTN<br>1st Alternate function pin type: Input/Output<br>1st Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.<br>2nd Alternate function pin name: P4LINKUPN<br>2nd Alternate function pin type: Output<br>2nd Alternate function: Port 4 Link Up Status output. |
| GPIO[3] | I/O | General Purpose I/O.<br>This pin can be configured as a general purpose I/O pin.<br>1st Alternate function pin name: PART3PERSTN<br>1st Alternate function pin type: Input/Output<br>1st Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.<br>2nd Alternate function pin name: P4ACTIVEN<br>2nd Alternate function pin type: Output<br>2nd Alternate function: Port 4 Link Active Status Output. |

**Table 5  General Purpose I/O Pins  (Part 1 of 2)**

| Signal | Type | Name/Description |
|--------|------|------------------|
| GPIO[4] | I/O | General Purpose I/O.<br>This pin can be configured as a general purpose I/O pin.<br>1st Alternate function pin name: FAILOVER0<br>1st Alternate function pin type: Input<br>1st Alternate function: When this signal changes state and the corresponding failover capability is enabled, a failover event is signaled.<br>2nd Alternate function pin name: P0LINKUPN<br>2nd Alternate function pin type: Output<br>2nd Alternate function: Port 0 Link Up Status output. |
| GPIO[5] | I/O | General Purpose I/O.<br>This pin can be configured as a general purpose I/O pin.<br>1st Alternate function pin name: GPEN<br>1st Alternate function pin type: Output<br>1st Alternate function: Hot-plug general purpose even output.<br>2nd Alternate function pin name: P0ACTIVEN<br>2nd Alternate function pin type: Output<br>2nd Alternate function: Port 0 Link Active Status Output. |
| GPIO[6] | I/O | General Purpose I/O.<br>This pin can be configured as a general purpose I/O pin.<br>1st Alternate function pin name: FAILOVER1<br>1st Alternate function pin type: Input<br>1st Alternate function: When this signal changes state and the corresponding failover capability is enabled, a failover event is signaled.<br>2nd Alternate function pin name: FAILOVER3<br>2nd Alternate function pin type: Input<br>2nd Alternate function: When this signal changes state and the corresponding failover capability is enabled, a failover event is signaled. |
| GPIO[7] | I/O | General Purpose I/O.<br>This pin can be configured as a general purpose I/O pin.<br>1st Alternate function pin name: FAILOVER2<br>1st Alternate function pin type: Input<br>1st Alternate function: When this signal changes state and the corresponding failover capability is enabled, a failover event is signaled.<br>2nd Alternate function pin name: P8LINKUPN<br>2nd Alternate function pin type: Output<br>2nd Alternate function: Port 8 Link Up Status output. |
| GPIO[8] | I/O | General Purpose I/O.<br>This pin can be configured as a general purpose I/O pin.<br>1st Alternate function pin name: IOEXPINTN<br>1st Alternate function pin type: Input<br>1st Alternate function: IO expander interrupt.<br>2nd Alternate function pin name: P8ACTIVEN<br>2nd Alternate function pin type: Output<br>2nd Alternate function: Port 8 Link Active Status Output. |

**Table 5  General Purpose I/O Pins  (Part 2 of 2)**

| Signal | Type | Name/Description |
|---|---|---|
| STK0CFG[1:0] | I | **Stack 0 Configuration.** These pins select the configuration of stack 0. |
| STK1CFG[1:0] | I | **Stack 1 Configuration.** These pins select the configuration of stack 1. |
| STK2CFG[4:0] | I | **Stack 2 Configuration.** These pins select the configuration of stack 2. |
| STK3CFG[4:0] | I | **Stack 3 Configuration.** These pins select the configuration of stack 3. |

**Table 6  Stack Configuration Pins**

| Signal | Type | Name/Description |
|---|---|---|
| CLKMODE[1:0] | I | **Clock Mode.** These signals determine the port clocking mode used by ports of the device. |
| GCLKFSEL | I | **Global Clock Frequency Select.** These signals select the frequency of the GCLKP and GCLKN signals.<br>0x0 100 MHz<br>0x1 125 MHz |
| PERSTN | I | **Fundamental Reset.** Assertion of this signal resets all logic inside the device. |
| RSTHALT | I | **Reset Halt.** When this signal is asserted during a switch fundamental reset sequence, the switch remains in a quasi-reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the quasi-reset state when the RSTHALT bit is cleared in the SWCTL register by an SMBus master. |
| SWMODE[3:0] | I | **Switch Mode.** These configuration pins determine the switch operating mode.<br> These pins should be static and not change following the negation of PERSTN.<br>0x0 - Single partition<br>0x1 - Single partition with Serial EEPROM initialization<br>0x2 - Single partition with Serial EEPROM Jump 0 initialization<br>0x3 - Single partition with Serial EEPROM Jump 1 initialization<br>0x4 through 0x7 - Reserved<br>0x8 - Single partition with reduced latency<br>0x9 - Single partition with Serial EEPROM initialization and reduced latency<br>0xA - Multi-partition with Unattached ports<br>0xB - Multi-partition with Unattached ports and I$^2$C Reset<br>0xC - Multi-partition with Unattached ports and Serial EEPROM initialization<br>0xD - Multi-partition with Unattached ports with I$^2$C Reset and Serial EEPROM initialization<br>0xE - Multi-partition with Disabled ports<br>0xF - Multi-partition with Disabled ports and Serial EEPROM initialization |

**Table 7  System Pins**

| Signal | Type | Name/Description |
|--------|------|------------------|
| JTAG_TCK | I | **JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle. |
| JTAG_TDI | I | **JTAG Data Input**. This is the serial data input to the boundary scan logic or JTAG Controller. |
| JTAG_TDO | O | **JTAG Data Output**. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated. |
| JTAG_TMS | I | **JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller. |
| JTAG_TRST_N | I | **JTAG Reset**. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur:<br>1) actively drive this signal low with control logic<br>2) statically drive this signal low with an external pull-down on the board |

**Table 8  Test Pins**

| Signal | Type | Name/Description |
|--------|------|------------------|
| REFRES[7:0] | — | **External Reference Resistor.** Reference for the corresponding SerDes bias currents and PLL calibration circuitry. A 3K Ohm +/- 1% resistor should be connected from this pin to ground and isolated from any source of noise injection. Each bit of this signal corresponds to a SerDes quad, e.g., REFRES[5] is the reference resistor for SerDes quad 5. |
| REFRESPLL | — | **PLL External Reference Resistor.** Provides a reference for the PLL bias currents and PLL calibration circuitry. A 3K Ohm +/- 1% resistor should be connected from this pin to ground and isolated from any source of noise injection. |
| $V_{DD}CORE$ | — | **Core $V_{DD}$.** Power supply for core logic (1.0V). |
| $V_{DD}I/O$ | — | **I/O $V_{DD}$.** LVTTL I/O buffer power supply (3.3V). |
| $V_{DD}PEA$ | — | **PCI Express Analog Power.** Serdes analog power supply (1.0V). |
| $V_{DD}PEHA$ | — | **PCI Express Analog High Power.** Serdes analog power supply (2.5V). |
| $V_{DD}PETA$ | — | **PCI Express Transmitter Analog Voltage.** Serdes transmitter analog power supply (1.0V). |
| $V_{SS}$ | — | **Ground.** |

**Table 9  Power, Ground, and SerDes Resistor Pins**

# Pin Characteristics

**Note:** Some input pads of the switch do not contain internal pull-ups or pull-downs. Unused SMBus and System inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, floating pins can cause a slight increase in power consumption. Unused Serdes (Rx and Tx) pins should be left floating. Finally, No Connection pins should not be connected.

| Function | Pin Name | Type | Buffer | I/O Type | Internal Resistor[1] | Notes |
|---|---|---|---|---|---|---|
| PCI Express Interface | PE00RN[1:0] | I | PCIe differential[2] | Serial Link | | Note: Unused SerDes pins can be left floating |
| | PE00RP[1:0] | I | | | | |
| | PE00TN[1:0] | O | | | | |
| | PE00TP[1:0] | O | | | | |
| | PE01RN[1:0] | I | | | | |
| | PE01RP[1:0] | I | | | | |
| | PE01TN[1:0] | O | | | | |
| | PE01TP[1:0] | O | | | | |
| | PE02RN[1:0] | I | | | | |
| | PE02RP[1:0] | I | | | | |
| | PE02TN[1:0] | O | | | | |
| | PE02TP[1:0] | O | | | | |
| | PE03RN[1:0] | I | | | | |
| | PE03RP[1:0] | I | | | | |
| | PE03TN[1:0] | O | | | | |
| | PE03TP[1:0] | O | | | | |
| | PE04RN[1:0] | I | | | | |
| | PE04RP[1:0] | I | | | | |
| | PE04TN[1:0] | O | | | | |
| | PE04TP[1:0] | O | | | | |
| | PE05RN[1:0] | I | | | | |
| | PE05RP[1:0] | I | | | | |
| | PE05TN[1:0] | O | | | | |
| | PE05TP[1:0] | O | | | | |
| | PE06RN[1:0] | I | | | | |
| | PE06RP[1:0] | I | | | | |
| | PE06TN[1:0] | O | | | | |
| | PE06TP[1:0] | O | | | | |
| | PE07RN[1:0] | I | | | | |
| | PE07RP[1:0] | I | | | | |
| | PE07TN[1:0] | O | | | | |
| | PE07TP[1:0] | O | | | | |
| | PE08RN[0] | I | | | | |
| | PE08RP[0] | I | | | | |
| | PE08TN[0] | O | | | | |

**Table 10  Pin Characteristics  (Part 1 of 5)**

| Function | Pin Name | Type | Buffer | I/O Type | Internal Resistor[1] | Notes |
|---|---|---|---|---|---|---|
| PCI Express Interface (cont.) | PE08TP[0] | O | PCIe differential | Serial Link | | |
| | PE09RN[0] | I | | | | |
| | PE09RP[0] | I | | | | |
| | PE09TN[0] | O | | | | |
| | PE09TP[0] | O | | | | |
| | PE10RN[0] | I | | | | |
| | PE10RP[0] | I | | | | |
| | PE10TN[0] | O | | | | |
| | PE10TP[0] | O | | | | |
| | PE11RN[0] | I | | | | |
| | PE11RP[0] | I | | | | |
| | PE11TN[0] | O | | | | |
| | PE11TP[0] | O | | | | |
| | PE12RN[0] | I | | | | |
| | PE12RP[0] | I | | | | |
| | PE12TN[0] | O | | | | |
| | PE12TP[0] | O | | | | |
| | PE13RN[0] | I | | | | |
| | PE13RP[0] | I | | | | |
| | PE13TN[0] | O | | | | |
| | PE13TP[0] | O | | | | |
| | PE14RN[0] | I | | | | |
| | PE14RP[0] | I | | | | |
| | PE14TN[0] | O | | | | |
| | PE14TP[0] | O | | | | |
| | PE15RN[0] | I | | | | |
| | PE15RP[0] | I | | | | |
| | PE15TN[0] | O | | | | |
| | PE15TP[0] | O | | | | |
| | PE16RN[0] | I | | | | |
| | PE16RP[0] | I | | | | |
| | PE16TN[0] | O | | | | |
| | PE16TP[0] | O | | | | |
| | PE17RN[0] | I | | | | |
| | PE17RP[0] | I | | | | |
| | PE17TN[0] | O | | | | |
| | PE17TP[0] | O | | | | |

**Table 10  Pin Characteristics  (Part 2 of 5)**

| Function | Pin Name | Type | Buffer | I/O Type | Internal Resistor[1] | Notes |
|----------|----------|------|--------|----------|---------------------|-------|
| PCI Express Interface (cont.) | PE18RN[0] | I | PCIe differential | Serial Link | | |
| | PE18RP[0] | I | | | | |
| | PE18TN[0] | O | | | | |
| | PE18TP[0] | O | | | | |
| | PE19RN[0] | I | | | | |
| | PE19RP[0] | I | | | | |
| | PE19TN[0] | O | | | | |
| | PE19TP[0] | O | | | | |
| | PE20RN[0] | I | | | | |
| | PE20RP[0] | I | | | | |
| | PE20TN[0] | O | | | | |
| | PE20TP[0] | O | | | | |
| | PE21RN[0] | I | | | | |
| | PE21RP[0] | I | | | | |
| | PE21TN[0] | O | | | | |
| | PE21TP[0] | O | | | | |
| | PE22RN[0] | I | | | | |
| | PE22RP[0] | I | | | | |
| | PE22TN[0] | O | | | | |
| | PE22TP[0] | O | | | | |
| | PE23RN[0] | I | | | | |
| | PE23RP[0] | I | | | | |
| | PE23TN[0] | O | | | | |
| | PE23TP[0] | O | | | | |

**Table 10  Pin Characteristics  (Part 3 of 5)**

| Function | Pin Name | Type | Buffer | I/O Type | Internal Resistor[1] | Notes |
|---|---|---|---|---|---|---|
| Reference Clocks | GCLKN[1:0] | I | HCSL | Diff. Clock Input | | Refer to Table 11 |
| | GCLKP[1:0] | I | | | | |
| | P00CLKN | I | | | | Note: Unused port clock pins should be connected to Vss on the board. |
| | P00CLKP | I | | | | |
| | P02CLKN | I | | | | |
| | P02CLKP | I | | | | |
| | P04CLKN | I | | | | |
| | P04CLKP | I | | | | |
| | P06CLKN | I | | | | |
| | P06CLKP | I | | | | |
| | P08CLKN | I | | | | |
| | P08CLKP | I | | | | |
| | P12CLKN | I | | | | |
| | P12CLKP | I | | | | |
| | P16CLKN | I | | | | |
| | P16CLKP | I | | | | |
| | P20CLKN | I | | | | |
| | P20CLKP | I | | | | |
| SMBus | MSMBCLK | I/O | LVTTL | STI[3] | | Note: When unused, these signals must be pulled up on the board using an external resistor or current source in accordance with the SMBus specification. |
| | MSMBDAT | I/O | | STI | | |
| | SSMBADDR[2,1] | I | | | pull-up | |
| | SSMBCLK | I/O | | STI | | Note: When unused, these signals must be pulled up on the board using an external resistor or current source in accordance with the SMBus specification. |
| | SSMBDAT | I/O | | STI | | |
| General Purpose I/O | GPIO[8:0] | I/O | LVTTL | STI, High Drive | pull-up | Unused pins can be left floating. |
| Stack Configuration | STK0CFG[1:0] | I | LVTTL | Input | pull-down | Unused pins can be left floating. |
| | STK1CFG[1:0] | I | | | pull-down | |
| | STK2CFG[4:0] | I | | | pull-down | |
| | STK3CFG[4:0] | I | | | pull-down | |

**Table 10  Pin Characteristics  (Part 4 of 5)**

| Function | Pin Name | Type | Buffer | I/O Type | Internal Resistor[1] | Notes |
|----------|----------|------|--------|----------|----------------------|-------|
| System Pins | CLKMODE[1:0] | I | LVTTL | Input | pull-up | Unused pins can be left floating. |
| | GCLKFSEL | I | | | pull-down | |
| | PERSTN | I | | | | Schmitt trigger |
| | RSTHALT | I | | | pull-down | Unused pins can be left floating. |
| | SWMODE[3:0] | I | | | pull-down | |
| EJTAG / JTAG | JTAG_TCK | I | LVTTL | STI | pull-up | Unused pins can be left floating. |
| | JTAG_TDI | I | | STI | pull-up | |
| | JTAG_TDO | O | | | | |
| | JTAG_TMS | I | | STI | pull-up | |
| | JTAG_TRST_N | I | | STI | pull-up | |
| SerDes Reference Resistors | REFRES[7:0] | — | Analog | | | Unused pins should be connected to Vss on the board. |
| | REFRESPLL | — | | | | |

**Table 10  Pin Characteristics  (Part 5 of 5)**

[1.] Internal resistor values under typical operating conditions are 92K $\Omega$ for pull-up and 91K $\Omega$ for pull-down.

[2.] All receiver pins set the DC common mode voltage to ground. All transmitters must be AC coupled to the media.

[3.] Schmitt Trigger Input (STI).

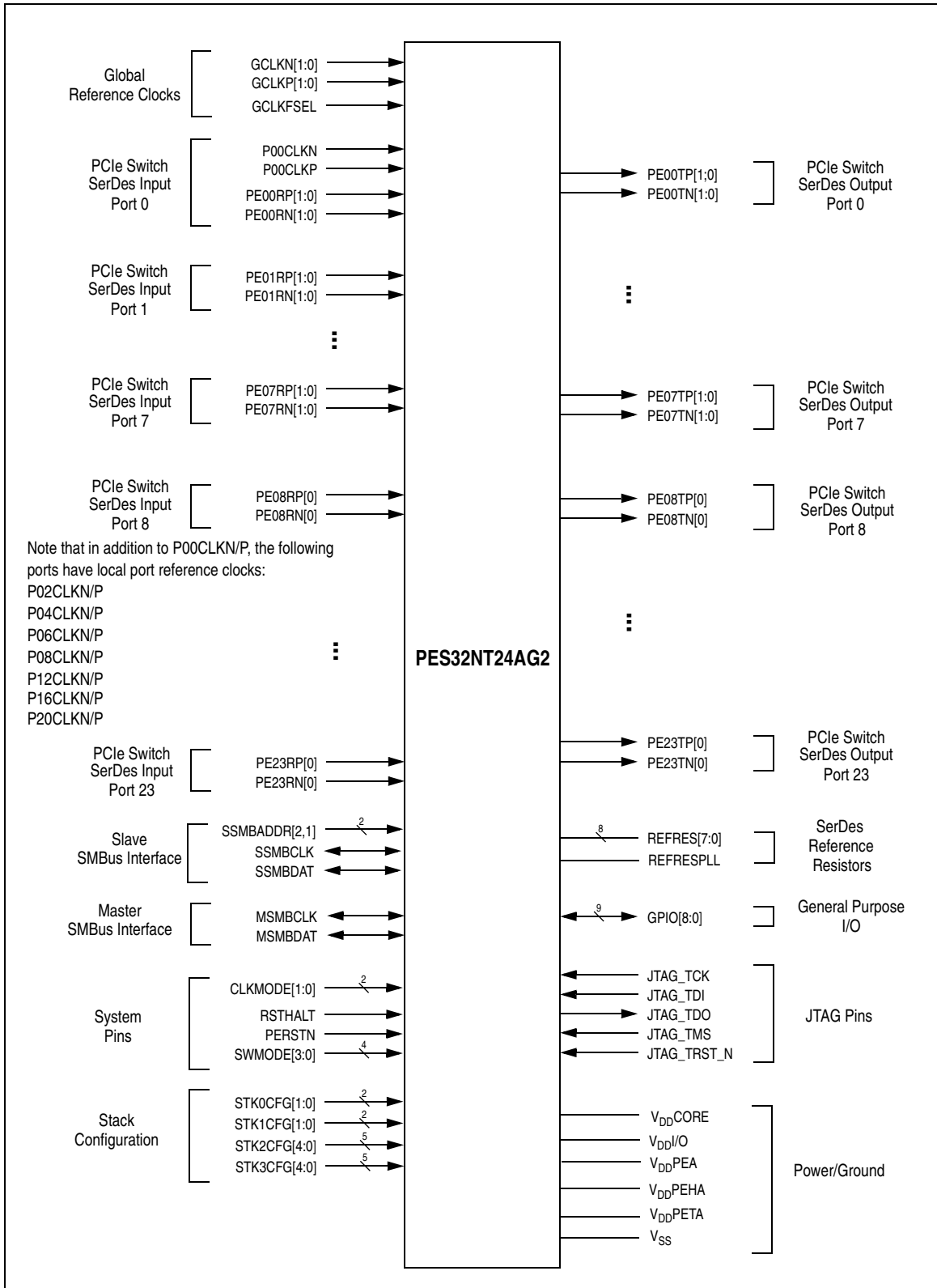## Logic Diagram — PES32NT24AG2



**Figure 3  PES32NT24AG2 Logic Diagram**

## System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 16 and 15.

| Parameter | Description | Condition | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| Refclk$_{FREQ}$ | Input reference clock frequency range | | 100 | | 125[1] | MHz |
| T$_{C-RISE}$ | Rising edge rate | Differential | 0.6 | | 4 | V/ns |
| T$_{C-FALL}$ | Falling edge rate | Differential | 0.6 | | 4 | V/ns |
| V$_{IH}$ | Differential input high voltage | Differential | +150 | | | mV |
| V$_{IL}$ | Differential input low voltage | Differential | | | -150 | mV |
| V$_{CROSS}$ | Absolute single-ended crossing point voltage | Single-ended | +250 | | +550 | mV |
| V$_{CROSS-DELTA}$ | Variation of V$_{CROSS}$ over all rising clock edges | Single-ended | | | +140 | mV |
| V$_{RB}$ | Ring back voltage margin | Differential | -100 | | +100 | mV |
| T$_{STABLE}$ | Time before V$_{RB}$ is allowed | Differential | 500 | | | ps |
| T$_{PERIOD-AVG}$ | Average clock period accuracy | | -300 | | 2800 | ppm |
| T$_{PERIOD-ABS}$ | Absolute period, including spread-spectrum and jitter | | 9.847 | | 10.203 | ns |
| T$_{CC-JITTER}$ | Cycle to cycle jitter | | | | 150 | ps |
| V$_{MAX}$ | Absolute maximum input voltage | | | | +1.15 | V |
| V$_{MIN}$ | Absolute minimum input voltage | | -0.3 | | | V |
| Duty Cycle | Duty cycle | | 40 | | 60 | % |
| Rise/Fall Matching | Single ended rising Refclk edge rate versus falling Refclk edge rate | | | 20 | | % |
| Z$_{C-DC}$ | Clock source output DC impedance | | 40 | | 60 | Ω |

**Table 11  Input Clock Requirements**

[1.] The input clock frequency will be either 100 or 125 MHz depending on signal GCLKFSEL.

**Note:** Refclk jitter compliant to PCIe Gen2 Common Clock architecture is adequate for the GCLKN/P[x] and PE[x]CLKN/P pins of this IDT PCIe switch.  This same jitter specification is applicable when interfacing the switch to another IDT switch in a Separate (Non-Common) Clock architecture.

## AC Timing Characteristics

| Parameter | Description | Gen 1 | | | Gen 2 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min[1] | Typ[1] | Max[1] | Min[1] | Typ[1] | Max[1] | |
| PCIe Transmit | | | | | | | | |
| UI | Unit Interval | 399.88 | 400 | 400.12 | 199.94 | 200 | 200.06 | ps |
| T$_{TX-EYE}$ | Minimum Tx Eye Width | 0.75 | | | 0.75 | | | UI |

**Table 12  PCIe AC Timing Characteristics  (Part 1 of 2)**

| Parameter | Description | Gen 1 | | | Gen 2 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min[1] | Typ[1] | Max[1] | Min[1] | Typ[1] | Max[1] | |
| $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ | Maximum time between the jitter median and maximum deviation from the median | | | 0.125 | | | | UI |
| $T_{TX-RISE}$, $T_{TX-FALL}$ | TX Rise/Fall Time: 20% - 80% | 0.125 | | | 0.15 | | | UI |
| $T_{TX-IDLE-MIN}$ | Minimum time in idle | 20 | | | 20 | | | UI |
| $T_{TX-IDLE-SET-TO-IDLE}$ | Maximum time to transition to a valid Idle after sending an Idle ordered set | | | 8 | | | 8 | ns |
| $T_{TX-IDLE-TO-DIFF-DATA}$ | Maximum time to transition from valid idle to diff data | | | 8 | | | 8 | ns |
| $T_{TX-SKEW}$ | Transmitter data skew between any 2 lanes | | | 1.3 | | | 1.3 | ns |
| $T_{MIN-PULSED}$ | Minimum Instantaneous Lone Pulse Width | | NA | | 0.9 | | | UI |
| $T_{TX-HF-DJ-DD}$ | Transmitter Deterministic Jitter > 1.5MHz Bandwidth | | NA | | | | 0.15 | UI |
| $T_{RF-MISMATCH}$ | Rise/Fall Time Differential Mismatch | | NA | | | | 0.1 | UI |
| PCIe Receive | | | | | | | | |
| UI | Unit Interval | 399.88 | 400 | 400.12 | 199.94 | | 200.06 | ps |
| $T_{RX-EYE}$ (with jitter) | Minimum Receiver Eye Width (jitter tolerance) | 0.4 | | | 0.4 | | | UI |
| $T_{RX-EYE-MEDIUM\ TO\ MAX\ JITTER}$ | Max time between jitter median & max deviation | | | 0.3 | | | | UI |
| $T_{RX-SKEW}$ | Lane to lane input skew | | | 20 | | | 8 | ns |
| $T_{RX-HF-RMS}$ | 1.5 — 100 MHz RMS jitter (common clock) | | NA | | | | 3.4 | ps |
| $T_{RX-HF-DJ-DD}$ | Maximum tolerable DJ by the receiver (common clock) | | NA | | | | 88 | ps |
| $T_{RX-LF-RMS}$ | 10 KHz to 1.5 MHz RMS jitter (common clock) | | NA | | | | 4.2 | ps |
| $T_{RX-MIN-PULSE}$ | Minimum receiver instantaneous eye width | | NA | | 0.6 | | | UI |

**Table 12  PCIe AC Timing Characteristics  (Part 2 of 2)**

[1.] Minimum, Typical, and Maximum values meet the requirements under PCI Express Base Specification 2.1.

| Signal | Symbol | Reference Edge | Min | Max | Unit | Timing Diagram Reference |
|---|---|---|---|---|---|---|
| **GPIO** | | | | | | |
| GPIO[8:0][1] | Tpw_13b[2] | None | 50 | — | ns | See Figure 4. |

**Table 13  GPIO AC Timing Characteristics**

[1.] GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

[2.] The values for this symbol were determined by calculation, not by testing.
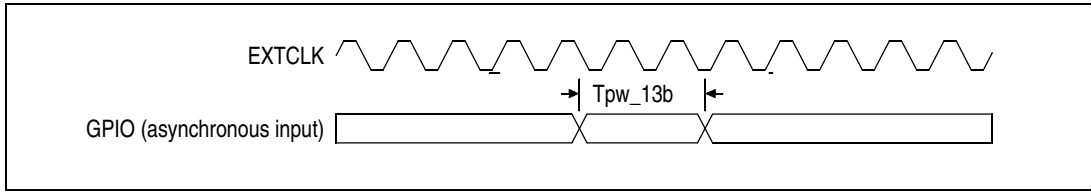
**Figure 4 GPIO AC Timing Waveform**

| Signal | Symbol | Reference Edge | Min | Max | Unit | Timing Diagram Reference |
|---|---|---|---|---|---|---|
| **JTAG** | | | | | | |
| JTAG_TCK | Tper_16a | none | 50.0 | — | ns | See Figure 5. |
| | Thigh_16a, Tlow_16a | | 10.0 | 25.0 | ns | |
| JTAG_TMS[1], JTAG_TDI | Tsu_16b | JTAG_TCK rising | 2.4 | — | ns | |
| | Thld_16b | | 1.0 | — | ns | |
| JTAG_TDO | Tdo_16c | JTAG_TCK falling | — | 20 | ns | |
| | Tdz_16c[2] | | — | 20 | ns | |
| JTAG_TRST_N | Tpw_16d[2] | none | 25.0 | — | ns | |

**Table 14 JTAG AC Timing Characteristics**

[1.] The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

[2.] The values for this symbol were determined by calculation, not by testing.
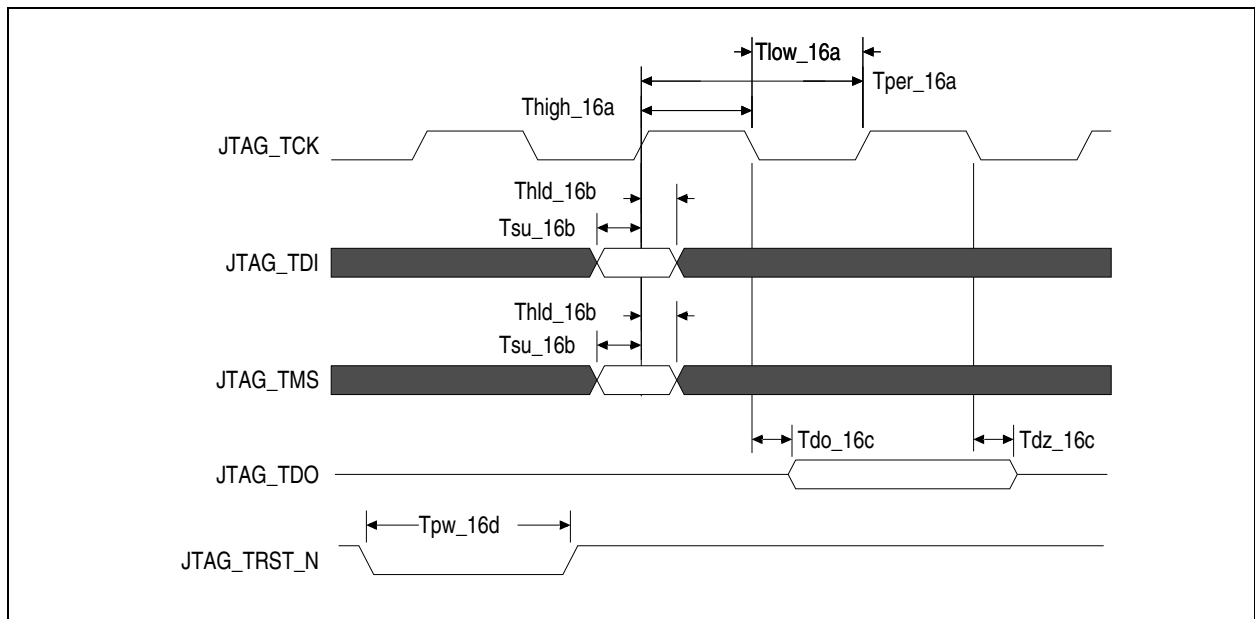
**Figure 5  JTAG AC Timing Waveform**

# Recommended Operating Temperature

| Grade | Temperature |
|---|---|
| Commercial | 0°C to +70°C Ambient |
| Industrial | -40°C to +85°C Ambient |

**Table 15  PES32NT24AG2 Operating Temperatures**

# Recommended Operating Supply Voltages — Commercial Temperature

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{DD}CORE$ | Internal logic supply | 0.9 | 1.0 | 1.1 | V |
| $V_{DD}I/O$ | I/O supply except for SerDes | 3.125 | 3.3 | 3.465 | V |
| $V_{DD}PEA^1$ | PCI Express Analog Power | 0.95 | 1.0 | 1.1 | V |
| $V_{DD}PEHA^2$ | PCI Express Analog High Power | 2.25 | 2.5 | 2.75 | V |
| $V_{DD}PETA^1$ | PCI Express Transmitter Analog Voltage | 0.95 | 1.0 | 1.1 | V |
| $V_{SS}$ | Common ground | 0 | 0 | 0 | V |

**Table 16  PES32NT24AG2 Operating Voltages — Commercial Temperature**

[1.] $V_{DD}PEA$ and $V_{DD}PETA$ should have no more than $25mV_{peak-peak}$ AC power supply noise superimposed on the 1.0V nominal DC value.

[2.] $V_{DD}PEHA$ should have no more than $50mV_{peak-peak}$ AC power supply noise superimposed on the 2.5V nominal DC value.

# Recommended Operating Supply Voltages — Industrial Temperature

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{DD}CORE$ | Internal logic supply | 0.9 | 1.0 | 1.1 | V |
| $V_{DD}I/O$ | I/O supply except for SerDes | 3.125 | 3.3 | 3.465 | V |
| $V_{DD}PEA^1$ | PCI Express Analog Power | 0.95 | 1.0 | 1.05 | V |
| $V_{DD}PEHA^2$ | PCI Express Analog High Power | 2.25 | 2.5 | 2.75 | V |
| $V_{DD}PETA^1$ | PCI Express Transmitter Analog Voltage | 0.95 | 1.0 | 1.1 | V |
| $V_{SS}$ | Common ground | 0 | 0 | 0 | V |

**Table 17  PES32NT24AG2 Operating Voltages — Industrial Temperature**

[1.] $V_{DD}PEA$ and $V_{DD}PETA$ should have no more than $25mV_{peak-peak}$ AC power supply noise superimposed on the 1.0V nominal DC value.

[2.] $V_{DD}PEHA$ should have no more than $50mV_{peak-peak}$ AC power supply noise superimposed on the 2.5V nominal DC value.

# Power-Up/Power-Down Sequence

During power supply ramp-up, $V_{DD}CORE$ must remain at least 1.0V below $V_{DD}I/O$ at all times. There are no other power-up sequence requirements for the various operating supply voltages. The power-down sequence can occur in any order.

# Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 16 (and also listed below).

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 16 (and also listed below).

| Number of Active Lanes per Port | | Core Supply | | PCIe Analog Supply | | PCIe Analog High Supply | | PCIe Transmitter Supply | | I/O Supply | | Total | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Typ 1.0V | Max 1.1V | Typ 1.0V | Max 1.1V | Typ 2.5V | Max 2.75V | Typ 1.0V | Max 1.1V | Typ 3.3V | Max 3.465 | Typ Power | Max Power |
| x8/x8/x8/x4/x4 (Full Swing) | mA | 2535 | 3400 | 1627 | 1855 | 233 | 233 | 687 | 740 | 3 | 5 | | |
| | Watts | 2.54 | 3.74 | 1.63 | 2.04 | 0.58 | 0.64 | 0.69 | 0.81 | 0.01 | 0.02 | 5.45 | 7.25 |
| x8/x8/x8/x4/x4 (Half Swing) | mA | 2535 | 3400 | 1399 | 1595 | 233 | 233 | 357 | 385 | 3 | 5 | | |
| | Watts | 2.54 | 3.74 | 1.40 | 1.76 | 0.58 | 0.64 | 0.36 | 0.42 | 0.01 | .02 | 4.89 | 6.58 |

**Table 18  PES32NT24AG2 Power Consumption**

**Note 1**: The above power consumption assumes that all ports are functioning at Gen2 (5.0 GT/S) speeds. Power consumption can be reduced by turning off unused ports through software or through boot EEPROM. Power savings will occur in $V_{DD}PEA$, $V_{DD}PEHA$, and $V_{DD}PETA$. Power savings can be estimated as directly proportional to the number of unused ports, since the power consumption of a turned-off port is close to zero. For example, if 3 ports out of 16 are turned off, then the power savings for each of the above three power rails can be calculated quite simply as 3/16 multiplied by the power consumption indicated in the above table.

**Note 2**: Using a port in Gen1 mode (2.5GT/S) results in approximately 18% power savings for each power rail: $V_{DD}PEA$, $V_{DD}PEHA$, and $V_{DD}PETA$.

# Thermal Considerations

This section describes thermal considerations for the PES32NT24AG2 (23mm$^2$ FCBGA484 package). The data in Table 19 below contains information that is relevant to the thermal performance of the PES32NT24AG2 switch.

| Symbol | Parameter | Value | Units | Conditions |
|---|---|---|---|---|
| $T_{J(max)}$ | Junction Temperature | 125 | $^oC$ | Maximum |
| $T_{A(max)}$ | Ambient Temperature | 70 | $^oC$ | Maximum for commercial-rated products |
| | | 85 | $^oC$ | Maximum for industrial-rated products |
| $\theta_{JA(effective)}$ | Effective Thermal Resistance, Junction-to-Ambient | 15.2 | $^oC/W$ | Zero air flow |
| | | 8.5 | $^oC/W$ | 1 m/S air flow |
| | | 7.1 | $^oC/W$ | 2 m/S air flow |
| $\theta_{JB}$ | Thermal Resistance, Junction-to-Board | 3.1 | $^oC/W$ | |
| $\theta_{JC}$ | Thermal Resistance, Junction-to-Case | 0.15 | $^oC/W$ | |
| P | Power Dissipation of the Device | 7.25 | Watts | Maximum |

**Table 19  Thermal Specifications for PES32NT24AG2, 23x23 mm FCBGA484 Package**

**Note:**   It is important for the reliability of this device in any user environment that the junction temperature not exceed the $T_{J(max)}$ value specified in Table 19. Consequently, the effective junction to ambient thermal resistance ($\theta_{JA}$) for the worst case scenario must be maintained below the value determined by the formula:

$$\theta_{JA} = (T_{J(max)} - T_{A(max)})/P$$

Given that the values of $T_{J(max)}$, $T_{A(max)}$, and P are known, the value of desired $\theta_{JA}$ becomes a known entity to the system designer. How to achieve the desired $\theta_{JA}$ is left up to the board or system designer, but in general, it can be achieved by adding the effects of $\theta_{JC}$ (value provided in Table 19), thermal resistance of the chosen adhesive ($\theta_{CS}$), that of the heat sink ($\theta_{SA}$), amount of airflow, and properties of the circuit board (number of layers and size of the board). It is strongly recommended that users perform their own thermal analysis for their own board and system design scenarios.

# DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 16.

**Note:** See Table 10, Pin Characteristics, for a complete I/O listing.

| I/O Type | Parameter | Description | Gen1 | | | Gen2 | | | Unit | Condi-tions |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min[1] | Typ[1] | Max[1] | Min[1] | Typ[1] | Max[1] | | |
| Serial Link | PCIe Transmit | | | | | | | | | |
| | $V_{TX-DIFFp-p}$ | Differential peak-to-peak output voltage | 800 | | 1200 | 800 | | 1200 | mV | |
| | $V_{TX-DIFFp-p-LOW}$ | Low-Drive Differential Peak to Peak Output Voltage | 400 | | 1200 | 400 | | 1200 | mV | |
| | $V_{TX-DE-RATIO-3.5dB}$ | De-emphasized differential output voltage | -3 | | -4 | -3.0 | -3.5 | -4.0 | dB | |
| | $V_{TX-DE-RATIO-6.0dB}$ | De-emphasized differential output voltage | | NA | | -5.5 | -6.0 | -6.5 | dB | |
| | $V_{TX-DC-CM}$ | DC Common mode voltage | 0 | | 3.6 | 0 | | 3.6 | V | |
| | $V_{TX-CM-ACP}$ | RMS AC peak common mode output voltage | | | 20 | | | | mV | |
| | $V_{TX-CM-DC-active-idle-delta}$ | Abs delta of DC common mode voltage between L0 and idle | | | 100 | | | 100 | mV | |
| | $V_{TX-CM-DC-line-delta}$ | Abs delta of DC common mode voltage between D+ and D- | | | 25 | | | 25 | mV | |
| | $V_{TX-Idle-DiffP}$ | Electrical idle diff peak output | | | 20 | | | 20 | mV | |
| | $RL_{TX-DIFF}$ | Transmitter Differential Return loss | 10 | | | | | 10 | dB | 0.05 - 1.25GHz |
| | | | | | | | | 8 | dB | 1.25 - 2.5GHz |
| | $RL_{TX-CM}$ | Transmitter Common Mode Return loss | 6 | | | | | 6 | dB | |
| | $Z_{TX-DIFF-DC}$ | DC Differential TX impedance | 80 | 100 | 120 | | | 120 | Ω | |
| | VTX-CM-ACpp | Peak-Peak AC Common | | NA | | | | 100 | mV | |
| | $V_{TX-DC-CM}$ | Transmit Driver DC Common Mode Voltage | 0 | | 3.6 | 0 | | 3.6 | V | |
| | $V_{TX-RCV-DETECT}$ | The amount of voltage change allowed during Receiver Detection | | | 600 | | | 600 | mV | |
| | $I_{TX-SHORT}$ | Transmitter Short Circuit Current Limit | 0 | | 90 | | | 90 | mA | |

**Table 20  DC Electrical Characteristics  (Part 1 of 3)**

| I/O Type | Parameter | Description | Gen1 | | | Gen2 | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min[1] | Typ[1] | Max[1] | Min[1] | Typ[1] | Max[1] | | |
| Serial Link (cont.) | PCIe Receive | | | | | | | | | |
| | $V_{RX-DIFFp-p}$ | Differential input voltage (peak-to-peak) | 175 | | 1200 | 120 | | 1200 | mV | |
| | $RL_{RX-DIFF}$ | Receiver Differential Return Loss | 10 | | | | | 10 | dB | 0.05 - 1.25GHz |
| | | | | | | | | 8 | | 1.25 - 2.5GHz |
| | $RL_{RX-CM}$ | Receiver Common Mode Return Loss | 6 | | | | | 6 | dB | |
| | $Z_{RX-DIFF-DC}$ | Differential input impedance (DC) | 80 | 100 | 120 | Refer to return loss spec | | | Ω | |
| | $Z_{RX--DC}$ | DC common mode impedance | 40 | 50 | 60 | 40 | | 60 | Ω | |
| | $Z_{RX-COMM-DC}$ | Powered down input common mode impedance (DC) | 200k | 350k | | | | 50k | Ω | |
| | $Z_{RX-HIGH-IMP-DC-POS}$ | DC input CM input impedance for V>0 during reset or power down | | | 50k | | | 50k | Ω | |
| | $Z_{RX-HIGH-IMP-DC-NEG}$ | DC input CM input impedance for V<0 during reset or power down | | | 1.0k | | | 1.0k | Ω | |
| | $V_{RX-IDLE-DET-DIFFp-p}$ | Electrical idle detect threshold | 65 | | 175 | 65 | | 175 | mV | |
| | $V_{RX-CM-ACp}$ | Receiver AC common-mode peak voltage | | | 150 | | | 150 | mV | $V_{RX-CM-ACp}$ |
| PCIe REFCLK | | | | | | | | | | |
| | $C_{IN}$ | Input Capacitance | 1.5 | — | | 1.5 | — | | pF | |
| Other I/Os | | | | | | | | | | |
| LOW Drive Output | $I_{OL}$ | | — | 2.5 | — | — | 2.5 | — | mA | $V_{OL}$ = 0.4v |
| | $I_{OH}$ | | — | -5.5 | — | — | -5.5 | — | mA | $V_{OH}$ = 1.5V |
| High Drive Output | $I_{OL}$ | | — | 12.0 | — | — | 12.0 | — | mA | $V_{OL}$ = 0.4v |
| | $I_{OH}$ | | — | -20.0 | — | — | -20.0 | — | mA | $V_{OH}$ = 1.5V |
| Schmitt Trigger Input (STI) | $V_{IL}$ | | -0.3 | — | 0.8 | -0.3 | — | 0.8 | V | — |
| | $V_{IH}$ | | 2.0 | — | $V_{DD}$I/O + 0.5 | 2.0 | — | $V_{DD}$I/O + 0.5 | V | — |
| Input | $V_{IL}$ | | -0.3 | — | 0.8 | -0.3 | — | 0.8 | V | — |
| | $V_{IH}$ | | 2.0 | — | $V_{DD}$I/O + 0.5 | 2.0 | — | $V_{DD}$I/O + 0.5 | V | — |
| 3.3V Output Low Voltage | $V_{OL}$ | | — | — | 0.4 | | — | 0.4 | V | $I_{OL}$ = 8mA for JTAG_TDO and GPIO pins |
| 3.3V Output High Voltage | $V_{OH}$ | | 2.4 | — | — | 2.4 | — | — | V | $I_{OH}$ = 8mA for JTAG_TDO and GPIO pins |
| Capacitance | $C_{IN}$ | | — | — | 8.5 | — | — | 8.5 | pF | — |

**Table 20  DC Electrical Characteristics  (Part 2 of 3)**