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34-Lane 16-Port PCIe® Gen2 System Interconnect Switch

89HPES34H16G2
Data Sheet

Device Overview

The 89HPES34H16G2 is a member of the IDT PRECISE™ family of PCI Express® switching solutions. The PES34H16G2 is a 34-lane, 16-port peripheral chip that performs PCI Express packet switching with a feature set optimized for high-performance applications such as servers, storage, and communications/networking. It provides connectivity and switching functions between a PCI Express upstream port and up to fifteen downstream ports and supports switching between downstream ports.

Features

- **High Performance Non-Blocking Switch Architecture**
  - 34-lane 16-port PCIe switch
    - *Three x8 switch ports each of which can bifurcate to two x4 ports (total of six x4 ports)*
    - *Ten x1 switch ports*
  - Integrated SerDes supports 5.0 GT/s Gen2 and 2.5 GT/s Gen1 operation
  - Delivers up to 34 GBps (272 Gbps) of switching capacity
  - Supports 128 Bytes to 2 KB maximum payload size
  - Low latency cut-through architecture
  - Supports one virtual channel and eight traffic classes
- **Standards and Compatibility**
  - PCI Express Base Specification 2.0 compliant
  - Implements the following optional PCI Express features
    - *Advanced Error Reporting (AER) on all ports*
    - *End-to-End CRC (ECRC)*
    - *Access Control Services (ACS)*
    - *Power Budgeting Enhanced Capability*
    - *Device Serial Number Enhanced Capability*
    - *Sub-System ID and Sub-System Vendor ID Capability*
    - *Internal Error Reporting ECN*
    - *Multicast ECN*
    - *VGA and ISA enable*
    - *L0s and L1 ASPM*
    - *ARI ECN*
  - Compatible with IDT 89HPES34H16 PCIe Gen1 switch
- **Port Configurability**
  - x8, x4, and x1 ports
    - Ability to merge adjacent x4 ports to create a x8 port
  - Automatic per port link width negotiation (x8 → x4 → x2 → x1)
  - Crosslink support
  - Automatic lane reversal
  - Autonomous and software managed link width and speed control
  - Per lane SerDes configuration
    - *De-emphasis*
    - *Receive equalization*
    - *Drive strength*
- **Switch Partitioning**
  - IDT proprietary feature that creates logically independent switches in the device
  - Supports up to 16 fully independent switch partitions
  - Configurable downstream port device numbering
  - Supports dynamic reconfiguration of switch partitions
    - *Dynamic port reconfiguration (downstream or upstream)*
    - *Dynamic migration of ports between partitions*
    - *Movable upstream port within and between switch partitions*
- **Initialization / Configuration**
  - Supports Root (BIOS, OS, or driver), Serial EEPROM, or SMBus switch initialization
  - Common switch configurations are supported with pin strapping (no external components)
  - Supports in-system Serial EEPROM initialization/programming
- **Quality of Service (QoS)**
  - Port arbitration
    - *Round robin*
  - Request metering
    - *IDT proprietary feature that balances bandwidth among switch ports for maximum system throughput*
  - High performance switch core architecture
    - *Combined Input Output Queued (CIOQ) switch architecture with large buffers*
- **Multicast**
  - Compliant to the PCI-SIG multicast ECN
  - Supports arbitrary multicasting of Posted transactions
  - Supports 64 multicast groups
  - Multicast overlay mechanism support
  - ECRC regeneration support
- **Clocking**
  - Supports 100 MHz and 125 MHz reference clock frequencies
  - Flexible clocking modes
    - *Common clock*
    - *Non-common clock*
- **Hot-Plug and Hot Swap**
  - Hot-plug controller on all ports
    - *Hot-plug supported on all downstream switch ports*

- All ports support hot-plug using low-cost external I^2C I/O expanders
- Configurable presence detect supports card and cable applications
- GPE output pin for hot-plug event notification
  - *Enables SCI/SMI generation for legacy operating system support*
- Hot-swap capable I/O

◆ **Power Management**

- Supports D0, D3hot and D3 power management states
- Active State Power Management (ASPM)
  - *Supports L0, L0s, L1, L2/L3 Ready and L3 link states*
  - *Configurable L0s and L1 entry timers allow performance/ power-savings tuning*
- Supports PCI Express Power Budgeting Capability
- SerDes power savings
  - *Supports low swing / half-swing SerDes operation*
  - *SerDes optionally turned-off in D3hot*
  - *SerDes associated with unused ports are turned-off*
  - *SerDes associated with unused lanes are placed in a low power state*

◆ **32 General Purpose I/O**

◆ **Reliability, Availability and Serviceability (RAS)**

- ECRC support
- AER on all ports
- SECDED ECC protection on all internal RAMs
- End-to-end data path parity protection
- Checksum Serial EEPROM content protected
- Autonomous link reliability (preserves system operation in the presence of faulty links)
- Ability to generate an interrupt (INTx or MSI) on link up/down transitions

◆ **Test and Debug**

- On-chip link activity and status outputs available for Port 0 (upstream port)
- Per port link activity and status outputs available using external I^2C I/O expander for all other ports
- SerDes test modes
- Supports IEEE 1149.6 AC JTAG and IEEE 1149.1 JTAG

◆ **Power Supplies**

- Requires only two power supply voltages (1.0 V and 2.5 V) Note that a 3.3V is preferred for V_{DD}I/O
- No power sequencing requirements

◆ **Packaged in a 35mm x 35mm 1156-ball Flip Chip BGA with 1mm ball spacing**

- Compatible with IDT 89HPES34H16 PCIe Gen1 switch

Note: For pin compatibility issues, contact the IDT help desk at ssdhelp@idt.com.

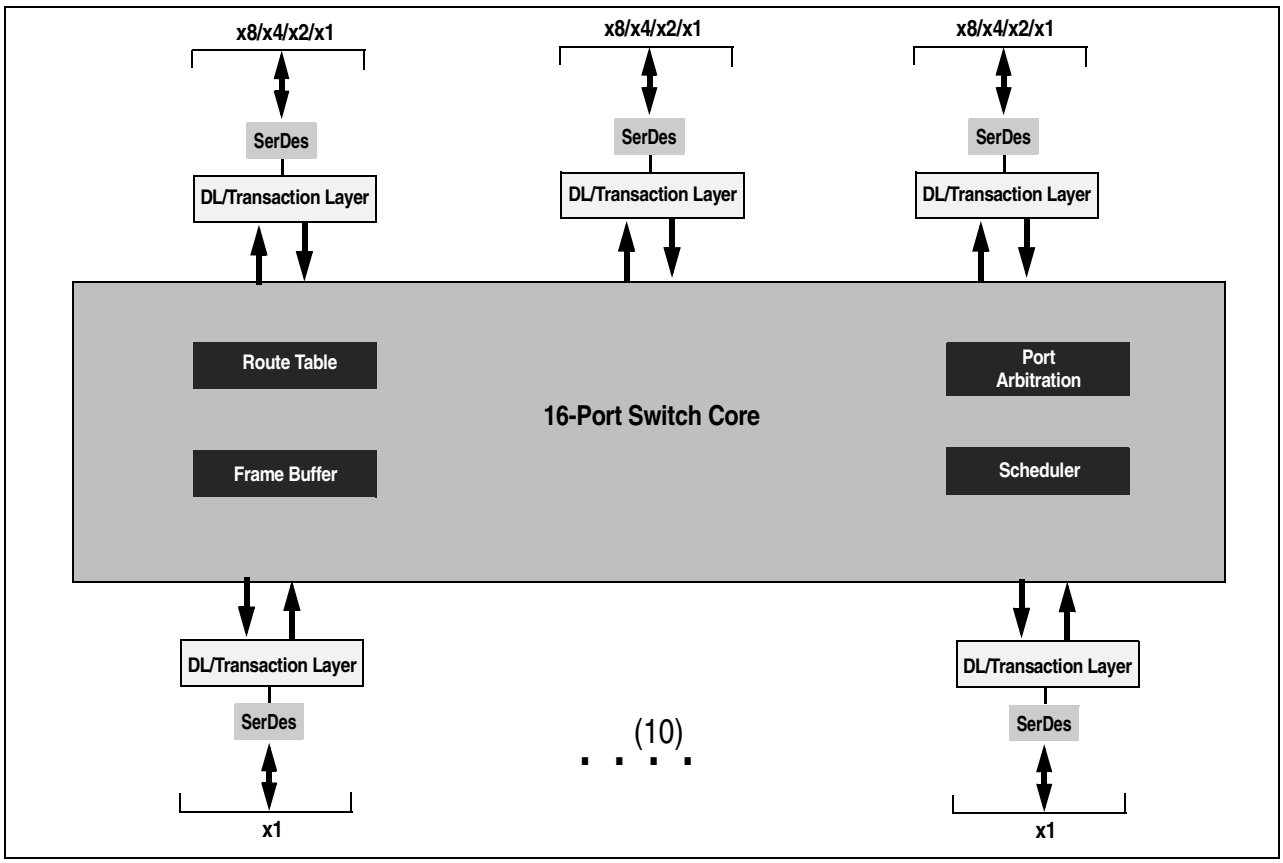
Product Description

Utilizing standard PCI Express interconnect, the PES34H16G2 provides the most efficient I/O connectivity for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides 34 GBps (272 Gbps) of aggregated, full-duplex switching capacity through 34 integrated serial lanes, using proven and robust IDT technology. Each lane provides 5 GT/s of bandwidth in both directions and is fully compliant with PCI Express Base Specification, Revision 2.0.

The PES34H16G2 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers. The PES34H16G2 can operate either as a store and forward switch or a cut-through switch. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to enable efficient switching and I/O connectivity.

The PES34H16G2 is a *partitionable* PCIe switch. This means that in addition to operating as a standard PCI express switch, the PES34H16G2 ports may be partitioned into groups that logically operate as completely independent PCIe switches. Figure 2 illustrates a three partition PES34H16G2 configuration.

Block Diagram



34 PCI Express Lanes
Up to 6 x4 ports and 10 x1 Ports

Figure 1 PES34H16G2 Block Diagram

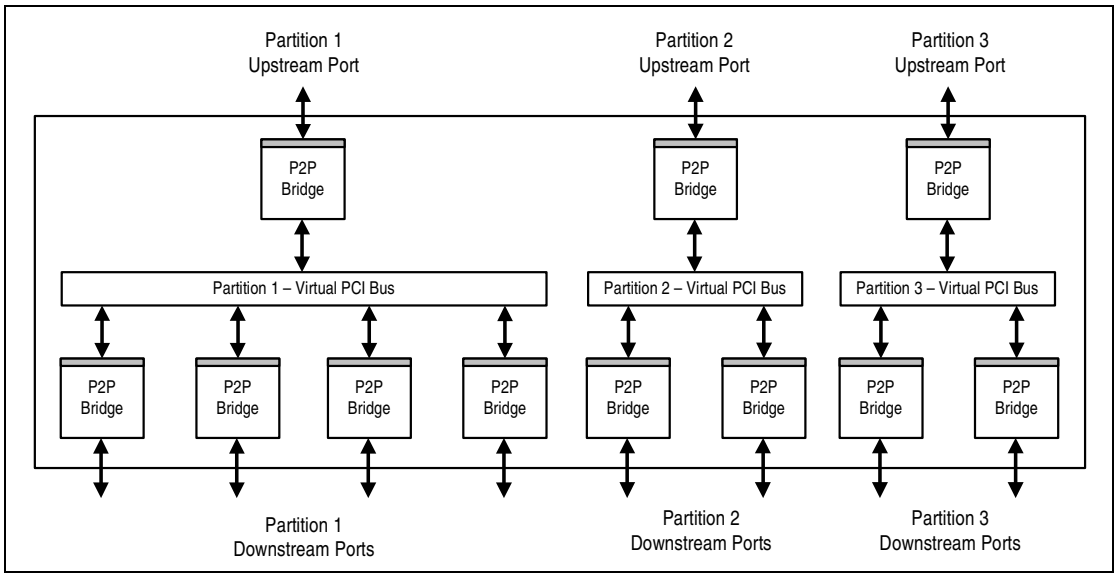


Figure 2 Example of Usage of Switch Partitioning

SMBus Interface

The PES34H16G2 contains two SMBus interfaces. The slave interface provides full access to the configuration registers in the PES34H16G2, allowing every configuration register in the device to be read or written by an external agent. The master interface allows the default configuration register values of the PES34H16G2 to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander.

Six pins make up each of the two SMBus interfaces. These pins consist of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins. In the slave interface, these address pins allow the SMBus address to which the device responds to be configured. In the master interface, these address pins allow the SMBus address of the serial configuration EEPROM from which data is loaded to be configured. The SMBus address is set up on negation of PERSTN by sampling the corresponding address pins. When the pins are sampled, the resulting address is assigned as shown in Table 1.

Bit	Slave SMBus Address	Master SMBus Address
1	SSMBADDR[1]	MSMBADDR[1]
2	SSMBADDR[2]	MSMBADDR[2]
3	SSMBADDR[3]	MSMBADDR[3]
4	0	MSMBADDR[4]
5	SSMBADDR[5]	1
6	1	0
7	1	1

Table 1 Master and Slave SMBus Address Assignment

As shown in Figure 3, the master and slave SMBuses may only be used in a split configuration.

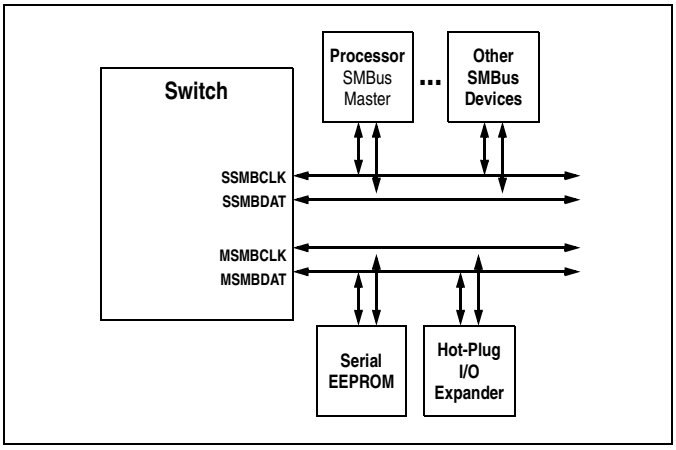


Figure 3 Split SMBus Interface Configuration

The switch's SMBus master interface does not support SMBus arbitration. As a result, the switch's SMBus master must be the only master in the SMBus lines that connect to the serial EEPROM and I/O expander slaves. In the split configuration, the master and slave SMBuses operate as two independent buses; thus, multi-master arbitration is not required.

Hot-Plug Interface

The PES34H16G2 supports PCI Express Hot-Plug on each downstream port (ports 1 through 15). To reduce the number of pins required on the device, the PES34H16G2 utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES34H16G2 generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES34H16G2. In response to an I/O expander interrupt, the PES34H16G2 generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

General Purpose Input/Output

The PES34H16G2 provides 32 General Purpose I/O (GPIO) pins that may be individually configured as general purpose inputs, general purpose outputs, or alternate functions. Some GPIO pins are shared with other on-chip functions. These alternate functions may be enabled via software, SMBus slave interface, or serial configuration EEPROM.

Pin Description

The following tables list the functions of the pins provided on the PES34H16G2. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an “N” are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level. Differential signals end with a suffix “N” or “P.” The differential signal ending in “P” is the positive portion of the differential pair and the differential signal ending in “N” is the negative portion of the differential pair.

Signal	Type	Name/Description
PE00RN[3:0] PE00RP[3:0]	I	**PCI Express Port 0 Serial Data Receive.** Differential PCI Express receive pairs for port 0.
PE00TN[3:0] PE00TP[3:0]	O	**PCI Express Port 0 Serial Data Transmit.** Differential PCI Express transmit pairs for port 0.
PE01RN[3:0] PE01RP[3:0]	I	**PCI Express Port 1 Serial Data Receive.** Differential PCI Express receive pairs for port 1. When port 0 is merged with port 1, these signals become port 0 receive pairs for lanes 4 through 7.
PE01TN[3:0] PE01TP[3:0]	O	**PCI Express Port 1 Serial Data Transmit.** Differential PCI Express transmit pairs for port 1. When port 0 is merged with port 1, these signals become port 0 transmit pairs for lanes 4 through 7.
PE02RN[3:0] PE02RP[3:0]	I	**PCI Express Port 2 Serial Data Receive.** Differential PCI Express receive pairs for port 2.
PE02TN[3:0] PE02TP[3:0]	O	**PCI Express Port 2 Serial Data Transmit.** Differential PCI Express transmit pairs for port 2.
PE03RN[3:0] PE03RP[3:0]	I	**PCI Express Port 3 Serial Data Receive.** Differential PCI Express receive pairs for port 3. When port 2 is merged with port 3, these signals become port 2 receive pairs for lanes 4 through 7.
PE03TN[3:0] PE03TP[3:0]	O	**PCI Express Port 3 Serial Data Transmit.** Differential PCI Express transmit pairs for port 2. When port 2 is merged with port 3, these signals become port 2 transmit pairs for lanes 4 through 7.
PE04RN[3:0] PE04RP[3:0]	I	**PCI Express Port 4 Serial Data Receive.** Differential PCI Express receive pairs for port 4.
PE04TN[3:0] PE04TP[3:0]	O	**PCI Express Port 4 Serial Data Transmit.** Differential PCI Express transmit pairs for port 4.
PE05RN[3:0] PE05RP[3:0]	I	**PCI Express Port 5 Serial Data Receive.** Differential PCI Express receive pairs for port 5. When port 4 is merged with port 5, these signals become port 4 receive pairs for lanes 4 through 7.

Table 2 PCI Express Interface Pins (Part 1 of 2)

Signal	Type	Name/Description
PE05TN[3:0] PE05TP[3:0]	O	**PCI Express Port 5 Serial Data Transmit.** Differential PCI Express transmit pairs for port 5. When port 4 is merged with port 5, these signals become port 4 transmit pairs for lanes 4 through 7.
PE06RN[0] PE06RP[0]	I	**PCI Express Port 6 Serial Data Receive.** Differential PCI Express receive pair for port 6.
PE06TN[0] PE06TP[0]	O	**PCI Express Port 6 Serial Data Transmit.** Differential PCI Express transmit pair for port 6.
PE07RN[0] PE07RP[0]	I	**PCI Express Port 7 Serial Data Receive.** Differential PCI Express receive pair for port 7.
PE07TN[0] PE07TP[0]	O	**PCI Express Port 7 Serial Data Transmit.** Differential PCI Express transmit pair for port 7.
PE08RN[0] PE08RP[0]	I	**PCI Express Port 8 Serial Data Receive.** Differential PCI Express receive pair for port 8.
PE08TN[0] PE08TP[0]	O	**PCI Express Port 8 Serial Data Transmit.** Differential PCI Express transmit pair for port 8.
PE09RN[0] PE09RP[0]	I	**PCI Express Port 9 Serial Data Receive.** Differential PCI Express receive pair for port 9.
PE09TN[[0] PE09TP[0]	O	**PCI Express Port 9 Serial Data Transmit.** Differential PCI Express transmit pair for port 9.
PE10RN[0] PE10RP[0]	I	**PCI Express Port 10 Serial Data Receive.** Differential PCI Express receive pair for port 10.
PE10TN[0] PE10TP[0]	O	**PCI Express Port 10 Serial Data Transmit.** Differential PCI Express transmit pair for port 10.
PE11RN[0] PE11RP[0]	I	**PCI Express Port 11 Serial Data Receive.** Differential PCI Express receive pair for port 11.
PE11TN[0] PE11TP[0]	O	**PCI Express Port 11 Serial Data Transmit.** Differential PCI Express transmit pair for port 11.
PE12RN[0] PE12RP[0]	I	**PCI Express Port 12 Serial Data Receive.** Differential PCI Express receive pair for port 12.
PE12TN[0] PE12TP[0]	O	**PCI Express Port 12 Serial Data Transmit.** Differential PCI Express transmit pair for port 12.
PE13RN[0] PE13RP[0]	I	**PCI Express Port 13 Serial Data Receive.** Differential PCI Express receive pair for port 13.
PE13TN[0] PE13TP[0]	O	**PCI Express Port 13 Serial Data Transmit.** Differential PCI Express transmit pair for port 13. W
PE14RN[0] PE14RP[0]	I	**PCI Express Port 14 Serial Data Receive.** Differential PCI Express receive pair for port 14.
PE14TN[0] PE14TP[0]	O	**PCI Express Port 14 Serial Data Transmit.** Differential PCI Express transmit pair for port 14.
PE15RN[0] PE15RP[0]	I	**PCI Express Port 15 Serial Data Receive.** Differential PCI Express receive pair for port 15.
PE15TN[0] PE15TP[0]	O	**PCI Express Port 15 Serial Data Transmit.** Differential PCI Express transmit pair for port 15.

Table 2 PCI Express Interface Pins (Part 2 of 2)

Signal	Type	Name/Description
GCLKN[1:0] GCLKP[1:0]	I	**Global Reference Clock.** Differential reference clock input pair. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic. The frequency of the differential reference clock is determined by the GCLKFSEL signal.

Table 3 Reference Clock Pins

Signal	Type	Name/Description
MSMBADDR[4:1]	I	**Master SMBus Address.** These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded.
MSMBCLK	I/O	**Master SMBus Clock.** This bidirectional signal is used to synchronize transfers on the master SMBus. It is active and generating the clock only when the EEPROM or I/O Expanders are being accessed.
MSMBDAT	I/O	**Master SMBus Data.** This bidirectional signal is used for data on the master SMBus.
SSMBADDR[5,3:1]	I	**Slave SMBus Address.** These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	**Slave SMBus Clock.** This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	**Slave SMBus Data.** This bidirectional signal is used for data on the slave SMBus.

Table 4 SMBus Interface Pins

Signal	Type	Name/Description
GPIO[0]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART0PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[1]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART1PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[2]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART2PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[3]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART3PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.

Table 5 General Purpose I/O Pins (Part 1 of 5)

Signal	Type	Name/Description
GPIO[4]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function — Reserved 2nd Alternate function pin name: P0LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 0 Link Up Status output.
GPIO[5]	O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: GPEN 1st Alternate function pin type: Output 1st Alternate function: Hot-plug general purpose even output. 2nd Alternate function pin name: P0ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 0 Link Active Status Output.
GPIO[6]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[7]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[8]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN Alternate function pin type: Input Alternate function: IO expander interrupt.
GPIO[9]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0APN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 0 Attention Push Button Input.
GPIO[10]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0PDN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 0 Presence Detect Input.
GPIO[11]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0PFN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 0 Power Fault Input.
GPIO[12]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0PWRGDN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 0 Power Good Input.
GPIO[13]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0MRLN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 0 Manually Operated Retention latch Input.
GPIO[14]	O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0AIN Alternate function pin type: Output Alternate function: Hot Plug Signal Group 0 Attention Indicator Output.

Table 5 General Purpose I/O Pins (Part 2 of 5)

Signal	Type	Name/Description
GPIO[15]	O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0PIN Alternate function pin type: Output Alternate function: Hot Plug Signal Group 0 Power Indicator Output.
GPIO[16]	O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0PEP Alternate function pin type: Output Alternate function: Hot Plug Signal Group 0 Power Enable Output.
GPIO[17]	O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0RSTN Alternate function pin type: Output Alternate function: Hot Plug Signal Group 0 Reset Output.
GPIO[18]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP1APN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 1 Attention Push Button Input.
GPIO[19]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP1PDN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 1 Presence Detect Input.
GPIO[20]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP1PFN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 1 Power Fault Input.
GPIO[21]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP1PWRGDN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 1 Power Good Input.
GPIO[22]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP1MRLN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 1 Manually Operated Retention. 2nd Alternate function pin name: P1LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 1 Link Up Status Output.
GPIO[23]	O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP1AIN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 1 Attention Indicator Output. 2nd Alternate function pin name: P1ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 1 Link Active Status Output.

Table 5 General Purpose I/O Pins (Part 3 of 5)

Signal	Type	Name/Description
GPIO[24]	O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP1PIN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 1 Power Indicator Output. 2nd Alternate function pin name: P2LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 2 Link Up Status Output.
GPIO[25]	O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP1PEP 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 1 Power Enable Output. 2nd Alternate function pin name: P2ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 2 Link Active Status Output.
GPIO[26]	O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP1RSTN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 1 Reset Output. 2nd Alternate function pin name: P3LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 3 Link Up Status Output.
GPIO[27]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2APN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 2 Attention Push Button Input. 2nd Alternate function pin name: P3ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 3 Link Active Status Output.
GPIO[28]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2PDN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 0 Presence Detect Input. 2nd Alternate function pin name: P4LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 4 Link Up Status Output.

Table 5 General Purpose I/O Pins (Part 4 of 5)

Signal	Type	Name/Description
GPIO[29]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2PFN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 2 Power Fault Input. 2nd Alternate function pin name: P4ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 4 Link Active Status Output.
GPIO[30]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2PWRGDN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 2 Power Good Input. 2nd Alternate function pin name: P5LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 5 Link Up Status Output.
GPIO[31]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2MRLN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 2 Manually Operated Retention Latch Input. 2nd Alternate function pin name: P5ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 5 Link Active Status Output.

Table 5 General Purpose I/O Pins (Part 5 of 5)

Signal	Type	Name/Description
CLKMODE[1:0]		**Clock Mode.** These signals determine the port clocking mode used by ports of the device.
GCLKFSEL	I	**Global Clock Frequency Select.** These signals select the frequency of the GCLKP and GCLKN signals. 0x0 100 MHz 0x1 125 MHz
MSMBSMODE	I	**Master SMBus Slow Mode.** The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 KHz. This value may not be overridden.
P01MERGEN	I	**Port 0 and 1 Merge.** P01MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 0 is merged with port 1 to form a single x8 port. The Serdes lanes associated with port 1 become lanes 4 through 7 of port 0. When this pin is high, port 0 and port 1 are not merged, and each operates as a single x4 port.
P23MERGEN	I	**Port 2 and 3 Merge.** P23MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 2 is merged with port 3 to form a single x8 port. The Serdes lanes associated with port 3 become lanes 4 through 7 of port 2. When this pin is high, port 2 and port 3 are not merged, and each operates as a single x4 port.
P45MERGEN	I	**Port 4 and 5 Merge.** P45MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 4 is merged with port 5 to form a single x8 port. The Serdes lanes associated with port 5 become lanes 4 through 7 of port 4. When this pin is high, port 4 and port 5 are not merged, and each operates as a single x4 port.

Table 6 System Pins (Part 1 of 2)

Signal	Type	Name/Description
PERSTN	I	**Fundamental Reset.** Assertion of this signal resets all logic inside the PES34H16G2 and initiates a PCI Express fundamental reset.
RSTHALT	I	**Reset Halt.** When this signal is asserted during a PCI Express fundamental reset, the PES34H16G2 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the PA_SWCTL register by an SMBus master.
SWMODE[3:0]	I	**Switch Mode.** These configuration pins determine the PES34H16G2 switch operating mode. **Note:** These pins should be static and not change following the negation of PERSTN. 0x0 - Single partition 0x1 - Single partition with Serial EEPROM initialization 0x2 through 0x7 - Reserved 0x8 - Single partition with port 0 selected as the upstream port (port 2 disabled) 0x9 - Single partition with port 2 selected as the upstream port (port 0 disabled) 0xA - Single partition with Serial EEPROM initialization and port 0 selected as the upstream port (port 2 disabled) 0xB - Single partition with Serial EEPROM initialization and port 2 selected as the upstream port (port 0 disabled) 0xC - Multi-partition 0xD - Multi-partition with Serial EEPROM initialization 0xE - Reserved 0xF - Reserved

Table 6 System Pins (Part 2 of 2)

Signal	Type	Name/Description
JTAG_TCK	I	**JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input**. This is the serial data input to the boundary scan logic or JTAG Controller.
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	**JTAG Reset**. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 7 Test Pins

Signal	Type	Name/Description
REFRES00	I/O	**Port 0 External Reference Resistor.** Provides a reference for the Port 0 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES01	I/O	**Port 1 External Reference Resistor.** Provides a reference for the Port 1 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES02	I/O	**Port 2 External Reference Resistor.** Provides a reference for the Port 2 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES30	I/O	**Port 3 External Reference Resistor.** Provides a reference for the Port 3 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES04	I/O	**Port 4 External Reference Resistor.** Provides a reference for the Port 4 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES05	I/O	**Port 5 External Reference Resistor.** Provides a reference for the Port 5 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES06	I/O	**Port 6 External Reference Resistor.** Provides a reference for the Port 6 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES07	I/O	**Port 7 External Reference Resistor.** Provides a reference for the Port 7 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES08	I/O	**Port 8 External Reference Resistor.** Provides a reference for the Port 8 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES09	I/O	**Port 9 External Reference Resistor.** Provides a reference for the Port 9 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES10	I/O	**Port 10 External Reference Resistor.** Provides a reference for the Port 10 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES11	I/O	**Port 11 External Reference Resistor.** Provides a reference for the Port 11 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES12	I/O	**Port 12 External Reference Resistor.** Provides a reference for the Port 12 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES13	I/O	**Port 13 External Reference Resistor.** Provides a reference for the Port 13 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES14	I/O	**Port 14 External Reference Resistor.** Provides a reference for the Port 14 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.

Table 8 Power, Ground, and SerDes Resistor Pins (Part 1 of 2)

Signal	Type	Name/Description
REFRES15	I/O	**Port 15 External Reference Resistor.** Provides a reference for the Port 15 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRESPLL	I/O	**PLL External Reference Resistor.** Provides a reference for the PLL bias currents and PLL calibration circuitry. A 3K Ohm +/- 1% resistor should be connected from this pin to ground.
V_{DD}CORE	I	**Core V_{DD}.** Power supply for core logic (1.0V).
V_{DD}I/O	I	**I/O V_{DD}.** LVTTL I/O buffer power supply (2.5V or preferred 3.3V).
V_{DD}PEA	I	**PCI Express Analog Power.** Serdes analog power supply (1.0V).
V_{DD}PEHA	I	**PCI Express Analog High Power.** Serdes analog power supply (2.5V).
V_{DD}PETA	I	**PCI Express Transmitter Analog Voltage.** Serdes transmitter analog power supply (1.0V).
V_{SS}	I	**Ground.**

Table 8 Power, Ground, and SerDes Resistor Pins (Part 2 of 2)

Pin Characteristics

Note: Some input pads of the switch do not contain internal pull-ups or pull-downs. Unused SMBus and System inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, floating pins can cause a slight increase in power consumption. Unused Serdes (Rx and Tx) pins should be left floating. Finally, No Connection pins should not be connected.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
PCI Express Interface	PE00RN[3:0]	I	PCIe differential[2]	Serial Link		
	PE00RP[3:0]	I				
	PE00TN[3:0]	O				
	PE00TP[3:0]	O				
	PE01RN[3:0]	I				
	PE01RP[3:0]	I				
	PE01TN[3:0]	O				
	PE01TP[3:0]	O				
	PE02RN[3:0]	I				
	PE02RP[3:0]	I				
	PE02TN[3:0]	O				
	PE02TP[3:0]	O				
	PE03RN[3:0]	I				
	PE03RP[3:0]	I				
	PE03TN[3:0]	O				
	PE03TP[3:0]	O				
	PE04RN[3:0]	I				
	PE04RP[3:0]	I				
	PE04TN[3:0]	O				
	PE04TP[3:0]	O				
	PE05RN[3:0]	I				
	PE05RP[3:0]	I				
	PE05TN[3:0]	O				
	PE05TP[3:0]	O				
	PE06RN[0]	I				
	PE06RP[0]	I				
	PE06TN[0]	O				
	PE06TP[0]	O				
	PE07RN[0]	I				
	PE07RP[0]	I				
	PE07TN[0]	O				
	PE07TP[0]	O				
	PE08RN[0]	I				

Table 9 Pin Characteristics (Part 1 of 4)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
PCI Express Interface (cont.)	PE08RP[0]	I	PCIe differential	Serial Link		
	PE08TN[0]	O				
	PE08TP[0]	O				
	PE09RN[0]	I				
	PE09RP[0]	I				
	PE09TN[0]	O				
	PE09TP[0]	O				
	PE10RN[0]	I				
	PE10RP[0]	I				
	PE10TN[0]	O				
	PE10TP[0]	O				
	PE11RN[0]	I				
	PE11RP[0]	I				
	PE11TN[0]	O				
	PE11TP[0]	O				
	PE12RN[0]	I				
	PE12RP[0]	I				
	PE12TN[0]	O				
	PE12TP[0]	O				
	PE13RN[0]	I				
	PE13RP[0]	I				
	PE13TN[0]	O				
	PE13TP[0]	O				
	PE14RN[0]	I				
	PE14RP[0]	I				
	PE14TN[0]	O				
	PE14TP[0]	O				
	PE15RN[0]	I				
	PE15RP[0]	I				
	PE15TN[0]	O				
	PE15TP[0]	O				
	GCLKN[1:0]	I	HCSL	Diff. Clock Input		Refer to Table 10
	GCLKP[1:0]	I				

Table 9 Pin Characteristics (Part 2 of 4)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
SMBus	MSMBADDR[4:1]	I	LVTTL		pull-down	
	MSMBCLK	I/O		STI[3]		
	MSMBDAT	I/O		STI		
	SSMBADDR[5,3:1]	I			pull-up	
	SSMBCLK	I/O		STI		
	SSMBDAT	I/O		STI		
General Purpose I/O	GPIO[31:0]	I/O	LVTTL		pull-up	
System Pins	CLKMODE[1:0]	I	LVTTL	Input	pull-up	
	GCLKFSEL	I			pull-down	
	MSMBSMODE	I			pull-down	
	P01MERGEN	I			pull-down	
	P23MERGEN	I			pull-down	
	P45MERGEN	I			pull-down	
	PERSTN	I		STI		
	RSTHALT	I		Input	pull-down	
	SWMODE[3:0]	I			pull-down	
EJTAG / JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I		STI	pull-up	
	JTAG_TDO	O				
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I		STI	pull-up	External pull-down
SerDes Reference Resistors	REFRES00	I/O	Analog			
	REFRES01	I/O				
	REFRES02	I/O				
	REFRES03	I/O				
	REFRES04	I/O				
	REFRES05	I/O				
	REFRES06	I/O				
	REFRES07	I/O				
	REFRES08	I/O				
	REFRES09	I/O				
	REFRES10	I/O				
	REFRES11	I/O				
	REFRES12	I/O				
	REFRES13	I/O				

Table 9 Pin Characteristics (Part 3 of 4)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
SerDes Reference Resistors (Cont.)	REFRES14	I/O	Analog			
	REFRES15	I/O				
	REFRESPLL	I/O				

Table 9 Pin Characteristics (Part 4 of 4)

1. Internal resistor values under typical operating conditions are 92K Ω for pull-up and 91K Ω for pull-down.

2. All receiver pins set the DC common mode voltage to ground. All transmitters must be AC coupled to the media.

3. Schmitt Trigger Input (STI).

Logic Diagram — PES34H16G2

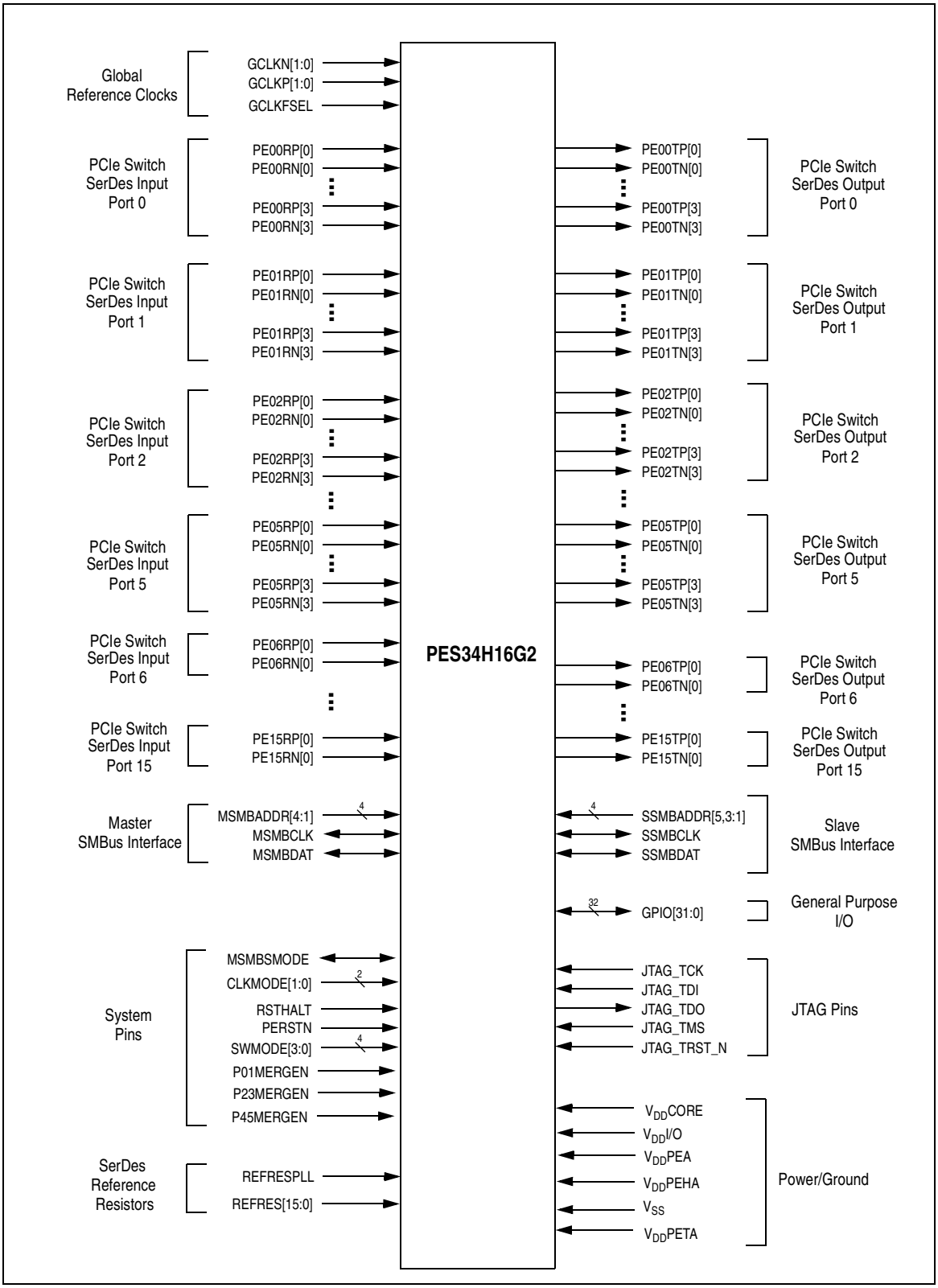


Figure 4 PES34H16G2 Logic Diagram

System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 14 and 15.

Parameter	Description	Condition	Min	Typical	Max	Unit
$Refclk_{FREQ}$	Input reference clock frequency range		100		125[1]	MHz
T_{C-RISE}	Rising edge rate	Differential	0.6		4	V/ns
T_{C-FALL}	Falling edge rate	Differential	0.6		4	V/ns
V_{IH}	Differential input high voltage	Differential	+150			mV
V_{IL}	Differential input low voltage	Differential			-150	mV
V_{CROSS}	Absolute single-ended crossing point voltage	Single-ended	+250		+550	mV
$V_{CROSS-DELTA}$	Variation of V_{CROSS} over all rising clock edges	Single-ended			+140	mV
V_{RB}	Ring back voltage margin	Differential	-100		+100	mV
T_{STABLE}	Time before V_{RB} is allowed	Differential	500			ps
$T_{PERIOD-AVG}$	Average clock period accuracy		-300		2800	ppm
$T_{PERIOD-ABS}$	Absolute period, including spread-spectrum and jitter		9.847		10.203	ns
$T_{CC-JITTER}$	Cycle to cycle jitter				150	ps
V_{MAX}	Absolute maximum input voltage				+1.15	V
V_{MIN}	Absolute minimum input voltage		-0.3			V
Duty Cycle	Duty cycle		40		60	%
Rise/Fall Matching	Single ended rising Refclk edge rate versus falling Refclk edge rate			20		%
Z_{C-DC}	Clock source output DC impedance		40		60	Ω

Table 10 Input Clock Requirements

1. The input clock frequency will be either 100 or 125 MHz depending on signal GCLKFSEL.

AC Timing Characteristics

Parameter	Description	Gen 1			Gen 2			Units
		Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]	
PCIe Transmit								
UI	Unit Interval	399.88	400	400.12	199.94	200	200.06	ps
T_{TX-EYE}	Minimum Tx Eye Width	0.75			0.75			UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.125				UI
$T_{TX-RISE}$, $T_{TX-FALL}$	TX Rise/Fall Time: 20% - 80%	0.125			0.15			UI
$T_{TX-IDLE-MIN}$	Minimum time in idle	20			20			UI

Table 11 PCIe AC Timing Characteristics (Part 1 of 2)

Parameter	Description	Gen 1			Gen 2			Units
		Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]	
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Idle after sending an Idle ordered set			8			8	ns
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition from valid idle to diff data			8			8	ns
$T_{TX-SKEW}$	Transmitter data skew between any 2 lanes			1.3			1.3	ns
$T_{MIN-PULSED}$	Minimum Instantaneous Lone Pulse Width	NA			0.9			UI
$T_{TX-HF-DJ-DD}$	Transmitter Deterministic Jitter > 1.5MHz Bandwidth	NA					0.15	UI
$T_{RF-MISMATCH}$	Rise/Fall Time Differential Mismatch	NA					0.1	UI
PCIe Receive								
UI	Unit Interval	399.88	400	400.12	199.94		200.06	ps
$T_{RX-EYE\ (with\ jitter)}$	Minimum Receiver Eye Width (jitter tolerance)	0.4			0.4			UI
$T_{RX-EYE-MEDIUM\ TO\ MAX\ JITTER}$	Max time between jitter median & max deviation			0.3				UI
$T_{RX-SKEW}$	Lane to lane input skew			20			8	ns
$T_{RX-HF-RMS}$	1.5 — 100 MHz RMS jitter (common clock)	NA					3.4	ps
$T_{RX-HF-DJ-DD}$	Maximum tolerable DJ by the receiver (common clock)	NA					88	ps
$T_{RX-LF-RMS}$	10 KHz to 1.5 MHz RMS jitter (common clock)	NA					4.2	ps
$T_{RX-MIN-PULSE}$	Minimum receiver instantaneous eye width	NA			0.6			UI

Table 11 PCIe AC Timing Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 2.0

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[31:0][1]	Tpw_13b[2]	None	50	—	ns	See Figure 5.

Table 12 GPIO AC Timing Characteristics

1. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

2. The values for this symbol were determined by calculation, not by testing.

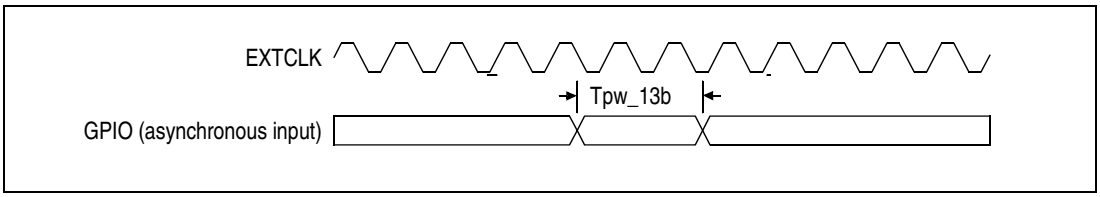


Figure 5 GPIO AC Timing Waveform

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	50.0	—	ns	See Figure 6.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	20	ns	
	Tdz_16c[2]		—	20	ns	
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	ns	

Table 13 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

2. The values for this symbol were determined by calculation, not by testing.

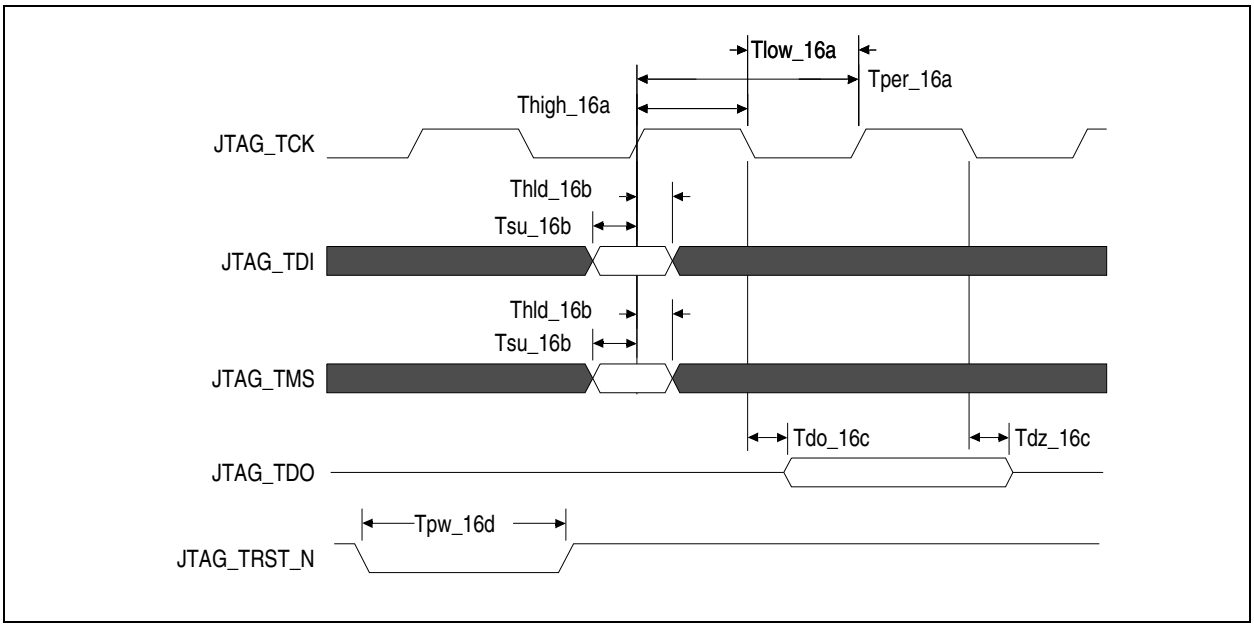


Figure 6 JTAG AC Timing Waveform

Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}CORE	Internal logic supply	0.9	1.0	1.1	V
V_{DD}I/O	I/O supply except for SerDes	2.25	2.5	2.75	V
		3.125	3.3	3.465	V
V_{DD}PEA[1]	PCI Express Analog Power	0.95	1.0	1.1	V
V_{DD}PEHA[2]	PCI Express Analog High Power	2.25	2.5	2.75	V
V_{DD}PETA[1]	PCI Express Transmitter Analog Voltage	0.95	1.0	1.1	V
V_{SS}	Common ground	0	0	0	V

Table 14 PES34H16G2 Operating Voltages

1. V_{DD}PEA and V_{DD}PETA should have no more than 25m$V_{peak-peak}$ AC power supply noise superimposed on the 1.0V nominal DC value.
2. V_{DD}PEHA should have no more than 50m$V_{peak-peak}$ AC power supply noise superimposed on the 2.5V nominal DC value.

Power-Up/Power-Down Sequence

During power supply ramp-up, V_{DD}CORE must remain at least 1.0V below V_{DD}I/O at all times. There are no other power-up sequence requirements for the various operating supply voltages.

The power-down sequence can occur in any order.

Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 15 PES34H16G2 Operating Temperatures

Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 14 (and also listed below).

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 14 (and also listed below).

Number of active Lanes per Port		Core Supply		PCIe Digital Supply		PCIe Analog Supply		PCIe Transmitter Supply		I/O Supply		Total	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 2.5V	Max 2.75V	Typ 1.0V	Max 1.1V	Typ 2.5V	Max 2.75V	Typ Power	Max Power
Three x8 and ten x1 (Full Swing)	**mA**	3630	6264	1741	2049	805	818	1060	1117	32	40		
	Watts	3.63	6.89	1.74	2.25	2.01	2.25	1.06	1.23	0.08	0.11	8.52	12.73
Three x8 and ten x1 (Half Swing)	**mA**	3630	6264	1497	1762	805	818	551	581	32	40		
	Watts	3.63	6.89	1.50	1.94	2.01	2.25	0.55	0.64	0.08	0.11	7.77	11.83

Table 16 PES34H16G2 Power Consumption — 2.5V I/O

Number of active Lanes per Port		Core Supply		PCIe Digital Supply		PCIe Analog Supply		PCIe Transmitter Supply		I/O Supply		Total	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 2.5V	Max 2.75V	Typ 1.0V	Max 1.1V	Typ 3.3V	Max 3.465V	Typ Power	Max Power
Three x8 and ten x1 (Full Swing)	**mA**	3630	6264	1741	2049	805	818	1060	1117	36	46		
	Watts	3.63	6.89	1.74	2.25	2.01	2.25	1.06	1.23	0.12	0.16	8.56	12.78
Three x8 and ten x1 (Half Swing)	**mA**	3630	6264	1497	1762	805	818	551	581	36	46		
	Watts	3.63	6.89	1.50	1.94	2.01	2.25	0.55	0.64	0.12	0.16	7.81	11.88

Table 17 PES34H16G2 Power Consumption — 3.3V I/O

Note 1: I/O supply of 3.3V is preferred.

Note 2: The above power consumption assumes that all ports are functioning at Gen2 (5.0 GT/S) speeds. Power consumption can be reduced by turning off unused ports through software or through boot EEPROM. Power savings will occur in V_{DD}PEA, V_{DD}PEHA, and V_{DD}PETA. Power savings can be estimated as directly proportional to the number of unused ports, since the power consumption of a turned-off port is close to zero. For example, if 3 ports out of 16 are turned off, then the power savings for each of the above three power rails can be calculated quite simply as 3/16 multiplied by the power consumption indicated in the above table.

Note 3: Using a port in Gen1 mode (2.5GT/S) results in approximately 18% power savings for each power rail: V_{DD}PEA, V_{DD}PEHA, and V_{DD}PETA.

Thermal Considerations

This section describes thermal considerations for the PES34H16G2 ($35X35^2$ FCBGA1156 package). The data in Table 18 below contains information that is relevant to the thermal performance of the PES34H16G2 switch.

Symbol	Parameter	Value	Units	Conditions
$T_{J(max)}$	Junction Temperature	125	°C	Maximum
$T_{A(max)}$	Ambient Temperature	70	°C	Maximum for commercial-rated products
		85	°C	Maximum for industrial-rated products
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	13.0	°C/W	Zero air flow
		6.8	°C/W	1 m/S air flow
		5.8	°C/W	2 m/S air flow
θ_{JB}	Thermal Resistance, Junction-to-Board	2.5	°C/W	
θ_{JC}	Thermal Resistance, Junction-to-Case	0.15	°C/W	
P	Power Dissipation of the Device	12.78	Watts	Maximum

Table 18 Thermal Specifications for PES34H16G2, 35x35mm FCBGA1156 Package

Note: It is important for the reliability of this device in any user environment that the junction temperature not exceed the $T_{J(max)}$ value specified in Table 18. Consequently, the effective junction to ambient thermal resistance (θ_{JA}) for the worst case scenario must be maintained below the value determined by the formula:

$$\theta_{JA} = (T_{J(max)} - T_{A(max)})/P$$

Given that the values of $T_{J(max)}$, $T_{A(max)}$, and P are known, the value of desired θ_{JA} becomes a known entity to the system designer. How to achieve the desired θ_{JA} is left up to the board or system designer, but in general, it can be achieved by adding the effects of θ_{JC} (value provided in Table 18), thermal resistance of the chosen adhesive (θ_{CS}), that of the heat sink (θ_{SA}), amount of airflow, and properties of the circuit board (number of layers and size of the board). It is strongly recommended that users perform their own thermal analysis for their own board and system design scenarios.