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12-lane 3-Port PCI Express® Switch

89HPES12N3A
Data Sheet

Device Overview

The 89HPES12N3A is a member of the IDT PRECISE™ family of PCI Express® switching solutions. The PES12N3A is a 12-lane, 3-port peripheral chip that performs PCI Express packet switching with a feature set optimized for high performance applications such as servers, storage, and communications/networking. It provides connectivity and switching functions between a PCI Express upstream port and two downstream ports and supports switching between downstream ports.

Features

- **High Performance PCI Express Switch**
  - *Twelve 2.5Gbps PCI Express lanes*
  - *Three switch ports*
  - *Upstream port configurable up to x4*
  - *Downstream ports configurable up to x4*
  - *Low-latency cut-through switch architecture*
  - *Support for Max Payload Sizes up to 2048 bytes*
  - *One virtual channel*
  - *Eight traffic classes*
  - *PCI Express Base Specification Revision 1.1 compliant*
- **Flexible Architecture with Numerous Configuration Options**
  - *Automatic per port link width negotiation to x4, x2 or x1*
  - *Automatic lane reversal on all ports*
  - *Automatic polarity inversion on all lanes*
  - *Ability to load device configuration from serial EEPROM*
- **Legacy Support**
  - *PCI compatible INTx emulation*
  - *Bus locking*
- **Highly Integrated Solution**
  - *Requires no external components*
  - *Incorporates on-chip internal memory for packet buffering and queueing*
  - *Integrates twelve 2.5 Gbps embedded SerDes with 8B/10B encoder/decoder (no separate transceivers needed)*
- **Reliability, Availability, and Serviceability (RAS) Features**
  - *Supports ECRC and Advanced Error Reporting*
  - *Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)*
  - *Supports PCI Express Native Hot-Plug, Hot-Swap capable I/O*
  - *Compatible with Hot-Plug I/O expanders used on PC and server motherboards*

Block Diagram

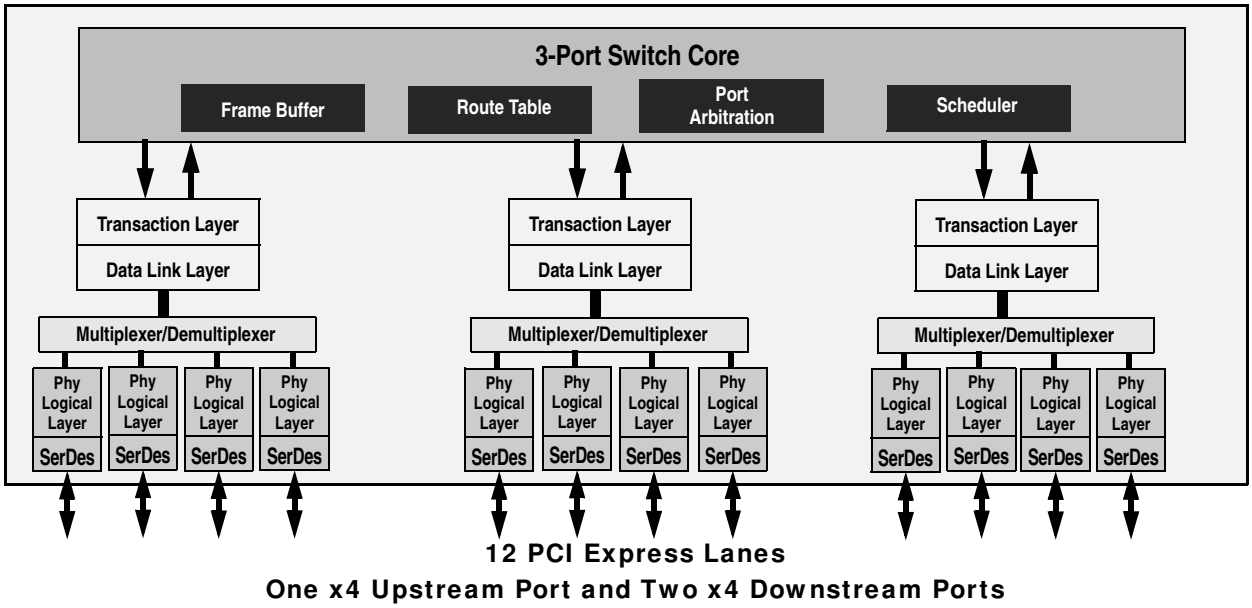


Figure 1 Internal Block Diagram

- **Power Management**
  - *Utilizes advanced low-power design techniques to achieve low typical power consumption*
  - *Supports PCI Power Management Interface specification (PCI-PM 1.1)*
    - *Supports device power management states: D0, $D3_{hot}$ and $D3_{cold}$*
  - *Unused SerDes are disabled*
- **Testability and Debug Features**
  - *Ability to read and write any internal register via the SMBus*
- **Eight General Purpose Input/Output Pins**
  - *Each pin may be individually configured as an input or output*
  - *Each pin may be individually configured as an interrupt input*
  - *Some pins have selectable alternate functions*
- **Packaged in 19x19mm 324-ball BGA with 1mm ball spacing**

Product Description

Utilizing standard PCI Express interconnect, the PES12N3A provides the most efficient I/O connectivity solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides connectivity for up to 3 ports across 12 integrated serial lanes. Each lane provides 2.5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification revision 1.1.

SMBus Interface

The PES12N3A contains two SMBus interfaces. The slave interface provides full access to the configuration registers in the PES12N3A, allowing every configuration register in the device to be read or written by an external agent. The master interface allows the default configuration register values of the PES12N3A to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander.

Six pins make up each of the two SMBus interfaces. These pins consist of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins. In the slave interface, these address pins allow the SMBus address to which the device responds to be configured. In the master interface, these address pins allow the SMBus address of the serial configuration EEPROM from which data is loaded to be configured. The SMBus address is set up on negation of PERSTN by sampling the corresponding address pins. When the pins are sampled, the resulting address is assigned as shown in Table 1.

Bit	Slave SMBus Address	Master SMBus Address
1	SSMBADDR[1]	MSMBADDR[1]
2	SSMBADDR[2]	MSMBADDR[2]
3	SSMBADDR[3]	MSMBADDR[3]

Table 1 Master and Slave SMBus Address Assignment

Bit	Slave SMBus Address	Master SMBus Address
4	0	MSMBADDR[4]
5	SSMBADDR[5]	1
6	1	0
7	1	1

Table 1 Master and Slave SMBus Address Assignment

As shown in Figure 2, the master and slave SMBuses may be used in a unified or split configuration. In the unified configuration, shown in Figure 2(a), the master and slave SMBuses are tied together and the PES12N3A acts both as a SMBus master as well as a SMBus slave on this bus. This requires that the SMBus master or processor that has access to PES12N3A registers supports SMBus arbitration. In some systems, this SMBus master interface may be implemented using general purpose I/O pins on a processor or micro controller, and may not support SMBus arbitration. To support these systems, the PES12N3A may be configured to operate in a split configuration as shown in Figure 2(b).

In the split configuration, the master and slave SMBuses operate as two independent buses and thus multi-master arbitration is never required. The PES12N3A supports reading and writing of the serial EEPROM on the master SMBus via the slave SMBus, allowing in system programming of the serial EEPROM.

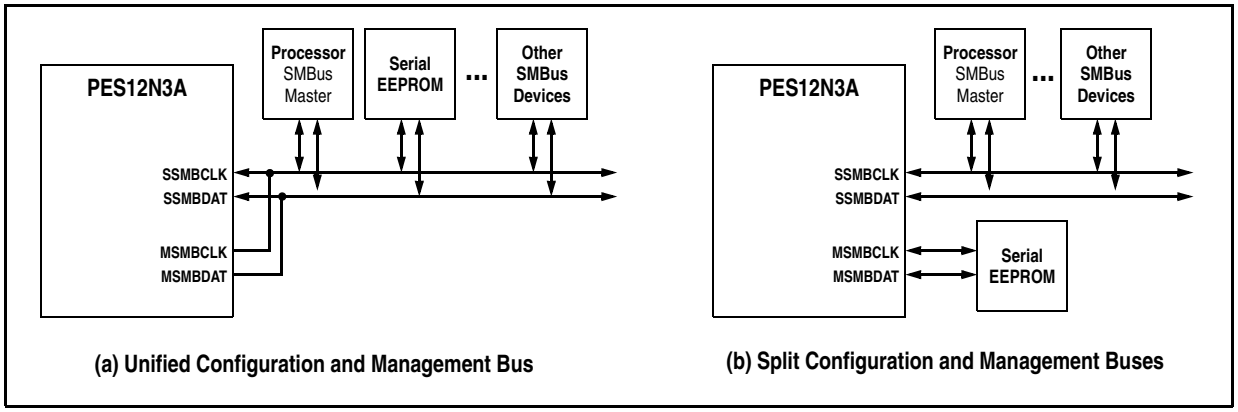


Figure 2 SMBus Interface Configuration Examples

Hot-Plug Interface

The PES12N3A supports PCI Express Hot-Plug on each downstream port. To reduce the number of pins required on the device, the PES12N3A utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES12N3A generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES12N3A. In response to an I/O expander interrupt, the PES12N3A generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

General Purpose Input/Output

The PES12N3A provides eight General Purpose Input/Output (GPIO) pins that may be used by the system designer as bit I/O ports. Each GPIO pin may be configured independently as an input or output through software control. Some GPIO pins are shared with other on-chip functions. These alternate functions may be enabled via software, SMBus slave interface, or serial configuration EEPROM.

The PES12N3A is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 1.1. The PES12N3A can operate either as a store and forward or cut-through switch and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to enable efficient switching and I/O connectivity for servers, storage, and embedded applications.

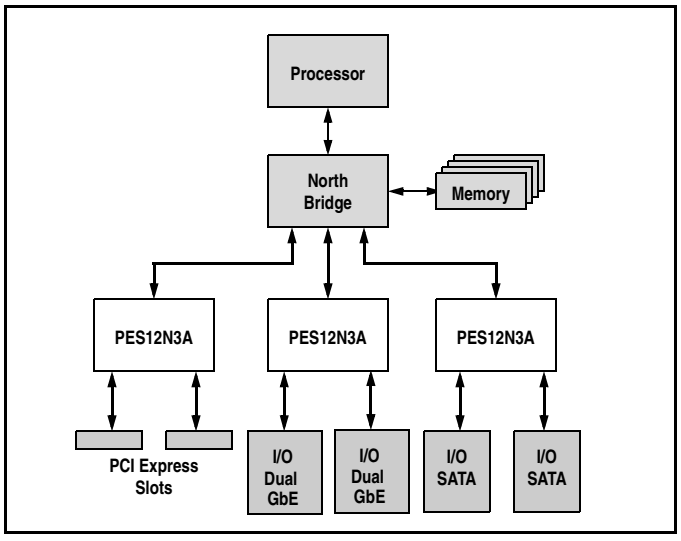


Figure 3 I/O Expansion Application

Pin Description

The following tables list the functions of the pins provided on the PES12N3A. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an "N" are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Note: In the PES12N3A, the two downstream ports are labeled port 2 and port 4.

Signal	Type	Name/Description
PE0RP[3:0] PE0RN[3:0]	I	**PCI Express Port 0 Serial Data Receive.** Differential PCI Express receive pairs for port 0.
PE0TP[3:0] PE0TN[3:0]	O	**PCI Express Port 0 Serial Data Transmit.** Differential PCI Express transmit pairs for port 0.
PE2RP[3:0] PE2RN[3:0]	I	**PCI Express Port 2 Serial Data Receive.** Differential PCI Express receive pairs for port 2.
PE2TP[3:0] PE2TN[3:0]	O	**PCI Express Port 2 Serial Data Transmit.** Differential PCI Express transmit pairs for port 2.
PE4RP[3:0] PE4RN[3:0]	I	**PCI Express Port 4 Serial Data Receive.** Differential PCI Express receive pairs for port 4.
PE4TP[3:0] PE4TN[3:0]	O	**PCI Express Port 4 Serial Data Transmit.** Differential PCI Express transmit pairs for port 4.
PEREFCLKP[2:1] PEREFCLKN[2:1]	I	**PCI Express Reference Clock.** Differential reference clock pair input. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic and on-chip SerDes. The frequency of the differential reference clock is determined by the REFCLKM signal.
REFCLKM	I	**PCI Express Reference Clock Mode Select.** This signal selects the frequency of the reference clock input. 0x0 - 100 MHz 0x1 - 125 MHz

Table 2 PCI Express Interface Pins

Signal	Type	Name/Description
MSMBADDR[4:1]	I	**Master SMBus Address.** These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded.
MSMBCLK	I/O	**Master SMBus Clock.** This bidirectional signal is used to synchronize transfers on the master SMBus. It is active and generating the clock only when the EEPROM or I/O Expanders are being accessed.
MSMBDAT	I/O	**Master SMBus Data.** This bidirectional signal is used for data on the master SMBus.
SSMBADDR[5,3:1]	I	**Slave SMBus Address.** These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	**Slave SMBus Clock.** This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	**Slave SMBus Data.** This bidirectional signal is used for data on the slave SMBus.

Table 3 SMBus Interface Pins

Signal	Type	Name/Description
GPIO[0]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P2RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 2
GPIO[1]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P4RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 4
GPIO[2]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN0 Alternate function pin type: Input Alternate function: I/O Expander interrupt 0 input
GPIO[3]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[4]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN2 Alternate function pin type: Input Alternate function: I/O Expander interrupt 2 input
GPIO[5]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[6]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[7]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: GPEN Alternate function pin type: Output Alternate function: General Purpose Event (GPE) output

Table 4 General Purpose I/O Pins

Signal	Type	Name/Description
CCLKDS	I	**Common Clock Downstream.** When the CCLKDS pin is asserted, it indicates that a common clock is being used between the downstream device and the downstream port.
CCLKUS	I	**Common Clock Upstream.** When the CCLKUS pin is asserted, it indicates that a common clock is being used between the upstream device and the upstream port.
MSMBSMODE	I	**Master SMBus Slow Mode.** The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 KHz. This value may not be overridden.

Table 5 System Pins (Part 1 of 2)

Signal	Type	Name/Description
PERSTN	I	**Fundamental Reset.** Assertion of this signal resets all logic inside the PES12N3A and initiates a PCI Express fundamental reset.
RSTHALT	I	**Reset Halt.** When this signal is asserted during a PCI Express fundamental reset, the PES12N3A executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the SWCTL register by an SMBus master.
SWMODE[3:0]	I	**Switch Mode.** These configuration pins determine the PES12N3A switch operating mode. These pins should be static and not change after the negation of PERSTN. 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM initialization 0x2 - through 0xF Reserved

Table 5 System Pins (Part 2 of 2)

Signal	Type	Name/Description
JTAG_TCK	I	**JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input**. This is the serial data input to the boundary scan logic or JTAG Controller.
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	**JTAG Reset**. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 6 Test Pins

Signal	Type	Name/Description
V_{DD}CORE	I	**Core V_{DD}.** Power supply for core logic.
V_{DD}IO	I	**I/O V_{DD}.** LVTTL I/O buffer power supply.
V_{DD}PE	I	**PCI Express Digital Power.** PCI Express digital power used by the digital power of the SerDes.

Table 7 Power and Ground Pins

Signal	Type	Name/Description
$V_{DD}APE$	I	**PCI Express Analog Power.** PCI Express analog power used by the PLL and bias generator.
$V_{TT}PE$	I	**PCI Express Termination Power.**
V_{SS}	I	Ground.

Table 7 Power and Ground Pins

Pin Characteristics

Note: Some input pads of the PES12N3A do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
PCI Express Interface	PE0RN[3:0]	I	CML	Serial link		
	PE0RP[3:0]	I				
	PE0TN[3:0]	O				
	PE0TP[3:0]	O				
	PE2RN[3:0]	I				
	PE2RP[3:0]	I				
	PE2TN[3:0]	O				
	PE2TP[3:0]	O				
	PE4RN[3:0]	I				
	PE4RP[3:0]	I				
	PE4TN[3:0]	O				
	PE4TP[3:0]	O				
	PEREFCLKN[2:1]	I	LVPECL/ CML	Diff. Clock Input		Refer to Table 9
	PEREFCLKP[2:1]	I				
	REFCLKM	I	LVTTL	Input	pull-down	
SMBus	MSMBADDR[4:1]	I	LVTTL	Input	pull-up	
	MSMBCLK	I/O		STI[2]		pull-up on board
	MSMBDAT	I/O		STI		pull-up on board
	SSMBADDR[5,3:1]	I		Input	pull-up	
	SSMBCLK	I/O		STI		pull-up on board
	SSMBDAT	I/O		STI		pull-up on board
General Purpose I/O	GPIO[7:0]	I/O	LVTTL	High Drive	pull-up	
System Pins	CCLKDS	I	LVTTL	Input	pull-up	
	CCLKUS	I			pull-up	
	MSMBSMODE	I			pull-down	
	PERSTN	I				
	RSTHALT	I			pull-down	
	SWMODE[3:0]	I			pull-down	

Table 8 Pin Characteristics (Part 1 of 2)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I		STI	pull-up	
	JTAG_TDO	O				
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I		STI	pull-up	External pull-down

Table 8 Pin Characteristics (Part 2 of 2)

1. Internal resistor values under typical operating conditions are 54K Ω for pull-up and 251K Ω for pull-down.

2. Schmitt Trigger Input (STI).

Logic Diagram — PES12N3A

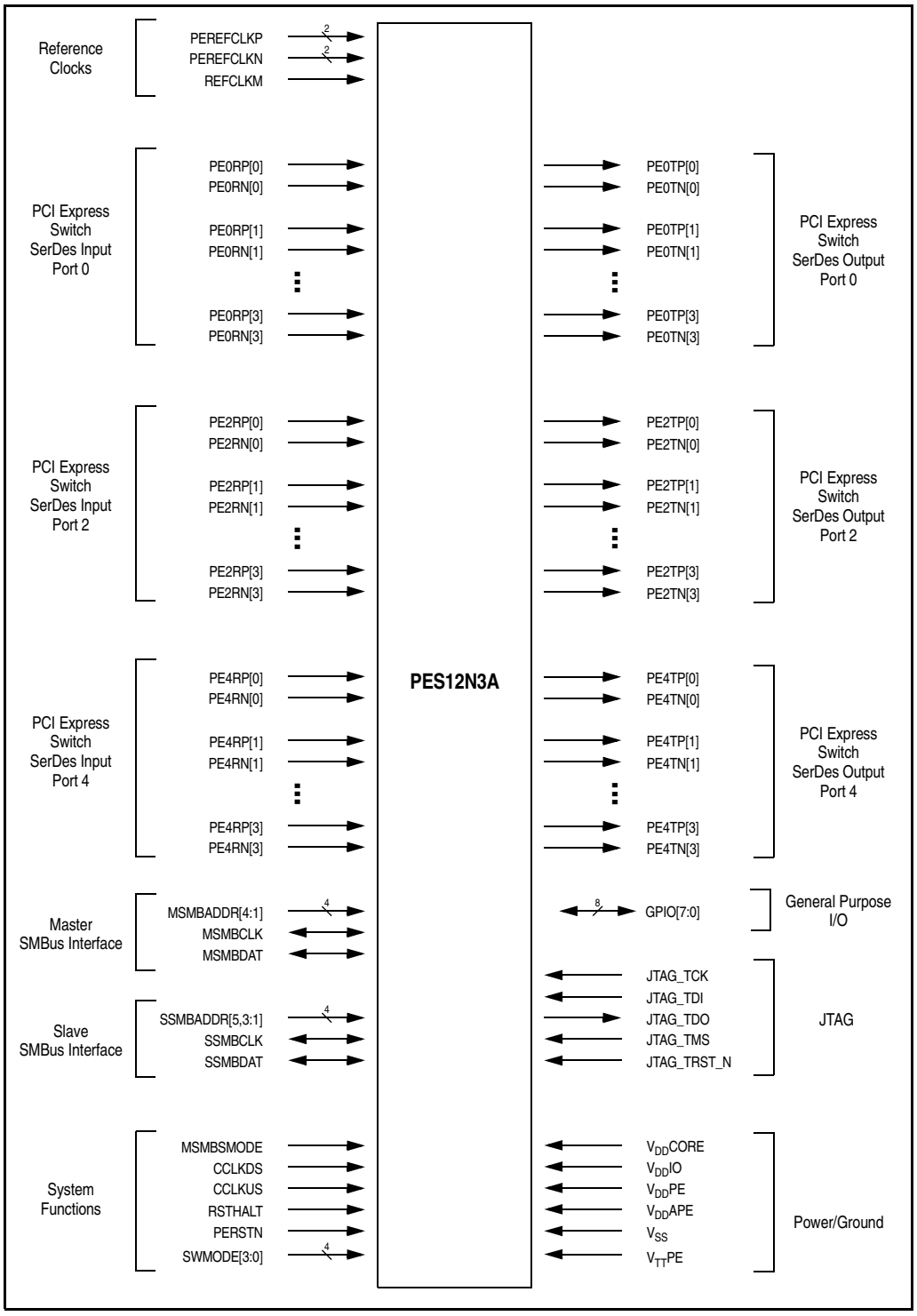


Figure 4 PES12N3A Logic Diagram

System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 13 and 14.

Parameter	Description	Min	Typical	Max	Unit
$Refclk_{FREQ}$	Input reference clock frequency range	100		125[1]	MHz
$Refclk_{DC}$[2]	Duty cycle of input clock	40	50	60	%
T_R, T_F	Rise/Fall time of input clocks			0.2*RCUI	RCUI[3]
V_{SW}	Differential input voltage swing[4]	0.6		1.6	V
T_{jitter}	Input clock jitter (cycle-to-cycle)			125	ps
R_T	Termination Resistor		110		Ohms

Table 9 Input Clock Requirements

1. The input clock frequency will be either 100 or 125 MHz depending on signal REFCLKM.
2. ClkIn must be AC coupled. Use 0.01 — 0.1 µF ceramic capacitors.
3. RCUI (Reference Clock Unit Interval) refers to the reference clock period.
4. AC coupling required.

AC Timing Characteristics

Parameter	Description	Min[1]	Typical[1]	Max[1]	Units
PCIe Transmit					
UI	Unit Interval	399.88	400	400.12	ps
T_{TX-EYE}	Minimum Tx Eye Width	0.7	.9		UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.15	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+ / D- Tx output rise/fall time	50	90		ps
$T_{TX- IDLE-MIN}$	Minimum time in idle	50			UI
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Idle after sending an Idle ordered set			20	UI
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition from valid idle to diff data			20	UI
$T_{TX-SKEW}$	Transmitter data skew between any 2 lanes		500	1300	ps
PCIe Receive					
UI	Unit Interval	399.88	400	400.12	ps
T_{RX-EYE} (with jitter)	Minimum Receiver Eye Width (jitter tolerance)	0.4			UI

Table 10 PCIe AC Timing Characteristics (Part 1 of 2)

Parameter	Description	Min[1]	Typical[1]	Max[1]	Units
$T_{RX-EYE-MEDIUM\ TO\ MAX\ JITTER}$	Max time between jitter median & max deviation			0.3	UI
$T_{RX-IDLE-DET-DIFF-ENTER\ TIME}$	Unexpected Idle Enter Detect Threshold Integration Time			10	ms
$T_{RX-SKEW}$	Lane to lane input skew			20	ns

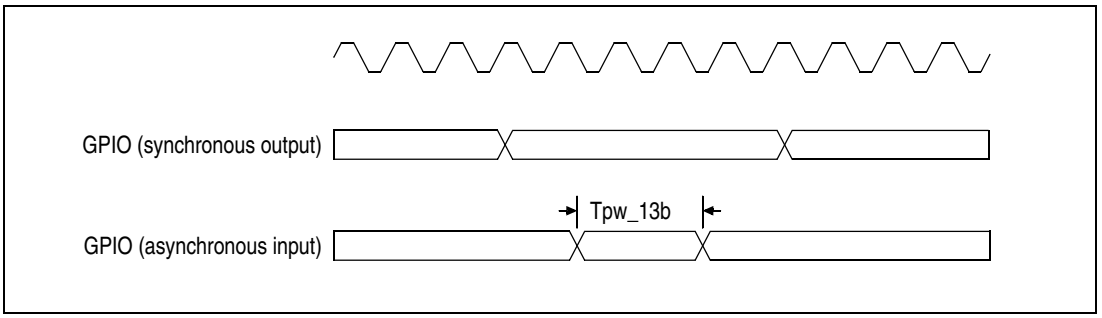
Table 10 PCIe AC Timing Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.1

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[7:0][1]	Tpw_13b[2]	None	50	—	ns	

Table 11 GPIO AC Timing Characteristics

1. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.
2. The values for this symbol were determined by calculation, not by testing.



Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	50.0	—	ns	See Figure 5.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	20	ns	
	Tdz_16c[2]		—	20	ns	
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	ns	

Table 12 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

2. The values for this symbol were determined by calculation, not by testing.

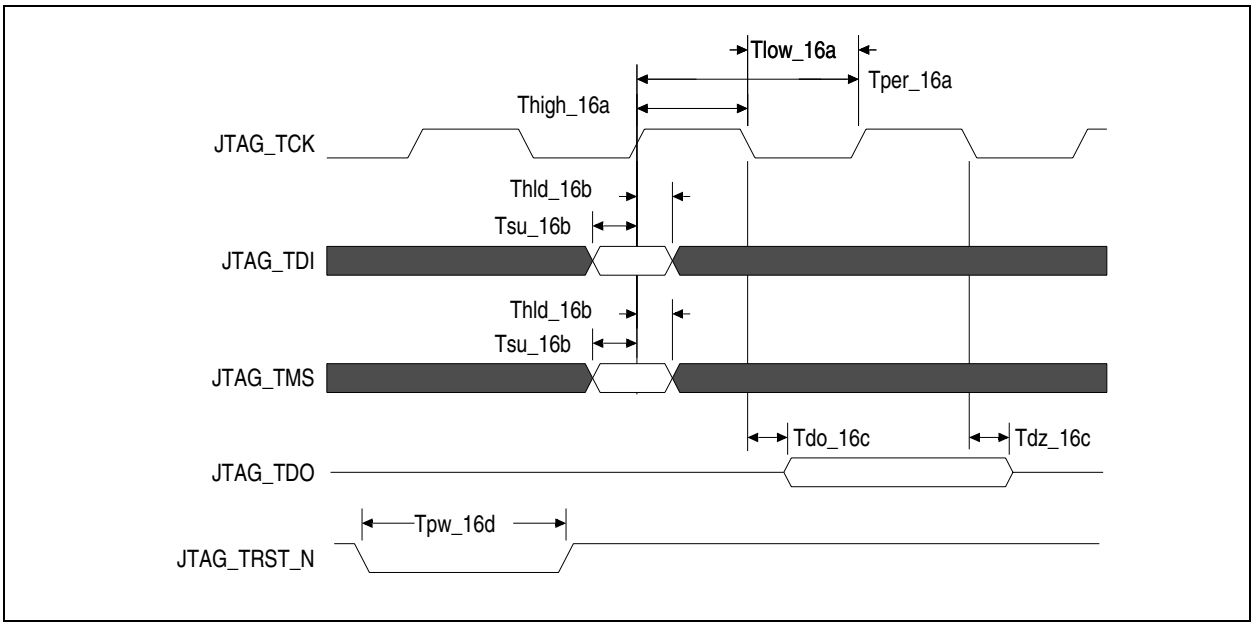


Figure 5 JTAG AC Timing Waveform

Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}CORE	Internal logic supply	0.9	1.0	1.1	V
V_{DD}I/O	I/O supply except for SerDes LVPECL/CML	3.0	3.3	3.6	V
V_{DD}PE	PCI Express Digital Power	0.9	1.0	1.1	V
V_{DD}APE	PCI Express Analog Power	0.9	1.0	1.1	V
V_{TT}PE	PCI Express Serial Data Transmit Termination Voltage	1.425	1.5	1.575	V
V_{SS}	Common ground	0	0	0	V

Table 13 PES12N3A Operating Voltages

Power-Up Sequence

This section describes the sequence in which various voltages must be applied to the part during power-up to ensure proper functionality. For the PES12N3A, the power-up sequence must be as follows:

1. V_{DD}I/O — 3.3V
2. V_{DD}Core, V_{DD}PE, V_{DD}APE — 1.0V
3. V_{TT}PE — 1.5V

When powering up, each voltage level must ramp and stabilize prior to applying the next voltage in the sequence to ensure internal latch-up issues are avoided. There are no maximum time limitations in ramping to valid power levels. The power-down sequence must be in the reverse order of the power-up sequence.

Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 14 PES12N3A Operating Temperatures

Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 13 (and also listed below).

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 13 (and also listed below).

Number of active Lanes per Port		Core Supply		PCIe Digital Supply		PCIe Analog Supply		PCIe Termination Supply		I/O Supply		Total	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 1.5V	Max 1.575V	Typ 3.3V	Max 3.6V	Typ Power	Max Power
4/4/4	mA	723	928	578	693	223	251	291	345	1	1	1.96W	2.6W
	Watts	0.72	1.02	0.58	0.76	0.22	0.28	0.44	0.54	0.004	0.004		
4/1/1	mA	618	746	398	458	207	223	142	160	1	1	1.44W	1.8W
	Watts	0.62	0.82	0.4	0.5	0.21	0.25	0.21	0.25	0.003	0.003		

Table 15 PES12N3A Power Consumption

Thermal Considerations

This section describes thermal considerations for the PES12N3A (19mm^2 BCG324 package). The data in Table 16 below contains information that is relevant to the thermal performance of the PES12N3A switch.

Symbol	Parameter	Value	Units	Conditions
$T_{J(max)}$	Junction Temperature	125	^{0}C	Maximum
$T_{A(max)}$	Ambient Temperature	70	^{0}C	Maximum for commercial-rated products
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	21.8	^{0}C/W	Zero air flow
		15.1	^{0}C/W	1 m/S air flow
		13.9	^{0}C/W	2 m/S air flow
θ_{JB}	Thermal Resistance, Junction-to-Board	11.4	^{0}C/W	
θ_{JC}	Thermal Resistance, Junction-to-Case	5.1	^{0}C/W	
P	Power Dissipation of the Device	2.6	Watts	Maximum

Table 16 Thermal Specifications for PES12N3A, 19x19 mm BCG324 Package

Note: The parameter $\theta_{JA(eff)}$ is not the *absolute* thermal resistance for the package as defined by JEDEC (JESD-51). Because resistance can vary with the number of board layers, size of the board, and airflow, $\theta_{JA(eff)}$ is the *effective* thermal resistance. The values for effective θ_{JA} given above are based on a 10-layer, standard height, full length (4.3"x12.2") PCIe add-in card.

Heat Sink

Table 17 lists heat sink requirements for the PES12N3A under three common usage scenarios. As shown in this table, a heat sink is not required in most cases.

Air Flow	Board Size	Board Layers	Heat Sink Requirement
Zero	4.3"x12.2" (standard height, full length form factor) or larger	4 or more	No heat sink required
Zero	Any	6 or more	No heat sink required
1 m/S or more	Any	Any	No heat sink required

Table 17 Heat Sink Requirements Based on Air Flow and Board Characteristics

Thermal Usage Examples

The junction-to-ambient thermal resistance is a measure of a device's ability to dissipate heat from the die to its surroundings in the absence of a heat sink. The general formula to determine θ_{JA} is:

$$\theta_{JA} = (T_J - T_A)/P$$

Thermal reliability of a device is generally assured when the actual value of T_J in the specific system environment being considered is less than the maximum T_J specified for the device. Using an ambient temperature of 70°C and assuming a system with 1m/S airflow, the actual value of T_J is:

$$T_{J(actual)} = T_A + P * \theta_{JA(eff)} = 70^oC + 2.6W * 9.9W/^oC = 96^oC$$

The actual T_J of 96°C is well below the maximum T_J of 125°C specified for the device (shown in Table 16). Therefore, no heat sink is needed in this scenario. The formula is also useful from a system design perspective. It can be used to determine if a heat sink should be added to the device based on some desired value of T_J. For example, if for reliability purposes the desired T_J is 100°C, then the maximum allowable T_A is:

$$T_{A(allowed)} = T_{J(desired)} - (P * \theta_{JA(effective)})$$

$$T_{A(allowed)} = 100^oC - (2.6W * 9.9W/^oC) = 100^oC - 26^oC = 74^oC$$

An appropriate level of increased air flow and/or a heat sink can be added to achieve this lower ambient temperature Please contact ssdhelp@idt.com for further assistance.

DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 13.

Note: See Table 8, Pin Characteristics, for a complete I/O listing.

I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Serial Link	**PCIe Transmit**						
	$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	800		1200	mV	
	$V_{TX-DE-RATIO}$	De-emphasized differential output voltage	-3		-4	dB	
	$V_{TX-DC-CM}$	DC Common mode voltage	-0.1	1	3.7	V	
	$V_{TX-CM-ACP}$	RMS AC peak common mode output voltage			20	mV	
	$V_{TX-CM-DC-active-idle-delta}$	Abs delta of DC common mode voltage between L0 and idle			100	mV	
	$V_{TX-CM-DC-line-delta}$	Abs delta of DC common mode voltage between D+ and D-			25	mV	
	$V_{TX-Idle-DiffP}$	Electrical idle diff peak output			20	mV	
	$V_{TX-RCV-Detect}$	Voltage change during receiver detection			600	mV	
	$RL_{TX-DIFF}$	Transmitter Differential Return loss	12			dB	
	RL_{TX-CM}	Transmitter Common Mode Return loss	6			dB	
	$Z_{TX-DEFF-DC}$	DC Differential TX impedance	80	100	120	Ω	
	Z_{OSE}	Single ended TX Impedance	40	50	60	Ω	
	Transmitter Eye Diagram	TX Eye Height (De-emphasized bits)	505	650		mV	
	Transmitter Eye Diagram	TX Eye Height (Transition bits)	800	950		mV	
	PCIe Receive						
	$V_{RX-DIFFp-p}$	Differential input voltage (peak-to-peak)	175		1200	mV	
	$V_{RX-CM-AC}$	Receiver common-mode voltage for AC coupling			150	mV	
	$RL_{RX-DIFF}$	Receiver Differential Return Loss	15			dB	
	RL_{RX-CM}	Receiver Common Mode Return Loss	6			dB	
	$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	Ω	
	$Z_{RX-COMM-DC}$	Single-ended input impedance	40	50	60	Ω	
	$Z_{RX-COMM-HIGH-Z-DC}$	Powered down input common mode impedance (DC)	200k	350k		Ω	
	$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	mV	
PCIe REFCLK							
	C_{IN}	Input Capacitance	1.5	—		pF	

Table 18 DC Electrical Characteristics (Part 1 of 2)

I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Other I/Os							
LOW Drive Output	I_{OL}		—	2.5	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-5.5	—	mA	V_{OH} = 1.5V
High Drive Output	I_{OL}		—	12.0	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-20.0	—	mA	V_{OH} = 1.5V
Schmitt Trigger Input (STI)	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}IO+ 0.5	V	—
Input	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}IO+ 0.5	V	—
Capacitance	C_{IN}		—	—	8.5	pF	—
Leakage	Inputs		—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/downs		—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ WITH}$ Pull-ups/downs		—	—	± 80	µA	V_{DD}I/O (max)

Table 18 DC Electrical Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.0a.

Package Pinout — 324-BGA Signal Pinout for PES12N3A

The following table lists the pin numbers and signal names for the PES12N3A device.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	V_{SS}		E10	V_{DD}PE		K1	V_{DD}CORE		P10	V_{DD}IO	
A2	V_{SS}		E11	V_{SS}		K2	V_{SS}		P11	V_{DD}IO	
A3	PE0RP03		E12	V_{DD}PE		K3	V_{TT}PE		P12	V_{DD}IO	
A4	V_{DD}CORE		E13	V_{SS}		K4	V_{DD}CORE		P13	V_{DD}IO	
A5	PE0TN03		E14	V_{DD}CORE		K5	V_{DD}PE		P14	V_{DD}IO	
A6	V_{DD}CORE		E15	V_{DD}APE		K6	V_{SS}		P15	V_{SS}	
A7	PE0TP02		E16	V_{SS}		K7	V_{SS}		P16	V_{TT}PE	
A8	V_{DD}CORE		E17	PE4TP03		K8	V_{SS}		P17	V_{SS}	
A9	PE0RN02		E18	PE4TN03		K9	V_{SS}		P18	V_{DD}CORE	
A10	V_{DD}CORE		F1	V_{DD}CORE		K10	V_{SS}		R1	PE2TN03	
A11	PE0RP01		F2	V_{SS}		K11	V_{SS}		R2	PE2TP03	
A12	V_{DD}CORE		F3	V_{DD}CORE		K12	V_{SS}		R3	V_{SS}	
A13	PE0TP01		F4	V_{DD}APE		K13	V_{SS}		R4	V_{DD}IO	
A14	V_{DD}CORE		F5	V_{SS}		K14	V_{SS}		R5	V_{SS}	
A15	V_{DD}CORE		F6	V_{DD}CORE		K15	V_{DD}PE		R6	V_{DD}CORE	
A16	PE0TN00		F7	V_{SS}		K16	V_{TT}PE		R7	MSMBDAT	
A17	V_{SS}		F8	V_{DD}CORE		K17	V_{SS}		R8	SSMBADDR_5	
A18	V_{SS}		F9	V_{SS}		K18	V_{DD}CORE		R9	NC	
B1	V_{DD}CORE		F10	V_{DD}CORE		L1	PE2RN02		R10	SWMODE_2	
B2	V_{DD}CORE		F11	V_{SS}		L2	PE2RP02		R11	RSTHALT	
B3	PE0RN03		F12	V_{SS}		L3	V_{SS}		R12	GPIO_04	1
B4	V_{SS}		F13	V_{DD}PE		L4	V_{DD}PE		R13	V_{DD}CORE	
B5	PE0TP03		F14	V_{SS}		L5	V_{SS}		R14	V_{SS}	
B6	V_{SS}		F15	V_{DD}IO		L6	V_{DD}CORE		R15	V_{DD}IO	
B7	PE0TN02		F16	V_{SS}		L7	V_{DD}CORE		R16	V_{SS}	
B8	V_{SS}		F17	V_{SS}		L8	V_{DD}CORE		R17	PE4TP00	
B9	PE0RP02		F18	V_{DD}CORE		L9	V_{DD}CORE		R18	PE4TN00	
B10	V_{SS}		G1	PE2TP01		L10	V_{DD}CORE		T1	V_{DD}CORE	
B11	PE0RN01		G2	PE2TN01		L11	V_{DD}CORE		T2	V_{SS}	
B12	V_{SS}		G3	V_{SS}		L12	V_{DD}CORE		T3	V_{SS}	
B13	PE0TN01		G4	V_{DD}PE		L13	V_{DD}CORE		T4	JTAG_TCK	
B14	V_{SS}		G5	V_{DD}APE		L14	V_{SS}		T5	JTAG_TDO	
B15	V_{SS}		G6	V_{SS}		L15	V_{DD}PE		T6	MSMBADDR_1	
B16	PE0TP00		G7	V_{SS}		L16	V_{SS}		T7	MSMBCLK	

Table 19 PES12N3A 324-pin Signal Pin-Out (Part 1 of 3)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
B17	V_{DD}CORE		G8	V_{DD}IO		L17	PE4RP01		T8	SSMBADDR_2	
B18	V_{DD}CORE		G9	V_{SS}		L18	PE4RN01		T9	CCLKDS	
C1	PE2RP00		G10	V_{DD}IO		M1	V_{DD}CORE		T10	SWMODE_1	
C2	PE2RN00		G11	V_{SS}		M2	V_{SS}		T11	PERSTN	
C3	V_{SS}		G12	V_{DD}CORE		M3	V_{SS}		T12	GPIO_03	
C4	V_{DD}CORE		G13	V_{SS}		M4	V_{DD}APE		T13	GPIO_07	1
C5	V_{SS}		G14	V_{DD}APE		M5	V_{SS}		T14	V_{SS}	
C6	V_{TT}PE		G15	V_{DD}PE		M6	V_{DD}CORE		T15	REFCLKM	
C7	V_{SS}		G16	V_{SS}		M7	V_{SS}		T16	V_{SS}	
C8	V_{TT}PE		G17	PE4TN02		M8	V_{SS}		T17	V_{SS}	
C9	V_{SS}		G18	PE4TP02		M9	V_{DD}CORE		T18	V_{DD}CORE	
C10	V_{TT}PE		H1	V_{DD}CORE		M10	V_{DD}CORE		U1	PE2RP03	
C11	V_{SS}		H2	V_{SS}		M11	V_{SS}		U2	PE2RN03	
C12	V_{TT}PE		H3	V_{TT}PE		M12	V_{SS}		U3	V_{SS}	
C13	V_{DD}CORE		H4	V_{DD}APE		M13	V_{DD}CORE		U4	JTAG_TDI	
C14	PE0RP00		H5	V_{SS}		M14	V_{SS}		U5	JTAG_TMS	
C15	PE0RN00		H6	V_{SS}		M15	V_{DD}APE		U6	MSMBADDR_2	
C16	V_{DD}CORE		H7	V_{DD}CORE		M16	V_{SS}		U7	MSMBADDR_4	
C17	PE4RN03		H8	V_{SS}		M17	V_{SS}		U8	SSMBADDR_3	
C18	PE4RP03		H9	V_{DD}CORE		M18	V_{DD}CORE		U9	CCLKUS	
D1	V_{DD}CORE		H10	V_{DD}CORE		N1	PE2TP02		U10	SWMODE_0	
D2	V_{SS}		H11	V_{SS}		N2	PE2TN02		U11	NC	
D3	V_{SS}		H12	V_{DD}CORE		N3	V_{TT}PE		U12	GPIO_00	1
D4	V_{DD}CORE		H13	V_{SS}		N4	V_{DD}APE		U13	GPIO_02	1
D5	V_{SS}		H14	V_{DD}APE		N5	V_{SS}		U14	GPIO_06	
D6	V_{DD}APE		H15	V_{DD}PE		N6	V_{SS}		U15	MSMBSMODE	
D7	V_{SS}		H16	V_{TT}PE		N7	V_{SS}		U16	V_{SS}	
D8	V_{DD}APE		H17	V_{SS}		N8	V_{SS}		U17	PE4RN00	
D9	V_{SS}		H18	V_{DD}CORE		N9	V_{SS}		U18	PE4RP00	
D10	V_{DD}APE		J1	PE2RP01		N10	V_{SS}		V1	V_{DD}CORE	
D11	V_{SS}		J2	PE2RN01		N11	V_{SS}		V2	V_{SS}	
D12	V_{DD}APE		J3	V_{SS}		N12	V_{SS}		V3	PEREFCLKP1	
D13	V_{SS}		J4	V_{DD}PE		N13	V_{SS}		V4	PEREFCLKN1	
D14	V_{DD}CORE		J5	V_{SS}		N14	V_{SS}		V5	JTAG_TRST_N	
D15	V_{SS}		J6	V_{DD}CORE		N15	V_{DD}APE		V6	MSMBADDR_3	
D16	V_{SS}		J7	V_{SS}		N16	V_{TT}PE		V7	SSMBADDR_1	
D17	V_{SS}		J8	V_{SS}		N17	PE4TN01		V8	SSMBCLK	

Table 19 PES12N3A 324-pin Signal Pin-Out (Part 2 of 3)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
D18	V_{DD}CORE		J9	V_{DD}CORE		N18	PE4TP01		V9	SSMBDAT	
E1	PE2TN00		J10	V_{DD}CORE		P1	V_{DD}CORE		V10	NC	
E2	PE2TP00		J11	V_{SS}		P2	V_{SS}		V11	SWMODE_3	
E3	V_{DD}CORE		J12	V_{SS}		P3	V_{TT}PE		V12	V_{DD}IO	
E4	V_{SS}		J13	V_{DD}CORE		P4	V_{SS}		V13	GPIO_01	1
E5	V_{DD}CORE		J14	V_{SS}		P5	V_{DD}IO		V14	GPIO_05	
E6	V_{SS}		J15	V_{DD}CORE		P6	V_{DD}IO		V15	PEREFCLKP2	
E7	V_{SS}		J16	V_{SS}		P7	V_{DD}IO		V16	PEREFCLKN2	
E8	V_{DD}PE		J17	PE4RP02		P8	V_{DD}IO		V17	V_{SS}	
E9	V_{SS}		J18	PE4RN02		P9	V_{DD}IO		V18	V_{DD}CORE	

Table 19 PES12N3A 324-pin Signal Pin-Out (Part 3 of 3)

Alternate Signal Functions

Pin	GPIO	Alternate
U12	GPIO_00	P2RSTN
V13	GPIO_01	P4RSTN
U13	GPIO_02	IOEXPINTN0
R12	GPIO_04	IOEXPINTN2
T13	GPIO_07	GPEN

Table 20 PES12N3A Alternate Signal Functions

Power Pins

V_{DD}Core	V_{DD}Core	V_{DD}Core	V_{DD}IO	V_{DD}PE	V_{DD}APE	V_{TT}PE
A4	F3	L8	F15	E8	D6	C6
A6	F6	L9	G8	E10	D8	C8
A8	F8	L10	G10	E12	D10	C10
A10	F10	L11	P5	F13	D12	C12
A12	F18	L12	P6	G4	E15	H3
A14	G12	L13	P7	G15	F4	H16
A15	H1	M1	P8	H15	G5	K3
B1	H7	M6	P9	J4	G14	K16
B2	H9	M9	P10	K5	H4	N3
B17	H10	M10	P11	K15	H14	N16
B18	H12	M13	P12	L4	M4	P3
C4	H18	M18	P13	L15	M15	P16
C13	J6	P1	P14		N4	
C16	J9	P18	R4		N15	
D1	J10	R6	R15			
D4	J13	R13	V12			
D14	J15	T1				
D18	K1	T18				
E3	K4	V1				
E5	K18	V18				
E14	L6					
F1	L7					

Table 21 PES12N3A Power Pins

Ground Pins

V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
A1	D15	G11	K10	N8
A2	D16	G13	K11	N9
A17	D17	G16	K12	N10
A18	E4	H2	K13	N11
B4	E6	H5	K14	N12
B6	E7	H6	K17	N13
B8	E9	H8	L3	N14
B10	E11	H11	L5	P2
B12	E13	H13	L14	P4
B14	E16	H17	L16	P15
B15	F2	J3	M2	P17
C3	F5	J5	M3	R3
C5	F7	J7	M5	R5
C7	F9	J8	M7	R14
C9	F11	J11	M8	R16
C11	F12	J12	M11	T2
D2	F14	J14	M12	T3
D3	F16	J16	M14	T14
D5	F17	K2	M16	T16
D7	G3	K6	M17	T17
D9	G6	K7	N5	U3
D11	G7	K8	N6	U16
D13	G9	K9	N7	V2
				V17

Table 22 PES12N3A Ground Pins

Signals Listed Alphabetically

Signal Name	I/O Type	Location	Signal Category
CCLKDS	I	T9	System
CCLKUS	I	U9	
GPIO_00	I/O	U12	General Purpose Input/Output
GPIO_01	I/O	V13	
GPIO_02	I/O	U13	
GPIO_03	I/O	T12	
GPIO_04	I/O	R12	
GPIO_05	I/O	V14	
GPIO_06	I/O	U14	
GPIO_07	I/O	T13	
JTAG_TCK	I	T4	JTAG
JTAG_TDI	I	U4	
JTAG_TDO	O	T5	
JTAG_TMS	I	U5	
JTAG_TRST_N	I	V5	
MSMBADDR_1	I	T6	SMBus
MSMBADDR_2	I	U6	
MSMBADDR_3	I	V6	
MSMBADDR_4	I	U7	
MSMBCLK	I/O	T7	
MSMBDAT	I/O	R7	
MSMBSMODE	I	U15	System
NC		R9	PCI Express
NC		U11	
NC		V10	
PE0RN00	I	C15	
PE0RN01	I	B11	
PE0RN02	I	A9	
PE0RN03	I	B3	
PE0RP00	I	C14	
PE0RP01	I	A11	
PE0RP02	I	B9	
PE0RP03	I	A3	
PE0TN00	O	A16	

Table 23 PES12N3A Alphabetical Signal List (Part 1 of 3)

Signal Name	I/O Type	Location	Signal Category
PE0TN01	O	B13	PCI Express (cont.)
PE0TN02	O	B7	
PE0TN03	O	A5	
PE0TP00	O	B16	
PE0TP01	O	A13	
PE0TP02	O	A7	
PE0TP03	O	B5	
PE2RN00	I	C2	
PE2RN01	I	J2	
PE2RN02	I	L1	
PE2RN03	I	U2	
PE2RP00	I	C1	
PE2RP01	I	J1	
PE2RP02	I	L2	
PE2RP03	I	U1	
PE2TN00	O	E1	
PE2TN01	O	G2	
PE2TN02	O	N2	
PE2TN03	O	R1	
PE2TP00	O	E2	
PE2TP01	O	G1	
PE2TP02	O	N1	
PE2TP03	O	R2	
PE4RN00	I	U17	
PE4RN01	I	L18	
PE4RN02	I	J18	
PE4RN03	I	C17	
PE4RP00	I	U18	
PE4RP01	I	L17	
PE4RP02	I	J17	
PE4RP03	I	C18	
PE4TN00	O	R18	
PE4TN01	O	N17	
PE4TN02	O	G17	
PE4TN03	O	E18	
PE4TP00	O	R17	

Table 23 PES12N3A Alphabetical Signal List (Part 2 of 3)