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Device Overview

The 89HPES24T6G2 is a member of IDT's PRECISE™ family of PCI Express® switching solutions. The PES24T6G2 is a 24-lane, 6-port Gen2 peripheral chip that performs PCI Express base switching with a feature set optimized for high performance applications such as servers, storage, and communications systems. It provides connectivity and switching functions between a PCI Express upstream port and up to five downstream ports and supports switching between downstream ports.

Features

- ◆ **High Performance PCI Express Switch**
 - Twenty-four 5 Gbps Gen2 PCI Express lanes supporting 5 Gbps and 2.5 Gbps operation
 - Up to six switch ports
 - Support for Max Payload Size up to 2048 bytes
 - Supports one virtual channel and eight traffic classes
 - Fully compliant with PCI Express base specification Revision 2.0
- ◆ **Flexible Architecture with Numerous Configuration Options**
 - Automatic per port link width negotiation to x8, x4, x2, or x1
 - Automatic lane reversal on all ports
 - Automatic polarity inversion
 - Supports in-band hot-plug presence detect capability
 - Supports external signal for hot plug event notification allowing SCI/SMI generation for legacy operating systems

- Dynamic link width reconfiguration for power/performance optimization
- Configurable downstream port PCI-to-PCI bridge device numbering
- Crosslink support
- Supports ARI forwarding defined in the Alternative Routing-ID Interpretation (ARI) ECN for virtualized and non-virtualized environments
- Ability to load device configuration from serial EEPROM

◆ Legacy Support

- PCI compatible INTx emulation
- Supports bus locked transactions, allowing use of PCI Express with legacy software

◆ Highly Integrated Solution

- Requires no external components
- Incorporates on-chip internal memory for packet buffering and queueing
- Integrates twenty-four 5 Gbps / 2.5 Gbps embedded SerDes, 8B/10B encoder/decoder (no separate transceivers needed)

◆ Reliability, Availability, and Serviceability (RAS) Features

- Ability to disable peer-to-peer communications
- Supports ECRC and Advanced Error Reporting
- All internal data and control RAMs are SECDED ECC protected
- Supports PCI Express hot-plug on all downstream ports
- Supports upstream port hot-plug

Block Diagram

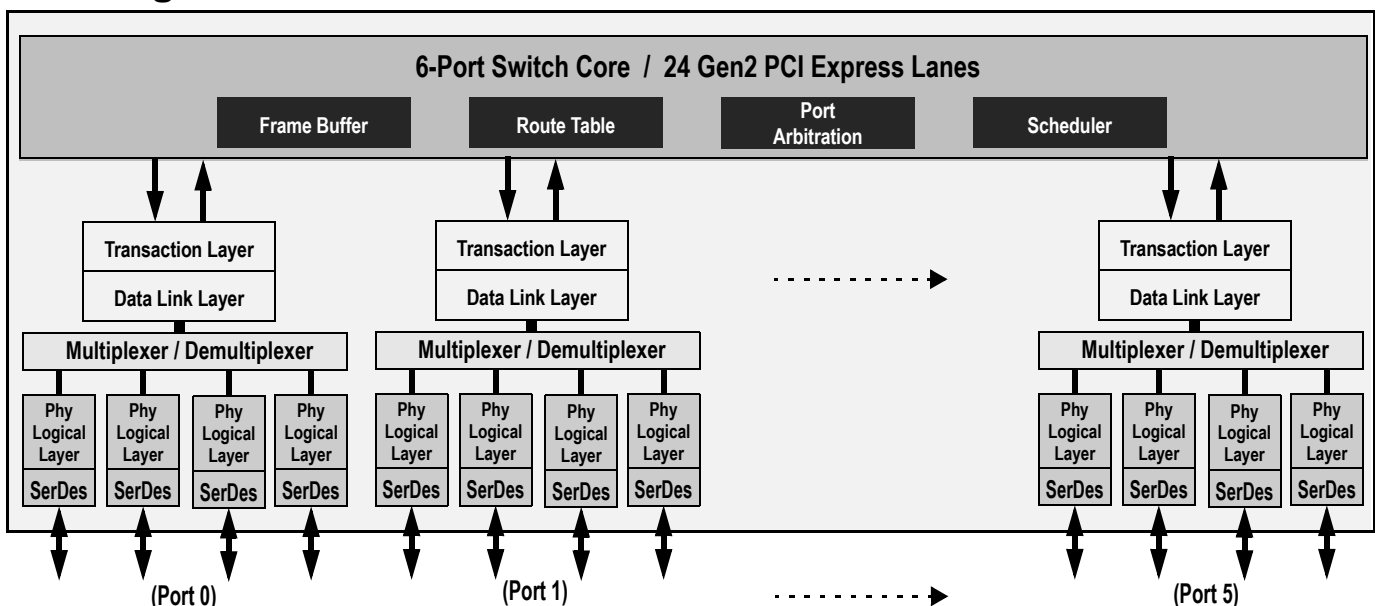


Figure 1 Internal Block Diagram

- Hot-swap capable I/O
- External Serial EEPROM contents are checksum protected
- Supports PCI Express Device Serial Number Capability
- Capability to monitor link reliability and autonomously change link speed to prevent link instability

◆ **Power Management**

- Utilizes advanced low-power design techniques to achieve low typical power consumption
- Support PCI Power Management Interface specification (PCI-PM 1.1)
 - Supports device power management states: D0, D3_{hot} and D3_{cold}
- Support for PCI Express Active State Power Management (ASPM) link state
 - Supports link power management states: L0, L0s, L1, L2/L3 Ready and L3
- Supports PCI Express Power Budgeting Capability
- Configurable SerDes power consumption
 - Supports optional PCI-Express SerDes Transmit Low-Swing Voltage Mode
 - Supports numerous SerDes Transmit Voltage Margin settings
- Unused SerDes are disabled

◆ **Testability and Debug Features**

- Per port link up and activity status outputs available on I/O expander outputs
- Built in SerDes 8-bit and 10-bit pseudo-random bit stream (PRBS) generators
- Numerous SerDes test modes, including a PRBS Master Loopback mode for in-system link testing
- Ability to read and write any internal register via SMBus and JTAG interfaces, including SerDes internal controls
- Per port statistics and performance counters, as well as proprietary link status registers

◆ **Eleven General Purpose Input/Output Pins**

- Each pin may be individually configured as an input or output
- Each pin may be individually configured as an interrupt input
- Some pins have selectable alternate functions

◆ **Option A Package: 19mm x 19mm 324-ball Flip Chip BGA with 1mm ball spacing**

◆ **Option B Package: 27mm x 27mm 676-ball Flip Chip BGA with 1mm ball spacing**

Product Description

Utilizing standard PCI Express interconnect, the PES24T6G2 provides the most efficient I/O connectivity solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides connectivity for up to 6 ports across 24 integrated serial lanes. Each lane provides 5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base Specification, Revision 2.0, including operation in 5 Gbps, 2.5 Gbps, and mixed 5 Gbps / 2.5Gbps modes.

The PES24T6G2 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification

Revision 2.0. The PES24T6G2 can operate either as a store and forward or cut-through switch and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to enable efficient switching and I/O connectivity for servers, storage, and embedded processors with limited connectivity.

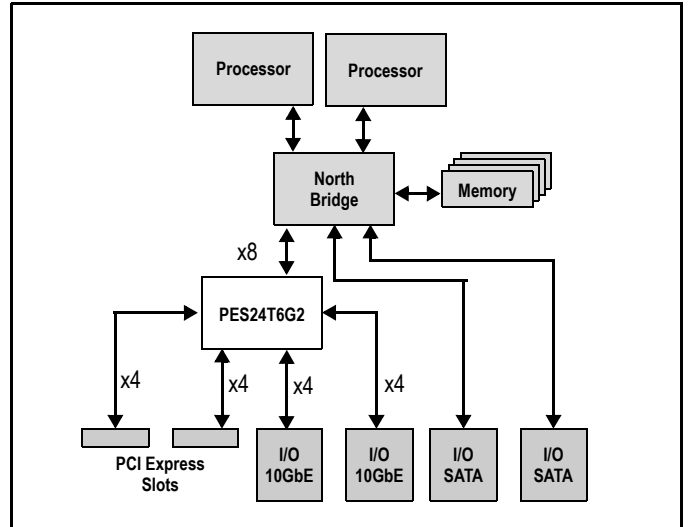


Figure 2 I/O Expansion Application

SMBus Interface

The PES24T6G2 contains two SMBus interfaces. The slave interface provides full access to the configuration registers in the PES24T6G2, allowing every configuration register in the device to be read or written by an external agent. The master interface allows the default configuration register values of the PES24T6G2 to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander.

Six pins make up each of the two SMBus interfaces. These pins consist of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins. In the slave interface, these address pins allow the SMBus address to which the device responds to be configured. In the master interface, these address pins allow the SMBus address of the serial configuration EEPROM from which data is loaded to be configured. The SMBus address is set up on negation of PERSTN by sampling the corresponding address pins. When the pins are sampled, the resulting address is assigned as shown in Table 1.

Note: MSMBADDR and SSMBADDR address pins are not available in the 19mm package. The MSMBADDR address is hardwired to 0x50, and the SSMBADDR address is hardwired to 0x77.

Bit	Slave SMBus Address	Master SMBus Address
1	SSMBADDR[1]	MSMBADDR[1]
2	SSMBADDR[2]	MSMBADDR[2]
3	SSMBADDR[3]	MSMBADDR[3]
4	0	MSMBADDR[4]
5	SSMBADDR[5]	1
6	1	0
7	1	1

Table 1 Master and Slave SMBus Address Assignment for 27x27mm Package

As shown in Figure 3, the master and slave SMBuses may be used in a unified or split configuration. In the unified configuration, shown in Figure 3(a), the master and slave SMBuses are tied together and the PES24T6G2 acts both as a SMBus master as well as a SMBus slave on this bus. This requires that the SMBus master or processor that has access to PES24T6G2 registers supports SMBus arbitration. In some systems, this SMBus master interface may be implemented using general purpose I/O pins on a processor or micro controller, and may not support SMBus arbitration. To support these systems, the PES24T6G2 may be configured to operate in a split configuration as shown in Figure 3(b).

In the split configuration, the master and slave SMBuses operate as two independent buses and thus multi-master arbitration is never required. The PES24T6G2 supports reading and writing of the serial EEPROM on the master SMBus via the slave SMBus, allowing in system programming of the serial EEPROM.

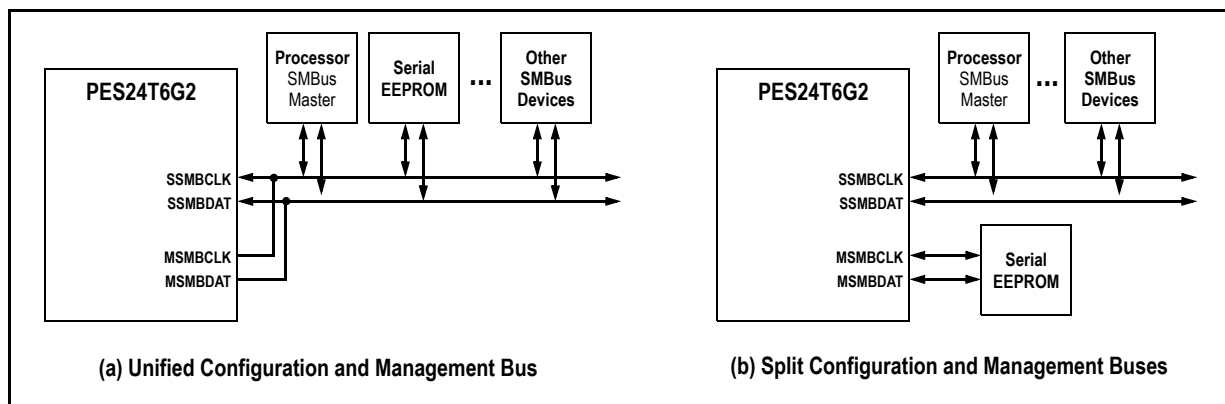


Figure 3 SMBus Interface Configuration Examples

Hot-Plug Interface

The PES24T6G2 supports PCI Express Hot-Plug on each downstream port. To reduce the number of pins required on the device, the PES24T6G2 utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES24T6G2 generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES24T6G2. In response to an I/O expander interrupt, the PES24T6G2 generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

General Purpose Input/Output

The PES24T6G2 provides General Purpose Input/Output (GPIO) pins (7 pins in the 19mm package and 11 pins in the 27mm package) that may be used by the system designer as bit I/O ports. Each GPIO pin may be configured independently as an input or output through software control. Many GPIO pins are shared with other on-chip functions. These alternate functions may be enabled via software, SMBus slave interface, or serial configuration EEPROM.

Pin Description

The following tables list the functions of the pins provided on the PES24T6G2. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an “N” are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Signal	Type	Name/Description
PE0RP[3:0] PE0RN[3:0]	I	PCI Express Port 0 Serial Data Receive. Differential PCI Express receive pairs for port 0. Port 0 is the upstream port.
PE0TP[3:0] PE0TN[3:0]	O	PCI Express Port 0 Serial Data Transmit. Differential PCI Express transmit pairs for port 0. Port 0 is the upstream port.
PE1RP[3:0] PE1RN[3:0]	I	PCI Express Port 1 Serial Data Receive. Differential PCI Express receive pairs for port 1.
PE1TP[3:0] PE1TN[3:0]	O	PCI Express Port 1 Serial Data Transmit. Differential PCI Express transmit pairs for port 1.
PE2RP[3:0] PE2RN[3:0]	I	PCI Express Port 2 Serial Data Receive. Differential PCI Express receive pairs for port 2.
PE2TP[3:0] PE2TN[3:0]	O	PCI Express Port 2 Serial Data Transmit. Differential PCI Express transmit pairs for port 2.
PE3RP[3:0] PE3RN[3:0]	I	PCI Express Port 3 Serial Data Receive. Differential PCI Express receive pairs for port 3.
PE3TP[3:0] PE3TN[3:0]	O	PCI Express Port 3 Serial Data Transmit. Differential PCI Express transmit pairs for port 3.
PE4RP[3:0] PE4RN[3:0]	I	PCI Express Port 4 Serial Data Receive. Differential PCI Express receive pairs for port 4.
PE4TP[3:0] PE4TN[3:0]	O	PCI Express Port 4 Serial Data Transmit. Differential PCI Express transmit pairs for port 4.
PE5RP[3:0] PE5RN[3:0]	I	PCI Express Port 5 Serial Data Receive. Differential PCI Express receive pairs for port 5.
PE5TP[3:0] PE5TN[3:0]	O	PCI Express Port 5 Serial Data Transmit. Differential PCI Express transmit pairs for port 5.
PEREFCLKP PEREFCLKN	I	PCI Express Reference Clock. Differential reference clock pair input. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic and on-chip SerDes. The frequency of the differential reference clock is determined by the REFCLKM signal.
REFCLKM ¹	I	PCI Express Reference Clock Mode Select. This signal selects the frequency of the reference clock input. 0x0 - 100 MHz 0x1 - 125 MHz This pin should be static and not change following the negation of PERSTN.

Table 2 PCI Express Interface Pins

¹ REFCLKM is not available in the 19mm package and frequency is set at 100MHz.

Signal	Type	Name/Description
MSMBADDR[4:1] ¹	I	Master SMBus Address. These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded.
MSMBCLK	I/O	Master SMBus Clock. This bidirectional signal is used to synchronize transfers on the master SMBus.

Table 3 SMBus Interface Pins (Part 1 of 2)

Signal	Type	Name/Description
MSMBDAT	I/O	Master SMBus Data. This bidirectional signal is used for data on the master SMBus.
SSMBADDR[5,3:1] ²	I	Slave SMBus Address. These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	Slave SMBus Clock. This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	Slave SMBus Data. This bidirectional signal is used for data on the slave SMBus.

Table 3 SMBus Interface Pins (Part 2 of 2)

¹. MSMBADDR pins are not available in the 19mm package. Address hardwired to 0x50.

². SSMBADDR pins are not available in the 19mm package. Address hardwired to 0x77.

Signal	Type	Name/Description
GPIO[0]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P2RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 2
GPIO[1]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P4RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 4
GPIO[2]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN0 Alternate function pin type: Input Alternate function: I/O Expander interrupt 0 input
GPIO[3] ¹	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN1 Alternate function pin type: Input Alternate function: I/O Expander interrupt 1 input
GPIO[4] ¹	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN2 Alternate function pin type: Input Alternate function: I/O Expander interrupt 2 input
GPIO[5] ¹	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN3 Alternate function pin type: Input Alternate function: I/O Expander interrupt 3 input
GPIO[6] ¹	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[7]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: GPEN Alternate function pin type: Output Alternate function: General Purpose Event (GPE) output

Table 4 General Purpose I/O Pins (Part 1 of 2)

Signal	Type	Name/Description
GPIO[8]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P1RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 1
GPIO[9]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P3RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 3
GPIO[10]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P5RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 5

Table 4 General Purpose I/O Pins (Part 2 of 2)

¹. GPIO pins 3, 4, 5, 6 are not available in the 19mm package.

Signal	Type	Name/Description
CCLKDS	I	Common Clock Downstream. The assertion of this pin indicates that all downstream ports are using the same clock source as that provided to downstream devices. This bit is used as the initial value of the Slot Clock Configuration bit in all of the Link Status Registers for downstream ports. The value may be overridden by modifying the SCLK bit in each downstream port's PCIELSTS register.
CCLKUS	I	Common Clock Upstream. The assertion of this pin indicates that the upstream port is using the same clock source as the upstream device. This bit is used as the initial value of the Slot Clock Configuration bit in the Link Status Register for the upstream port. The value may be overridden by modifying the SCLK bit in the P0_PCIELSTS register.
MSMBSMODE ¹	I	Master SMBus Slow Mode. The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 KHz. This value may not be overridden.
P01MERGEN	I	Port 0 and 1 Merge. P01MERGEN is an active low signal. It is pulled high internally via a 92K ohm resistor. When this pin is low, port 0 is merged with port 1 to form a single x8 port. The Serdes lanes associated with port 1 become lanes 4 through 7 of port 0. When this pin is high, port 0 and port 1 are not merged, and each operates as a single x4 port.
P23MERGEN	I	Port 2 and 3 Merge. P23MERGEN is an active low signal. It is pulled high internally via a 92K ohm resistor. When this pin is low, port 2 is merged with port 3 to form a single x8 port. The Serdes lanes associated with port 3 become lanes 4 through 7 of port 2. When this pin is high, port 2 and port 3 are not merged, and each operates as a single x4 port.
P45MERGEN	I	Port 4 and 5 Merge. P45MERGEN is an active low signal. It is pulled high internally via a 92K ohm resistor. When this pin is low, port 4 is merged with port 5 to form a single x8 port. The Serdes lanes associated with port 5 become lanes 4 through 7 of port 4. When this pin is high, port 4 and port 5 are not merged, and each operates as a single x4 port.
PERSTN	I	Fundamental Reset. Assertion of this signal resets all logic inside PES24T6G2 and initiates a PCI Express fundamental reset.

Table 5 System Pins (Part 1 of 2)

Signal	Type	Name/Description
RSTHALT ²	I	Reset Halt. When this signal is asserted during a PCI Express fundamental reset, PES24T6G2 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the SWCTL register by an SMBus master.
SWMODE[2:0]	I	Switch Mode. These configuration pins determine the PES24T6G2 switch operating mode. 0x0 -Normal switch mode 0x1 -Normal switch mode with Serial EEPROM initialization 0x2 - through 0x7 Reserved These pins should be static and not change following the negation of PERSTN.

Table 5 System Pins (Part 2 of 2)

¹. MSMBSMODE is not available in the 19mm package, resulting in the master SMBus operating only at 400 KHz.

². RSTHALT is not available in the 19mm package.

Signal	Type	Name/Description
JTAG_TCK	I	JTAG Clock. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	JTAG Data Input. This is the serial data input to the boundary scan logic or JTAG Controller.
JTAG_TDO	O	JTAG Data Output. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	JTAG Mode. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	JTAG Reset. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 6 Test Pins

Signal	Type	Name/Description
REFRES0	I/O	Port 0 External Reference Resistor. Provides a reference for the Port 0 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES1	I/O	Port 1 External Reference Resistor. Provides a reference for the Port 1 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES2	I/O	Port 2 External Reference Resistor. Provides a reference for the Port 2 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES3	I/O	Port 3 External Reference Resistor. Provides a reference for the Port 3 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES4	I/O	Port 4 External Reference Resistor. Provides a reference for the Port 4 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES5	I/O	Port 5 External Reference Resistor. Provides a reference for the Port 5 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
V _{DD} CORE	I	Core V_{DD}. Power supply for core logic.
V _{DD} I/O	I	I/O V_{DD}. LVTTTL I/O buffer power supply.
V _{DD} PEA	I	PCI Express Analog Power. Serdes analog power supply (1.0V).
V _{DD} PEHA	I	PCI Express Analog High Power. Serdes analog power supply (2.5V).
V _{DD} PETA	I	PCI Express Transmitter Analog Voltage. Serdes transmitter analog power supply (1.0V).
V _{SS}	I	Ground.

Table 7 Power, Ground, and SerDes Resistor Pins

Pin Characteristics

Note: Some input pads of the PES24T6G2 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor ¹	Notes
PCI Express Interface	PE0RN[3:0]	I	PCIe differential ²	Serial Link		
	PE0RP[3:0]	I				
	PE0TN[3:0]	O				
	PE0TP[3:0]	O				
	PE1RN[3:0]	I				
	PE1RP[3:0]	I				
	PE1TN[3:0]	O				
	PE1TP[3:0]	O				
	PE2RN[3:0]	I				
	PE2RP[3:0]	I				
	PE2TN[3:0]	O				
	PE2TP[3:0]	O				
	PE3RN[3:0]	I				
	PE3RP[3:0]	I				
	PE3TN[3:0]	O				
	PE3TP[3:0]	O				
	PE4RN[3:0]	I				
	PE4RP[3:0]	I				
	PE4TN[3:0]	O				
	PE4TP[3:0]	O				
	PE5RN[3:0]	I				
	PE5RP[3:0]	I				
	PE5TN[3:0]	O				
PE5TP[3:0]	O					
	PEREFCLKN	I	HCSL	Diff. Clock Input		Refer to Table 9
	PEREFCLKP	I				
	REFCLKM ³	I	LVTTTL	Input	pull-down	
SMBus	MSMBADDR[4:1] ⁴	I	LVTTTL	Input	pull-down	
	MSMBCLK	I/O		STI ⁵		pull-up on board
	MSMBDAT	I/O		STI		pull-up on board
	SSMBADDR[5,3:1] ⁴	I		Input	pull-up	
	SSMBCLK	I/O		STI		pull-up on board
	SSMBDAT	I/O		STI		pull-up on board
General Purpose I/O	GPIO[10:0] ⁶	I/O	LVTTTL	STI, High Drive	pull-up	

Table 8 Pin Characteristics (Part 1 of 2)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor ¹	Notes
System Pins	CCLKDS	I	LVTTL	Input	pull-up	
	CCLKUS	I		Input	pull-up	
	MSMBSMODE ⁷	I		Input	pull-down	
	P01MERGEN	I			pull-up	
	P23MERGEN	I			pull-up	
	P45MERGEN	I			pull-up	
	PERSTN	I		STI		
	RSTHALT ⁷	I		Input	pull-down	
	SWMODE[2:0]	I		Input	pull-down	
EJTAG / JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I		STI	pull-up	
	JTAG_TDO	O				
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I		STI	pull-up	
SerDes Reference Resistors	REFRES0	I/O	Analog			
	REFRES1	I/O				
	REFRES2	I/O				
	REFRES3	I/O				
	REFRES4	I/O				
	REFRES5	I/O				

Table 8 Pin Characteristics (Part 2 of 2)

- ¹. Internal resistor values under typical operating conditions are 92K Ω for pull-up and 90K Ω for pull-down.
- ². All receiver pins set the DC common mode voltage to ground. All transmitters must be AC coupled to the media.
- ³. REFCLKM is not available in the 19mm package.
- ⁴. SMBus address pins are not available in the 19mm package.
- ⁵. Schmitt Trigger Input (STI).
- ⁶. GPIO pins 3, 4, 5, 6 are not available in the 19mm package.
- ⁷. MSMBSMODE and RSTHALT are not available in the 19mm package.

Logic Diagram — PES24T6G2

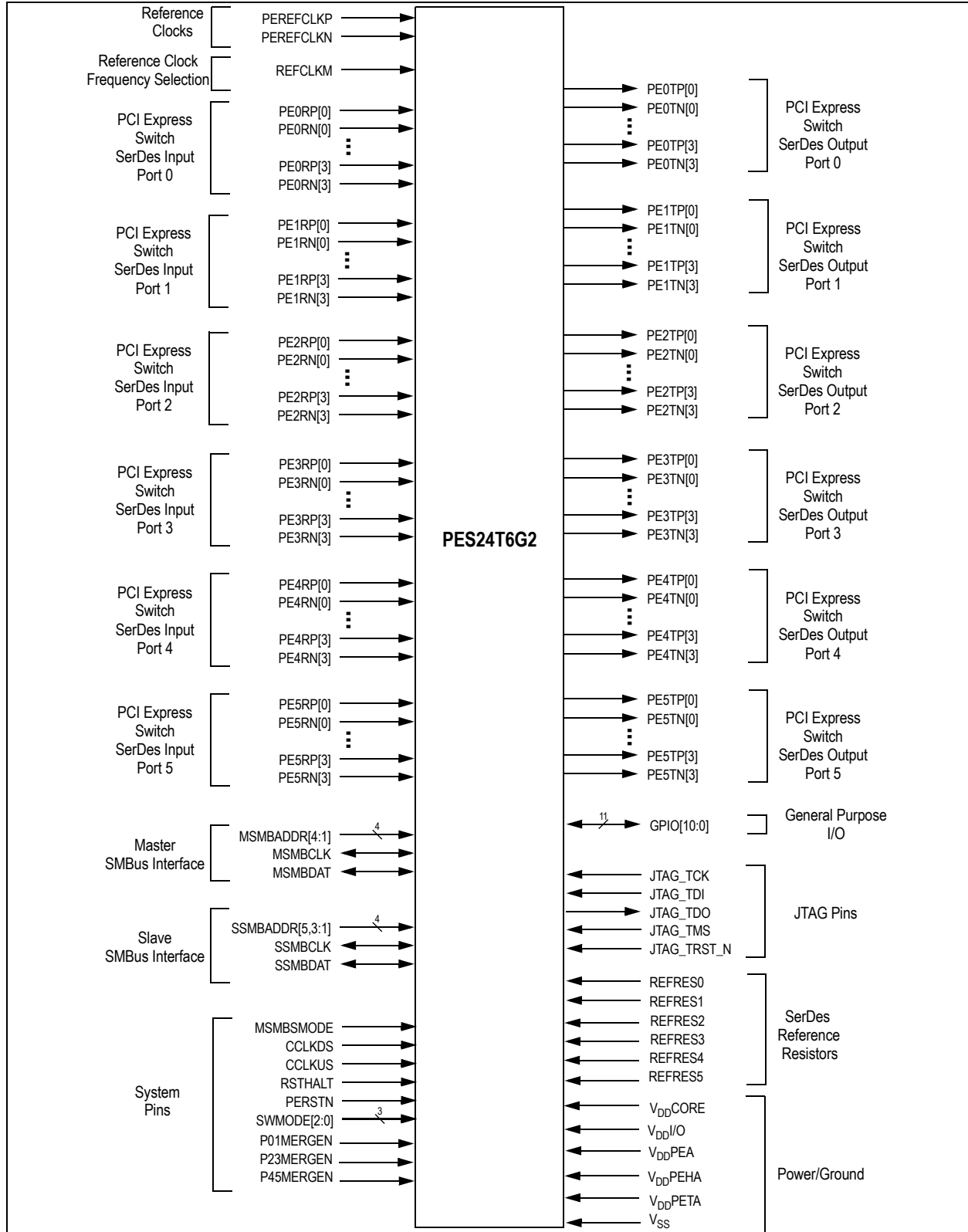


Figure 4 PES24T6G2 Logic Diagram

Note: The following pins are not available in the 19mm package: REFCLKM, MSMBADDR, SSBMADDR, MSMBSMODE, RSTHALT, GPIO[6:3].

System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 13 and 15.

Parameter	Description	Condition	Min	Typical	Max	Unit
Refclk _{FREQ}	Input reference clock frequency range		100		125 ¹	MHz
T _{C-RISE}	Rising edge rate	Differential	0.6		4	V/ns
T _{C-FALL}	Falling edge rate	Differential	0.6		4	V/ns
V _{IH}	Differential input high voltage	Differential	+150			mV
V _{IL}	Differential input low voltage	Differential			-150	mV
V _{CROSS}	Absolute single-ended crossing point voltage	Single-ended	+250		+550	mV
V _{CROSS-DELTA}	Variation of V _{CROSS} over all rising clock edges	Single-ended			+140	mV
V _{RB}	Ring back voltage margin	Differential	-100		+100	mV
T _{STABLE}	Time before V _{RB} is allowed	Differential	500			ps
T _{PERIOD-AVG}	Average clock period accuracy		-300		2800	ppm
T _{PERIOD-ABS}	Absolute period, including spread-spectrum and jitter		9.847		10.203	ns
T _{CC-JITTER}	Cycle to cycle jitter				150	ps
V _{MAX}	Absolute maximum input voltage				+1.15	V
V _{MIN}	Absolute minimum input voltage		-0.3			V
Duty Cycle	Duty cycle		40		60	%
Rise/Fall Matching	Single ended rising Refclk edge rate versus falling Refclk edge rate			20		%
Z _{C-DC}	Clock source output DC impedance		40		60	Ω

Table 9 Input Clock Requirements

¹ The input clock frequency will be either 100 or 125 MHz depending on signal REFCLKM. Frequency is set at 100 MHz in the 19mm package.

AC Timing Characteristics

Parameter	Description	Gen 1			Gen 2			Units
		Min ¹	Typ ¹	Max ¹	Min ¹	Typ ¹	Max ¹	
PCIe Transmit								
UI	Unit Interval	399.88	400	400.12	199.94	200	200.06	ps
T _{TX-EYE}	Minimum Tx Eye Width	0.75			0.75			UI
T _{TX-EYE-MEDIAN-to-MAX-JITTER}	Maximum time between the jitter median and maximum deviation from the median			0.125				UI
T _{TX-RISE} , T _{TX-FALL}	TX Rise/Fall Time: 20% - 80%	0.125			0.15			UI
T _{TX-IDLE-MIN}	Minimum time in idle	20			20			UI
T _{TX-IDLE-SET-TO-IDLE}	Maximum time to transition to a valid Idle after sending an Idle ordered set			8			8	ns

Table 10 PCIe AC Timing Characteristics (Part 1 of 2)

Parameter	Description	Gen 1			Gen 2			Units
		Min ¹	Typ ¹	Max ¹	Min ¹	Typ ¹	Max ¹	
T _{TX-IDLE-TO-DIFF-DATA}	Maximum time to transition from valid idle to diff data			8			8	ns
T _{TX-SKEW}	Transmitter data skew between any 2 lanes			1.3			1.3	ns
T _{MIN-PULSED}	Minimum Instantaneous Lone Pulse Width	NA			0.9			UI
T _{TX-HF-DJ-DD}	Transmitter Deterministic Jitter > 1.5MHz Bandwidth	NA					0.15	UI
T _{RF-MISMATCH}	Rise/Fall Time Differential Mismatch	NA					0.1	UI
PCIe Receive								
UI	Unit Interval	399.88	400	400.12	199.94		200.06	ps
T _{RX-EYE (with jitter)}	Minimum Receiver Eye Width (jitter tolerance)	0.4			0.4			UI
T _{RX-EYE-MEDIUM TO MAX JITTER}	Max time between jitter median & max deviation			0.3				UI
T _{RX-SKEW}	Lane to lane input skew			20			8	ns
T _{RX-HF-RMS}	1.5 — 100 MHz RMS jitter (common clock)	NA					3.4	ps
T _{RX-HF-DJ-DD}	Maximum tolerable DJ by the receiver (common clock)	NA					88	ps
T _{RX-LF-RMS}	10 KHz to 1.5 MHz RMS jitter (common clock)	NA					4.2	ps
T _{RX-MIN-PULSE}	Minimum receiver instantaneous eye width	NA			0.6			UI

Table 10 PCIe AC Timing Characteristics (Part 2 of 2)

¹. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 2.0

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[10:0] ¹	T _{pw} ²	None	50	—	ns	

Table 11 GPIO AC Timing Characteristics

¹. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous. Note that GPIO(6:3) pins are not available in the 19mm package.

². The values for this symbol were determined by calculation, not by testing.

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	50.0	—	ns	See Figure 5.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS ¹ , JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	20	ns	
	Tdz_16c ²		—	20	ns	
JTAG_TRST_N	Tpw_16d ²	none	25.0	—	ns	

Table 12 JTAG AC Timing Characteristics

¹ The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

² The values for this symbol were determined by calculation, not by testing.

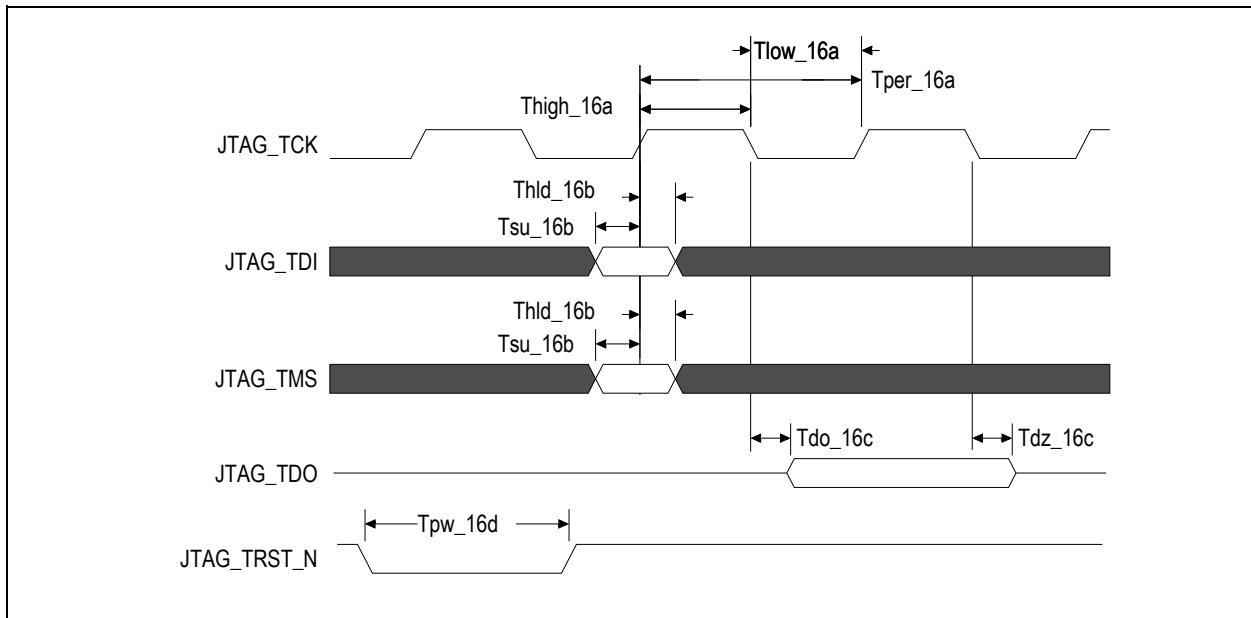


Figure 5 JTAG AC Timing Waveform

Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V _{DD} CORE	Internal logic supply	0.9	1.0	1.1	V
V _{DD} I/O	I/O supply except for SerDes LVPECL/CML	3.135	3.3	3.465	V
V _{DD} PEA ¹	PCI Express Analog Power	0.95	1.0	1.1	V
V _{DD} PEHA ²	PCI Express Analog High Power	2.25	2.5	2.75	V
V _{DD} PETA ¹	PCI Express Transmitter Analog Voltage	0.95	1.0	1.1	V
V _{SS}	Common ground	0	0	0	V

Table 13 PES24T6G2 Operating Voltages

¹ V_{DD}PEA and V_{DD}PETA should have no more than 25mV_{peak-peak} AC power supply noise superimposed on the 1.0V nominal DC value.

² V_{DD}PEHA should have no more than 50mV_{peak-peak} AC power supply noise superimposed on the 2.5V nominal DC value.

Absolute Maximum Voltage Rating

Core Supply	PCIe Analog Supply	PCIe Analog High Supply	PCIe Transmitter Supply	I/O Supply
1.5V	1.5V	4.6V	1.5V	4.6V

Table 14 PES24T6G2 Absolute Maximum Voltage Rating

Warning: For proper and reliable operation in adherence with this data sheet, the device should not exceed the recommended operating voltages in Table 13. The absolute maximum operating voltages in Table 14 are offered to provide guidelines for voltage excursions outside the recommended voltage ranges. Device functionality is not guaranteed at these conditions and sustained operation at these values or any exposure to voltages outside the maximum range may adversely affect device functionality and reliability.

Power-Up/Power-Down Sequence

During power supply ramp-up, V_{DD}CORE must remain at least 1.0V below V_{DD}I/O at all times. There are no other power-up sequence requirements for the various operating supply voltages.

The power-down sequence can occur in any order.

Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 15 PES24T6G2 Operating Temperatures

Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 13 (and also listed below).

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 13 (and also listed below).

Number of active Lanes per Port		Core Supply		PCIe Analog Supply		PCIe Analog High Supply		PCIe Termination Supply		I/O Supply		Total	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 2.5V	Max 2.75V	Typ 1.0V	Max 1.15V	Typ 3.3V	Max 3.465V	Typ Power	Max Power
8/4/4/4/4 (Full Swing)	mA	1010	1260	1384	1600	161	176	541	600	3	5		
	Watts	1.01	1.39	1.38	1.76	0.40	0.48	0.54	0.66	0.010	0.017	3.35	4.31
8/4/4/4/4 (Half swing)	mA	1010	1260	1190	1376	161	176	281	312	3	5		
	Watts	1.01	1.39	1.19	1.51	0.40	0.48	0.28	0.34	0.010	0.017	2.89	3.74

Table 16 PES24T6G2 Power Consumption

Thermal Considerations — Option A Package

This section describes thermal considerations for the PES24T6G2 (19mm² FCBGA324 package). The data in Table 17 below contains information that is relevant to the thermal performance of the PES24T6G2 switch.

Symbol	Parameter	Value	Units	Conditions
T _{J(max)}	Junction Temperature	125	°C	Maximum
T _{A(max)}	Ambient Temperature	70	°C	Maximum
θ _{JA(effective)}	Effective Thermal Resistance, Junction-to-Ambient	16.8	°C/W	Zero air flow
		10.1	°C/W	1 m/S air flow
		9.2	°C/W	2 m/S air flow
θ _{JB}	Thermal Resistance, Junction-to-Board	4.1	°C/W	
θ _{JC}	Thermal Resistance, Junction-to-Case	0.3	°C/W	
P	Power Dissipation of the Device	4.31	Watts	Maximum

Table 17 Thermal Specifications for PES24T6G2, 19x19 mm FCBGA324 Package

Thermal Considerations — Option B Package

This section describes thermal considerations for the PES24T6G2 (27mm² FCBGA676 package). The data in Table 18 below contains information that is relevant to the thermal performance of the PES24T6G2 switch.

Symbol	Parameter	Value	Units	Conditions
T _{J(max)}	Junction Temperature	125	°C	Maximum
T _{A(max)}	Ambient Temperature	70	°C	Maximum

Table 18 Thermal Specifications for PES24T6G2, 27x27 mm FCBGA676 Package

Symbol	Parameter	Value	Units	Conditions
$\theta_{JA(\text{effective})}$	Effective Thermal Resistance, Junction-to-Ambient	14.6	$^{\circ}\text{C}/\text{W}$	Zero air flow
		8.2	$^{\circ}\text{C}/\text{W}$	1 m/S air flow
		7.2	$^{\circ}\text{C}/\text{W}$	2 m/S air flow
θ_{JB}	Thermal Resistance, Junction-to-Board	3.1	$^{\circ}\text{C}/\text{W}$	
θ_{JC}	Thermal Resistance, Junction-to-Case	0.3	$^{\circ}\text{C}/\text{W}$	
P	Power Dissipation of the Device	4.31	Watts	Maximum

Table 18 Thermal Specifications for PES24T6G2, 27x27 mm FCBGA676 Package

Note: It is important for the reliability of this device in any user environment that the junction temperature not exceed the $T_{J(\text{max})}$ value specified in Table 17. Consequently, the effective junction to ambient thermal resistance (θ_{JA}) for the worst case scenario must be maintained below the value determined by the formula:

$$\theta_{JA} = (T_{J(\text{max})} - T_{A(\text{max})})/P$$

Given that the values of $T_{J(\text{max})}$, $T_{A(\text{max})}$, and P are known, the value of desired θ_{JA} becomes a known entity to the system designer. How to achieve the desired θ_{JA} is left up to the board or system designer, but in general, it can be achieved by adding the effects of θ_{JC} (value provided in Table 17), thermal resistance of the chosen adhesive (θ_{CS}), that of the heat sink (θ_{SA}), amount of airflow, and properties of the circuit board (number of layers and size of the board). As a general guideline, this device will not need a heat sink if the board has 8 or more layers AND the board size is larger than 4"x12" AND airflow in excess of 0.5 m/s is available. It is strongly recommended that users perform their own thermal analysis for their own board and system design scenarios.

DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 13.

Note: See Table 8, Pin Characteristics, for a complete I/O listing.

I/O Type	Parameter	Description	Gen1			Gen2			Unit	Condi- tions	
			Min ¹	Typ ¹	Max ¹	Min ¹	Typ ¹	Max ¹			
Serial Link	PCIe Transmit										
	V _{TX-DIFFp-p}	Differential peak-to-peak output voltage	800		1200	800		1200	mV		
	V _{TX-DIFFp-p-LOW}	Low-Drive Differential Peak to Peak Output Voltage	400		1200	400		1200	mV		
	V _{TX-DE-RATIO-3.5dB}	De-emphasized differential output voltage	-3		-4	-3.0	-3.5	-4.0	dB		
	V _{TX-DE-RATIO-6.0dB}	De-emphasized differential output voltage	NA			-5.5	-6.0	-6.5	dB		
	V _{TX-DC-CM}	DC Common mode voltage	0		3.6	0		3.6	V		
	V _{TX-CM-ACP}	RMS AC peak common mode output voltage			20				mV		
	V _{TX-CM-DC-active-idle-delta}	Abs delta of DC common mode voltage between L0 and idle			100			100	mV		
	V _{TX-CM-DC-line-delta}	Abs delta of DC common mode voltage between D+ and D-			25			25	mV		
	V _{TX-Idle-DiffP}	Electrical idle diff peak output			20			20	mV		
	RL _{TX-DIFF}	Transmitter Differential Return loss	10						10	dB	0.05 - 1.25GHz
									8	dB	1.25 - 2.5GHz
	RL _{TX-CM}	Transmitter Common Mode Return loss	6					6	dB		
	Z _{TX-DIFF-DC}	DC Differential TX impedance	80	100	120			120	Ω		
	V _{TX-CM-ACpp}	Peak-Peak AC Common	NA					100	mV		
	V _{TX-DC-CM}	Transmit Driver DC Common Mode Voltage	0		3.6	0		3.6	V		
V _{TX-RCV-DETECT}	The amount of voltage change allowed during Receiver Detection			600			600	mV			
I _{TX-SHORT}	Transmitter Short Circuit Current Limit	0		90				90	mA		

Table 19 DC Electrical Characteristics (Part 1 of 2)

I/O Type	Parameter	Description	Gen1			Gen2			Unit	Condi- tions
			Min ¹	Typ ¹	Max ¹	Min ¹	Typ ¹	Max ¹		
Serial Link (cont.)	PCIe Receive									
	$V_{RX-DIFFp-p}$	Differential input voltage (peak-to-peak)	175		1200	120		1200	mV	
	$RL_{RX-DIFF}$	Receiver Differential Return Loss	10					10	dB	0.05 - 1.25GHz
								8		1.25 - 2.5GHz
	RL_{RX-CM}	Receiver Common Mode Return Loss	6					6	dB	
	$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	Refer to return loss spec			Ω	
	Z_{RX-DC}	DC common mode impedance	40	50	60	40		60	Ω	
	$Z_{RX-COMM-DC}$	Powered down input common mode impedance (DC)	200k	350k				50k	Ω	
	$Z_{RX-HIGH-IMP-DC-POS}$	DC input CM input impedance for $V > 0$ during reset or power down			50k			50k	Ω	
	$Z_{RX-HIGH-IMP-DC-NEG}$	DC input CM input impedance for $V < 0$ during reset or power down			1.0k			1.0k	Ω	
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	65		175	mV		
$V_{RX-CM-ACp}$	Receiver AC common-mode peak voltage			150			150	mV	$V_{RX-CM-ACp}$	
PCIe REFCLK										
	C_{IN}	Input Capacitance	1.5	—		1.5	—		pF	
Other I/Os										
LOW Drive Output	I_{OL}		—	2.5	—	—	2.5	—	mA	$V_{OL} = 0.4v$
	I_{OH}		—	-5.5	—	—	-5.5	—	mA	$V_{OH} = 1.5V$
High Drive Output	I_{OL}		—	12.0	—	—	12.0	—	mA	$V_{OL} = 0.4v$
	I_{OH}		—	-20.0	—	—	-20.0	—	mA	$V_{OH} = 1.5V$
Schmitt Trig- ger Input (STI)	V_{IL}		-0.3	—	0.8	-0.3	—	0.8	V	—
	V_{IH}		2.0	—	$V_{DD}/O + 0.5$	2.0	—	$V_{DD}/O + 0.5$	V	—
Input	V_{IL}		-0.3	—	0.8	-0.3	—	0.8	V	—
	V_{IH}		2.0	—	$V_{DD}/O + 0.5$	2.0	—	$V_{DD}/O + 0.5$	V	—
Capacitance	C_{IN}		—	—	8.5	—	—	8.5	pF	—
Leakage	Inputs		—	—	± 10	—	—	± 10	μA	V_{DD}/O (max)
	I/O_{LEAK} W/O Pull-ups/downs		—	—	± 10	—	—	± 10	μA	V_{DD}/O (max)
	I/O_{LEAK} WITH Pull-ups/downs		—	—	± 80	—	—	± 80	μA	V_{DD}/O (max)

Table 19 DC Electrical Characteristics (Part 2 of 2)

¹ Minimum, Typical, and Maximum values meet the requirements under PCI Specification 2.0.

PES24T6G2 Package Options

Package Option	Package Size
A	19x19 mm
B	27x27 mm

Table 20 PES24T6G2 Package Options

Option A Package Pinout, 19x19mm 324-BGA Signal Pinout

The following table lists the pin numbers and signal names for the PES24T6G2 device.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	V _{SS}		B17	PE4TN00		D15	V _{DD} CORE		F13	V _{SS}	
A2	V _{DD} I/O		B18	PE4TP00		D16	V _{SS}		F14	PE4RN03	
A3	P01MERGEN		C1	PE3TP02		D17	V _{SS}		F15	PE4RP03	
A4	P23MERGEN		C2	PE3TN02		D18	V _{SS}		F16	V _{SS}	
A5	P45MERGEN		C3	V _{SS}		E1	PE3TP01		F17	PE4TN03	
A6	V _{DD} I/O		C4	PE3RP02		E2	PE3TN01		F18	PE4TP03	
A7	V _{SS}		C5	PE3RN02		E3	V _{SS}		G1	V _{SS}	
A8	JTAG_TDI		C6	V _{SS}		E4	PE3RP01		G2	V _{SS}	
A9	MSMBDAT		C7	JTAG_TCK		E5	PE3RN01		G3	V _{SS}	
A10	V _{DD} I/O		C8	JTAG_TRST_N		E6	V _{DD} CORE		G4	V _{DD} CORE	
A11	V _{SS}		C9	SSMBDAT		E7	V _{DD} CORE		G5	V _{DD} CORE	
A12	GPIO_00	1	C10	CCLKDS		E8	V _{DD} CORE		G6	V _{DD} PEA	
A13	V _{DD} I/O		C11	SWMODE_2		E9	V _{SS}		G7	V _{DD} PEA	
A14	V _{DD} I/O		C12	GPIO_02	1	E10	V _{DD} CORE		G8	V _{DD} CORE	
A15	V _{SS}		C13	GPIO_09	1	E11	V _{DD} CORE		G9	V _{DD} CORE	
A16	V _{SS}		C14	PE4RN01		E12	V _{DD} CORE		G10	V _{DD} CORE	
A17	V _{DD} I/O		C15	PE4RP01		E13	V _{DD} CORE		G11	V _{SS}	
A18	V _{DD} I/O		C16	V _{SS}		E14	PE4RN02		G12	V _{DD} PEA	
B1	PE3TP03		C17	PE4TN01		E15	PE4RP02		G13	V _{DD} PEA	
B2	PE3TN03		C18	PE4TP01		E16	V _{SS}		G14	V _{DD} CORE	
B3	V _{SS}		D1	V _{SS}		E17	PE4TN02		G15	V _{DD} CORE	
B4	PE3RP03		D2	V _{SS}		E18	PE4TP02		G16	V _{SS}	
B5	PE3RN03		D3	V _{SS}		F1	PE3TP00		G17	V _{SS}	
B6	V _{DD} I/O		D4	V _{DD} CORE		F2	PE3TN00		G18	V _{SS}	
B7	V _{DD} I/O		D5	V _{DD} CORE		F3	V _{SS}		H1	PE2TP03	
B8	JTAG_TMS		D6	V _{DD} I/O		F4	PE3RP00		H2	PE2TN03	
B9	SSMBCLK		D7	JTAG_TDO		F5	PE3RN00		H3	V _{SS}	
B10	V _{DD} I/O		D8	MSMBCLK		F6	V _{SS}		H4	PE2RP03	
B11	SWMODE_1		D9	CCLKUS		F7	V _{SS}		H5	PE2RN03	
B12	GPIO_01	1	D10	SWMODE_0		F8	V _{DD} CORE		H6	V _{DD} PEA	
B13	GPIO_10	1	D11	PERSTN		F9	V _{SS}		H7	V _{DD} PEA	
B14	PE4RN00		D12	GPIO_07	1	F10	V _{DD} CORE		H8	V _{DD} CORE	
B15	PE4RP00		D13	GPIO_08		F11	V _{SS}		H9	V _{DD} CORE	
B16	V _{SS}		D14	V _{DD} CORE		F12	V _{SS}		H10	V _{DD} CORE	

Table 21 PES24T6G2 (19x19mm 324-pin) Signal Pin-Out (Part 1 of 3)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
H11	V _{SS}		K13	V _{DD} PETA		M15	PE5RP03		P17	V _{DD} CORE	
H12	V _{DD} PEA		K14	V _{DD} CORE		M16	V _{SS}		P18	V _{SS}	
H13	V _{DD} PEA		K15	NC		M17	PE5TN03		R1	V _{SS}	
H14	PE5RN00		K16	V _{SS}		M18	PE5TP03		R2	V _{DD} CORE	
H15	PE5RP00		K17	REFRES5		N1	V _{SS}		R3	V _{DD} CORE	
H16	V _{SS}		K18	REFRES4		N2	V _{SS}		R4	PE1RP03	
H17	PE5TN00		L1	PE2TP01		N3	V _{SS}		R5	PE1RP02	
H18	PE5TP00		L2	PE2TN01		N4	V _{DD} CORE		R6	NC	
J1	PE2TP02		L3	V _{SS}		N5	V _{DD} CORE		R7	PE1RP01	
J2	PE2TN02		L4	PE2RP01		N6	V _{SS}		R8	PE1RP00	
J3	V _{SS}		L5	PE2RN01		N7	V _{SS}		R9	V _{DD} CORE	
J4	PE2RP02		L6	V _{DD} PETA		N8	V _{DD} PEA		R10	PE0RP03	
J5	PE2RN02		L7	V _{DD} PETA		N9	V _{DD} PEHA		R11	PE0RP02	
J6	V _{DD} PEHA		L8	V _{DD} PEA		N10	V _{DD} PETA		R12	V _{DD} CORE	
J7	V _{DD} PEHA		L9	V _{DD} PEHA		N11	V _{DD} PEA		R13	PE0RP01	
J8	V _{DD} CORE		L10	V _{DD} PETA		N12	V _{DD} PEHA		R14	PE0RP00	
J9	V _{SS}		L11	V _{DD} PEA		N13	V _{SS}		R15	V _{DD} CORE	
J10	V _{DD} CORE		L12	V _{DD} PEHA		N14	V _{SS}		R16	V _{DD} CORE	
J11	V _{SS}		L13	V _{DD} PETA		N15	V _{DD} CORE		R17	V _{DD} CORE	
J12	V _{DD} PEHA		L14	PE5RN02		N16	V _{SS}		R18	V _{SS}	
J13	V _{DD} PEHA		L15	PE5RP02		N17	V _{SS}		T1	V _{SS}	
J14	PE5RN01		L16	V _{SS}		N18	V _{SS}		T2	V _{SS}	
J15	PE5RP01		L17	PE5TN02		P1	V _{SS}		T3	V _{SS}	
J16	V _{SS}		L18	PE5TP02		P2	V _{DD} CORE		T4	V _{SS}	
J17	PE5TN01		M1	PE2TP00		P3	V _{DD} CORE		T5	V _{SS}	
J18	PE5TP01		M2	PE2TN00		P4	PE1RN03		T6	V _{SS}	
K1	REFRES2		M3	V _{SS}		P5	PE1RN02		T7	V _{SS}	
K2	REFRES3		M4	PE2RP00		P6	V _{DD} CORE		T8	V _{SS}	
K3	V _{SS}		M5	PE2RN00		P7	PE1RN01		T9	V _{SS}	
K4	V _{DD} CORE		M6	V _{DD} PETA		P8	PE1RN00		T10	V _{SS}	
K5	V _{DD} CORE		M7	V _{DD} PETA		P9	V _{DD} CORE		T11	V _{SS}	
K6	V _{DD} PETA		M8	V _{DD} PEA		P10	PE0RN03		T12	V _{SS}	
K7	V _{DD} PETA		M9	V _{DD} PEHA		P11	PE0RN02		T13	V _{SS}	
K8	V _{DD} CORE		M10	V _{DD} PETA		P12	V _{DD} CORE		T14	V _{SS}	
K9	V _{SS}		M11	V _{DD} PEA		P13	PE0RN01		T15	V _{SS}	
K10	V _{DD} CORE		M12	V _{DD} PEHA		P14	PE0RN00		T16	V _{SS}	
K11	V _{SS}		M13	V _{SS}		P15	V _{DD} CORE		T17	V _{SS}	

Table 21 PES24T6G2 (19x19mm 324-pin) Signal Pin-Out (Part 2 of 3)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
K12	V _{DD} PETA		M14	PE5RN03		P16	V _{DD} CORE		T18	V _{SS}	
U1	V _{SS}		U10	PE0TN03		V1	V _{SS}		V10	PE0TP03	
U2	PEREFCLKN		U11	PE0TN02		V2	PEREFCLKP		V11	PE0TP02	
U3	V _{SS}		U12	V _{SS}		V3	V _{SS}		V12	V _{SS}	
U4	PE1TN03		U13	PE0TN01		V4	PE1TP03		V13	PE0TP01	
U5	PE1TN02		U14	PE0TN00		V5	PE1TP02		V14	PE0TP00	
U6	REFRES1		U15	V _{SS}		V6	REFRES0		V15	V _{SS}	
U7	PE1TN01		U16	V _{SS}		V7	PE1TP01		V16	V _{SS}	
U8	PE1TN00		U17	V _{SS}		V8	PE1TP00		V17	V _{SS}	
U9	V _{SS}		U18	V _{SS}		V9	V _{SS}		V18	V _{SS}	

Table 21 PES24T6G2 (19x19mm 324-pin) Signal Pin-Out (Part 3 of 3)

Option A Package — Alternate Signal Functions

Pin	GPIO	Alternate
A12	GPIO_00	P2RSTN
B12	GPIO_01	P4RSTN
C12	GPIO_02	IOEXPINTN0
D12	GPIO_07	GPEN
D13	GPIO_08	P1RSTN
C13	GPIO_09	P3RSTN
B13	GPIO_10	P5RSTN

Table 22 PES24T6G2 (19x19mm 324-Pin) Alternate Signal Functions

Option A Package — Power Pins

V_{DD}Core	V_{DD}Core	V_{DD}Core	V_{DD}I/O	V_{DD}PEA	V_{DD}PEHA	V_{TT}PETA
D4	G9	N15	A2	G6	J6	K6
D5	G10	P2	A6	G7	J7	K7
D14	G14	P3	A10	G12	J12	K12
D15	G15	P6	A13	G13	J13	K13
E6	H8	P9	A14	H6	L9	L6
E7	H9	P12	A17	H7	L12	L7
E8	H10	P15	A18	H12	M9	L10
E10	J8	P16	B6	H13	M12	L13
E11	J10	P17	B7	L8	N9	M6
E12	K4	R2	B10	L11	N12	M7
E13	K5	R3	D6	M8		M10
F8	K8	R9		M11		N10
F10	K10	R12		N8		
G4	K14	R15		N11		
G5	N4	R16				
G8	N5	R17				

Table 23 PES24T6G2 (19x19mm 324-pin) Power Pins

Option A Package — Ground Pins

V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
A1	E9	H3	N2	T5	U12
A7	E16	H11	N3	T6	U15
A11	F3	H16	N6	T7	U16
A15	F6	J3	N7	T8	U17
A16	F7	J9	N13	T9	U18
B3	F9	J11	N14	T10	V1
B16	F11	J16	N16	T11	V3
C3	F12	K3	N17	T12	V9
C6	F13	K9	N18	T13	V12
C16	F16	K11	P1	T14	V15
D1	G1	K16	P18	T15	V16
D2	G2	L3	R1	T16	V17
D3	G3	L16	R18	T17	V18
D16	G11	M3	T1	T18	
D17	G16	M13	T2	U1	
D18	G17	M16	T3	U3	
E3	G18	N1	T4	U9	

Table 24 PES24T6G2 (19x19mm 324-pin) Ground Pins