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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

48-Lane 12-Port PCI Express® System Interconnect Switch

89HPES48H12
Data Sheet

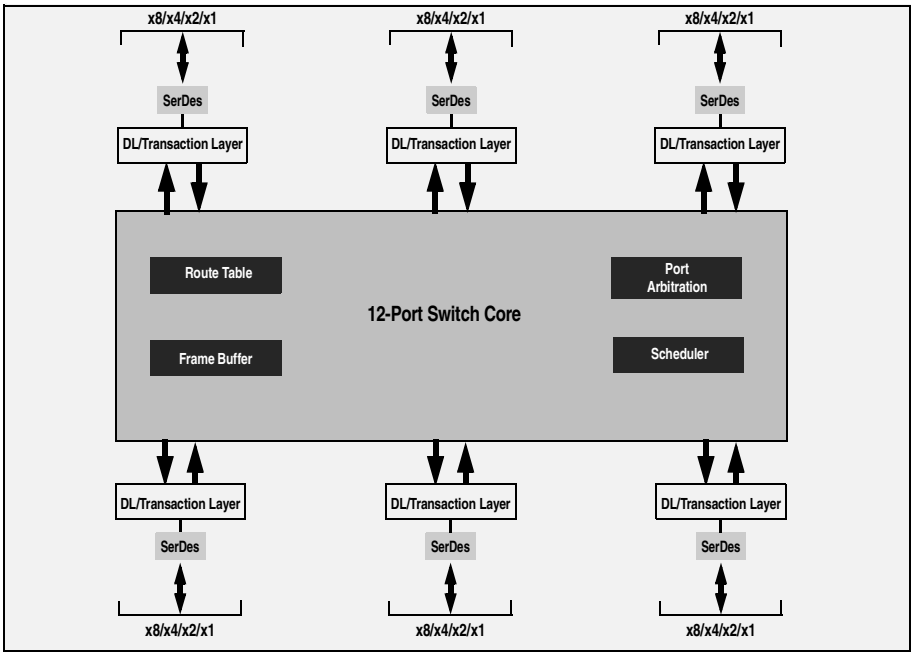
Device Overview

The 89HPES48H12 is a member of the IDT PRECISE™ family of PCI Express® switching solutions. The PES48H12 is a 48-lane, 12-port system interconnect switch optimized for PCI Express packet switching in high-performance applications, supporting multiple simultaneous peer-to-peer traffic flows. Target applications include servers, storage, communications, and embedded systems.

Features

- **High Performance PCI Express Switch**
  - *Twelve maximum switch ports*
    - Six main ports each of which consists of 8 SerDes
    - Each x8 main port can further bifurcate to 2 x4-ports
  - *Forty-eight 2.5 Gbps embedded SerDes*
    - Supports pre-emphasis and receive equalization on per-port basis
  - *Delivers 192 Gbps (24 GBps) of aggregate switching capacity*
  - *Low-latency cut-through switch architecture*
  - *Support for Max Payload Size up to 2048 bytes*
  - *Supports two virtual channels and eight traffic classes*
  - *PCI Express Base Specification Revision 1.1 compliant*
- **Flexible Architecture with Numerous Configuration Options**
  - *Port arbitration schemes utilizing round robin algorithms*
  - *Virtual channels arbitration based on priority*
  - *Automatic per port link width negotiation to x8, x4, x2 or x1*
  - *Supports automatic lane reversal on all ports*
  - *Supports automatic polarity inversion on all lanes*
  - *Supports locked transactions, allowing use with legacy software*
  - *Ability to load device configuration from serial EEPROM*
  - *Ability to control device via SMBus*
- **Highly Integrated Solution**
  - *Requires no external components*
  - *Incorporates on-chip internal memory for packet buffering and queueing*
  - *Integrates forty-eight 2.5 Gbps embedded full duplex SerDes, 8B/10B encoder/decoder (no separate transceivers needed)*
- **Reliability, Availability, and Serviceability (RAS) Features**
  - *Redundant upstream port failover capability*
  - *Supports optional PCI Express end-to-end CRC checking*
  - *Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)*

Block Diagram



48 PCI Express Lanes
Up to 6 x8 ports or 12 x4 Ports

Figure 1 Internal Block Diagram

  - *Supports optional PCI Express Advanced Error Reporting*
  - *Supports PCI Express Hot-Plug*
    - Compatible with Hot-Plug I/O expanders used on PC motherboards
  - *Supports Hot-Swap*
- **Power Management**
  - *Supports PCI Power Management Interface specification, Revision 1.1 (PCI-PM)*
    - Supports powerdown modes at the link level (L0, L0s, L1, L2/L3 Ready and L3) and at the device level (D0, $D3_{hot}$)
  - *Unused SerDes disabled*
- **Testability and Debug Features**
  - *Built in SerDes Pseudo-Random Bit Stream (PRBS) generator*
  - *Ability to read and write any internal register via the SMBus*
  - *Ability to bypass link training and force any link into any mode*
  - *Provides statistics and performance counters*
- **Thirty-two General Purpose Input/Output pins**
  - *Each pin may be individually configured as an input or output*
  - *Each pin may be individually configured as an interrupt input*
  - *Some pins have selectable alternate functions*
- **Packaged in a 35mm x 35mm 1156-ball Flip Chip BGA with 1mm ball spacing**

Product Description

Utilizing standard PCI Express interconnect, the PES48H12 provides the most efficient system interconnect switching solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides 192 Gbps of aggregated, full-duplex switching capacity through 48 integrated serial lanes, using proven and robust IDT technology. Each lane provides 2.5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification 1.1.

The PES48H12 is based on a flexible and efficient layered architecture. The PCI Express layers consist of SerDes, Physical, Data Link and Transaction layers. The PES48H12 can operate either as a store and forward switch or a cut-through switch and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and two Virtual Channels (VCs) with sophisticated resource management to enable efficient switching and I/O connectivity.

SMBus Interface

The PES48H12 contains two SMBus interfaces. The slave interface provides full access to the configuration registers in the PES48H12, allowing every configuration register in the device to be read or written by an external agent. The master interface allows the default configuration register values of the PES48H12 to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander.

Six pins make up each of the two SMBus interfaces. These pins consist of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins. In the slave interface, these address pins allow the SMBus address to which the device responds to be configured. In the master interface, these address pins allow the SMBus address of the serial configuration EEPROM from which data is loaded to be configured. The SMBus address is set up on negation of PERSTN by sampling the corresponding address pins. When the pins are sampled, the resulting address is assigned as shown in Table 1.

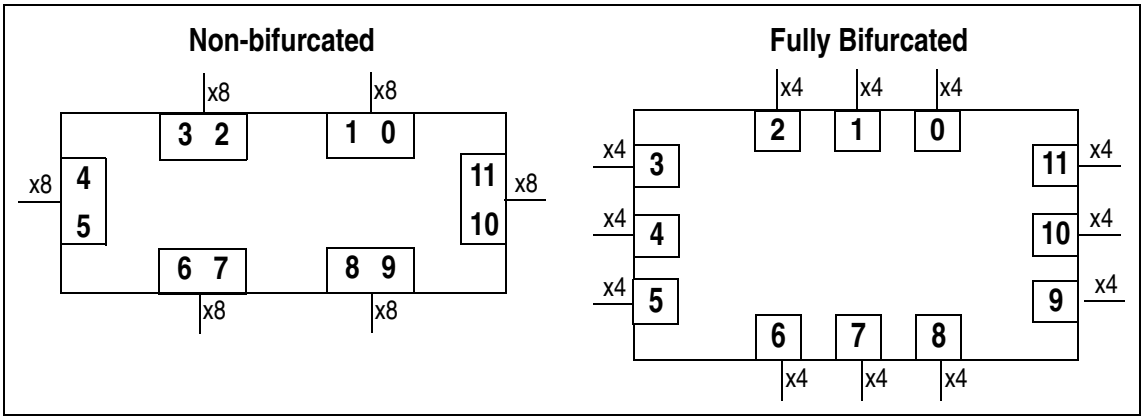


Figure 2 Port Configuration Examples

Note: The configurations in the above diagram show the maximum port widths. The PES48H12 can negotiate to narrower port widths — x4, x2, or x1.

Bit	Slave SMBus Address	Master SMBus Address
1	SSMBADDR[1]	MSMBADDR[1]
2	SSMBADDR[2]	MSMBADDR[2]
3	SSMBADDR[3]	MSMBADDR[3]
4	0	MSMBADDR[4]
5	SSMBADDR[5]	1
6	1	0
7	1	1

Table 1 Master and Slave SMBus Address Assignment

As shown in Figure 3, the master and slave SMBuses may be used in a unified or split configuration. In the unified configuration, shown in Figure 3(a), the master and slave SMBuses are tied together and the PES48H12 acts both as a SMBus master as well as a SMBus slave on this bus. This requires that the SMBus master or processor that has access to PES48H12 registers supports SMBus arbitration. In some systems, this SMBus master interface may be implemented using general purpose I/O pins on a processor or micro controller, and may not support SMBus arbitration. To support these systems, the PES48H12 may be configured to operate in a split configuration as shown in Figure 3(b).

In the split configuration, the master and slave SMBuses operate as two independent buses and thus multi-master arbitration is never required. The PES48H12 supports reading and writing of the serial EEPROM on the master SMBus via the slave SMBus, allowing in system programming of the serial EEPROM.

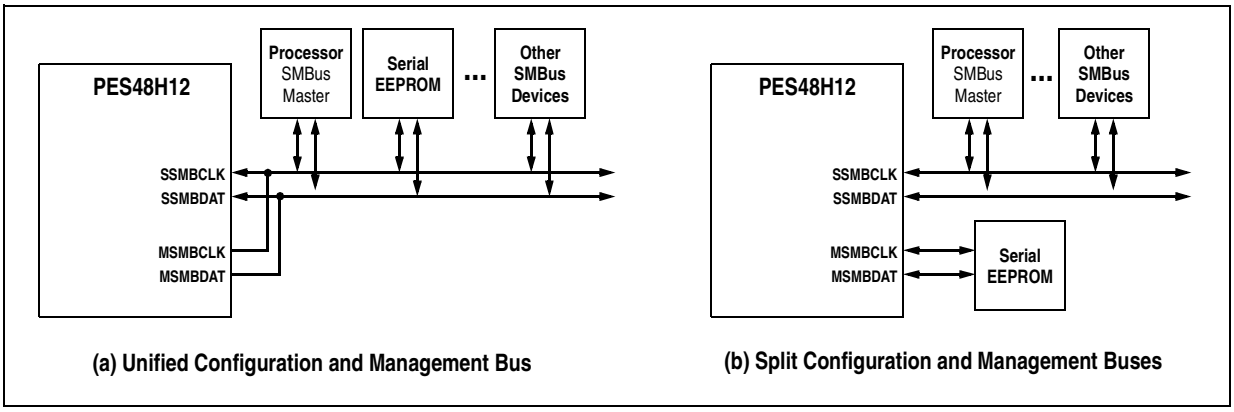


Figure 3 SMBus Interface Configuration Examples

Hot-Plug Interface

The PES48H12 supports PCI Express Hot-Plug on each downstream port (ports 1 through 11). To reduce the number of pins required on the device, the PES48H12 utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES48H12 generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES48H12. In response to an I/O expander interrupt, the PES48H12 generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

General Purpose Input/Output

The PES48H12 provides 32 General Purpose I/O (GPIO) pins that may be individually configured as general purpose inputs, general purpose outputs, or alternate functions. Some GPIO pins are shared with other on-chip functions. These alternate functions may be enabled via software, SMBus slave interface, or serial configuration EEPROM.

Pin Description

The following tables lists the functions of the pins provided on the PES48H12. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an “N” are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level. Differential signals end with a suffix “N” or “P.” The differential signal ending in “P” is the positive portion of the differential pair and the differential signal ending in “N” is the negative portion of the differential pair.

Signal	Type	Name/Description
PE0RP[3:0] PE0RN[3:0]	I	**PCI Express Port 0 Serial Data Receive.** Differential PCI Express receive pairs for port 0. Port 0 is the upstream port.
PE0TP[3:0] PE0TN[3:0]	O	**PCI Express Port 0 Serial Data Transmit.** Differential PCI Express transmit pairs for port 0. Port 0 is the upstream port.
PE1RP[3:0] PE1RN[3:0]	I	**PCI Express Port 1 Serial Data Receive.** Differential PCI Express receive pairs for port 1. When port 0 is merged with port 1, these signals become port 0 receive pairs for lanes 4 through 7.
PE1TP[3:0] PE1TN[3:0]	O	**PCI Express Port 1 Serial Data Transmit.** Differential PCI Express transmit pairs for port 1. When port 0 is merged with port 1, these signals become port 0 transmit pairs for lanes 4 through 7.
PE2RP[3:0] PE2RN[3:0]	I	**PCI Express Port 2 Serial Data Receive.** Differential PCI Express receive pairs for port 2.
PE2TP[3:0] PE2TN[3:0]	O	**PCI Express Port 2 Serial Data Transmit.** Differential PCI Express transmit pairs for port 2.
PE3RP[3:0] PE3RN[3:0]	I	**PCI Express Port 3 Serial Data Receive.** Differential PCI Express receive pairs for port 3. When port 2 is merged with port 3, these signals become port 2 receive pairs for lanes 4 through 7.
PE3TP[3:0] PE3TN[3:0]	O	**PCI Express Port 3 Serial Data Transmit.** Differential PCI Express transmit pairs for port 2. When port 2 is merged with port 3, these signals become port 2 transmit pairs for lanes 4 through 7.
PE4RP[3:0] PE4RN[3:0]	I	**PCI Express Port 4 Serial Data Receive.** Differential PCI Express receive pairs for port 4.
PE4TP[3:0] PE4TN[3:0]	O	**PCI Express Port 4 Serial Data Transmit.** Differential PCI Express transmit pairs for port 4.
PE5RP[3:0] PE5RN[3:0]	I	**PCI Express Port 5 Serial Data Receive.** Differential PCI Express receive pairs for port 5. When port 4 is merged with port 5, these signals become port 4 receive pairs for lanes 4 through 7.
PE5TP[3:0] PE5TN[3:0]	O	**PCI Express Port 5 Serial Data Transmit.** Differential PCI Express transmit pairs for port 5. When port 4 is merged with port 5, these signals become port 4 transmit pairs for lanes 4 through 7.
PE6RP[3:0] PE6RN[3:0]	I	**PCI Express Port 6 Serial Data Receive.** Differential PCI Express receive pairs for port 6.
PE6TP[3:0] PE6TN[3:0]	O	**PCI Express Port 6 Serial Data Transmit.** Differential PCI Express transmit pairs for port 6.
PE7RP[3:0] PE7RN[3:0]	I	**PCI Express Port 7 Serial Data Receive.** Differential PCI Express receive pairs for port 7. When port 6 is merged with port 7, these signals become port 6 receive pairs for lanes 4 through 7.

Table 2 PCI Express Interface Pins (Part 1 of 2)

Signal	Type	Name/Description
PE7TP[3:0] PE7TN[3:0]	O	**PCI Express Port 7 Serial Data Transmit.** Differential PCI Express transmit pairs for port 7. When port 6 is merged with port 7, these signals become port 6 transmit pairs for lanes 4 through 7.
PE8RP[3:0] PE8RN[3:0]	I	**PCI Express Port 8 Serial Data Receive.** Differential PCI Express receive pairs for port 8.
PE8TP[3:0] PE8TN[3:0]	O	**PCI Express Port 8 Serial Data Transmit.** Differential PCI Express transmit pairs for port 8.
PE9RP[3:0] PE9RN[3:0]	I	**PCI Express Port 9 Serial Data Receive.** Differential PCI Express receive pairs for port 9. When port 8 is merged with port 9, these signals become port 8 receive pairs for lanes 4 through 7.
PE9TP[3:0] PE9TN[3:0]	O	**PCI Express Port 9 Serial Data Transmit.** Differential PCI Express transmit pairs for port 9. When port 8 is merged with port 9, these signals become port 8 transmit pairs for lanes 4 through 7.
PE10RP[3:0] PE10RN[3:0]	I	**PCI Express Port 10 Serial Data Receive.** Differential PCI Express receive pairs for port 10.
PE10TP[3:0] PE10TN[3:0]	O	**PCI Express Port 10 Serial Data Transmit.** Differential PCI Express transmit pairs for port 10.
PE11RP[3:0] PE11RN[3:0]	I	**PCI Express Port 11 Serial Data Receive.** Differential PCI Express receive pairs for port 11. When port 10 is merged with port 11, these signals become port 10 receive pairs for lanes 4 through 7.
PE11TP[3:0] PE11TN[3:0]	O	**PCI Express Port 11 Serial Data Transmit.** Differential PCI Express transmit pairs for port 11. When port 10 is merged with port 11, these signals become port 10 transmit pairs for lanes 4 through 7.
REFCLKM	I	**PCI Express Reference Clock Mode Select.** This signal selects the frequency of the reference clock input. 0x0 - 100 MHz 0x1 - 125 MHz
REFCLKP[3:0] REFCLKN[3:0]	I	**PCI Express Reference Clock.** Differential reference clock pair input. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic and on-chip SerDes. The frequency of the differential reference clock is determined by the REFCLKM signal.

Table 2 PCI Express Interface Pins (Part 2 of 2)

Signal	Type	Name/Description
MSMBADDR[4:1]	I	**Master SMBus Address.** These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded.
MSMBCLK	I/O	**Master SMBus Clock.** This bidirectional signal is used to synchronize transfers on the master SMBus. It is active and generating the clock only when the EEPROM or I/O Expanders are being accessed.
MSMBDAT	I/O	**Master SMBus Data.** This bidirectional signal is used for data on the master SMBus.

Table 3 SMBus Interface Pins (Part 1 of 2)

Signal	Type	Name/Description
SSMBADDR[5,3:1]	I	**Slave SMBus Address.** These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	**Slave SMBus Clock.** This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	**Slave SMBus Data.** This bidirectional signal is used for data on the slave SMBus.

Table 3 SMBus Interface Pins (Part 2 of 2)

Signal	Type	Name/Description
GPIO[0]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[1]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[2]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[3]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[4]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[5]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: GPEN Alternate function pin type: Output Alternate function: General Purpose Event (GPE) output
GPIO[6]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P1RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 1
GPIO[7]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P2RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 2
GPIO[8]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P3RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 3
GPIO[9]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P4RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 4

Table 4 General Purpose I/O Pins (Part 1 of 3)

Signal	Type	Name/Description
GPIO[10]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P5RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 5
GPIO[11]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P6RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 6
GPIO[12]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P7RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 7
GPIO[13]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P8RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 8
GPIO[14]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P9RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 9
GPIO[15]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P10RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 10
GPIO[16]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P11RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 11
GPIO[17]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[18]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[19]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[20]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[21]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN0 Alternate function pin type: Input Alternate function: SMBus I/O expander interrupt 0

Table 4 General Purpose I/O Pins (Part 2 of 3)

Signal	Type	Name/Description
GPIO[22]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN1 Alternate function pin type: Input Alternate function: SMBus I/O expander interrupt 1
GPIO[23]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN2 Alternate function pin type: Input Alternate function: SMBus I/O expander interrupt 2
GPIO[24]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN3 Alternate function pin type: Input Alternate function: SMBus I/O expander interrupt 3
GPIO[25]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN4 Alternate function pin type: Input Alternate function: SMBus I/O expander interrupt 4
GPIO[26]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN5 Alternate function pin type: Input Alternate function: SMBus I/O expander interrupt 5
GPIO[27]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[28]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[29]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[30]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[31]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN10 Alternate function pin type: Input Alternate function: SMBus I/O expander interrupt 10

Table 4 General Purpose I/O Pins (Part 3 of 3)

Signal	Type	Name/Description
CCLKDS	I	**Common Clock Downstream.** When the CCLKDS pin is asserted, it indicates that a common clock is being used between the downstream device and the downstream port.
CCLKUS	I	**Common Clock Upstream.** When the CCLKUS pin is asserted, it indicates that a common clock is being used between the upstream device and the upstream port.
MSMBSMODE	I	**Master SMBus Slow Mode.** The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 KHz. This value may not be overridden.

Table 5 System Pins (Part 1 of 2)

Signal	Type	Name/Description
P01MERGEN	I	**Port 0 and 1 Merge.** P01MERGEN is an active low signal. It is pulled low internally via a 251K ohm resistor. When this pin is low, port 0 is merged with port 1 to form a single x8 port. The Serdes lanes associated with port 1 become lanes 4 through 7 of port 0. When this pin is high, port 0 and port 1 are not merged, and each operates as a single x4 port.
P23MERGEN	I	**Port 2 and 3 Merge.** P23MERGEN is an active low signal. It is pulled low internally via a 251K ohm resistor. When this pin is low, port 2 is merged with port 3 to form a single x8 port. The Serdes lanes associated with port 3 become lanes 4 through 7 of port 2. When this pin is high, port 2 and port 3 are not merged, and each operates as a single x4 port.
P45MERGEN	I	**Port 4 and 5 Merge.** P45MERGEN is an active low signal. It is pulled low internally via a 251K ohm resistor. When this pin is low, port 4 is merged with port 5 to form a single x8 port. The Serdes lanes associated with port 5 become lanes 4 through 7 of port 4. When this pin is high, port 4 and port 5 are not merged, and each operates as a single x4 port.
P67MERGEN	I	**Port 6 and 7 Merge.** P67MERGEN is an active low signal. It is pulled low internally via a 251K ohm resistor. When this pin is low, port 6 is merged with port 7 to form a single x8 port. The Serdes lanes associated with port 7 become lanes 4 through 7 of port 6. When this pin is high, port 6 and port 7 are not merged, and each operates as a single x4 port.
P89MERGEN	I	**Port 8 and 9 Merge.** P89MERGEN is an active low signal. It is pulled low internally via a 251K ohm resistor. When this pin is low, port 8 is merged with port 9 to form a single x8 port. The Serdes lanes associated with port 9 become lanes 4 through 7 of port 8. When this pin is high, port 8 and port 9 are not merged, and each operates as a single x4 port.
P1011MERGEN	I	**Port 10 and 11 Merge.** P67MERGEN is an active low signal. It is pulled low internally via a 251K ohm resistor. When this pin is low, port 10 is merged with port 11 to form a single x8 port. The Serdes lanes associated with port 11 become lanes 4 through 7 of port 10. When this pin is high, port 10 and port 11 are not merged, and each operates as a single x4 port.
PERSTN	I	**Fundamental Reset.** Assertion of this signal resets all logic inside PES48H12 and initiates a PCI Express fundamental reset.
RSTHALT	I	**Reset Halt.** When this signal is asserted during a PCI Express fundamental reset, PES48H12 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the PA_SWCTL register by an SMBus master.
SWMODE[3:0]	I	**Switch Mode.** These configuration pins determine the PES48H12 switch operating mode. These pins should be static and not change following the negation of PERSTN. 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM initialization 0x2 through 0x7 - Reserved 0x8 - Normal switch mode with upstream port failover (port 0 selected as the upstream port) 0x9 - Normal switch mode with upstream port failover (port 2 selected as the upstream port) 0xA - Normal switch mode with Serial EEPROM initialization and upstream port failover (port 0 selected as the upstream port) 0xB - Normal switch mode with Serial EEPROM initialization and upstream port failover (port 2 selected as the upstream port) 0xC through 0xF - Reserved

Table 5 System Pins (Part 2 of 2)

Signal	Type	Name/Description
JTAG_TCK	I	**JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input**. This is the serial data input to the boundary scan logic or JTAG Controller.
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	**JTAG Reset**. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 6 Test Pins

Signal	Type	Name/Description
V_{DD}CORE	I	**Core VDD.** Power supply for core logic.
V_{DD}IO	I	**I/O VDD.** LVTTL I/O buffer power supply.
V_{DD}PE	I	**PCI Express Digital Power.** PCI Express digital power used by the digital power of the SerDes.
V_{DD}APE	I	**PCI Express Analog Power.** PCI Express analog power used by the PLL and bias generator.
V_{SS}	I	**Ground.**
V_{TT}PE	I	**PCI Express Serial Data Transmit Termination Voltage.** This pin allows the driver termination voltage to be set, enabling the system designer to control the Common Mode Voltage and output voltage swing of the corresponding PCI Serial Data Transmit differential pair.

Table 7 Power and Ground Pins

Pin Characteristics

Note: Some input pads of the PES48H12 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes
PCI Express Interface	PE0RN[3:0]	I	CML	Serial Link		
	PE0RP[3:0]	I				
	PE0TN[3:0]	O				
	PE0TP[3:0]	O				
	PE1RN[3:0]	I				
	PE1RP[3:0]	I				
	PE1TN[3:0]	O				
	PE1TP[3:0]	O				
	PE2RN[3:0]	I				
	PE2RP[3:0]	I				
	PE2TN[3:0]	O				
	PE2TP[3:0]	O				
	PE3RN[3:0]	I				
	PE3RP[3:0]	I				
	PE3TN[3:0]	O				
	PE3TP[3:0]	O				
	PE4RN[3:0]	I				
	PE4RP[3:0]	I				
	PE4TN[3:0]	O				
	PE4TP[3:0]	O				
	PE5RN[3:0]	I				
	PE5RP[3:0]	I				
	PE5TN[3:0]	O				
	PE5TP[3:0]	O				
	PE6RN[3:0]	I				
	PE6RP[3:0]	I				
	PE6TN[3:0]	O				
	PE6TP[3:0]	O				
	PE7RN[3:0]	I				
	PE7RP[3:0]	I				
	PE7TN[3:0]	O				
	PE7TP[3:0]	O				

Table 8 Pin Characteristics (Part 1 of 3)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes
PCI Express Interface (cont.)	PE8RN[3:0]	I	CML	Serial Link		
	PE8RP[3:0]	I				
	PE8TN[3:0]	O				
	PE8TP[3:0]	O				
	PE9RN[3:0]	I				
	PE9RP[3:0]	I				
	PE9TN[3:0]	O				
	PE9TP[3:0]	O				
	PE10RN[3:0]	I				
	PE10RP[3:0]	I				
	PE10TN[3:0]	O				
	PE10TP[3:0]	O				
	PE11RN[3:0]	I				
	PE11RP[3:0]	I				
	PE11TN[3:0]	O				
	PE11TP[3:0]	O				
	PEREFCLKN[3:0]	I	LVPECL/ CML	Diff. Clock Input		Refer to Table 9
	PEREFCLKP[3:0]	I				
	REFCLKM	I	LVTTL	Input	pull-down	
SMBus Interface	MSMBADDR[4:1]	I	LVTTL	STI[1]	pull-up	
	MSMBCLK	I/O		STI		
	MSMBDAT	I/O		STI		
	SSMBADDR[5,3:1]	I			pull-up	
	SSMBCLK	I/O		STI		
	SSMBDAT	I/O		STI		
General Purpose I/O	GPIO[31:0]	I/O	LVTTL		pull-up	
System Pins	CCLKDS	I	LVTTL	Input	pull-up	
	CCLKUS	I			pull-up	
	MSMBSMODE	I			pull-down	
	P01MERGEN	I			pull-down	
	P23MERGEN	I			pull-down	
	P45MERGEN	I			pull-down	
	P67MERGEN	I			pull-down	
	P89MERGEN	I			pull-down	
	P1011MERGEN	I			pull-down	
	PERSTN	I				
	RSTHALT	I			pull-down	
	SWMODE[3:0]	I			pull-down	

Table 8 Pin Characteristics (Part 2 of 3)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes
EJTAG / JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I		STI	pull-up	
	JTAG_TDO	O				
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I		STI	pull-up	External pull-down

Table 8 Pin Characteristics (Part 3 of 3)

1. Schmitt Trigger Input (STI).

Logic Diagram — PES48H12

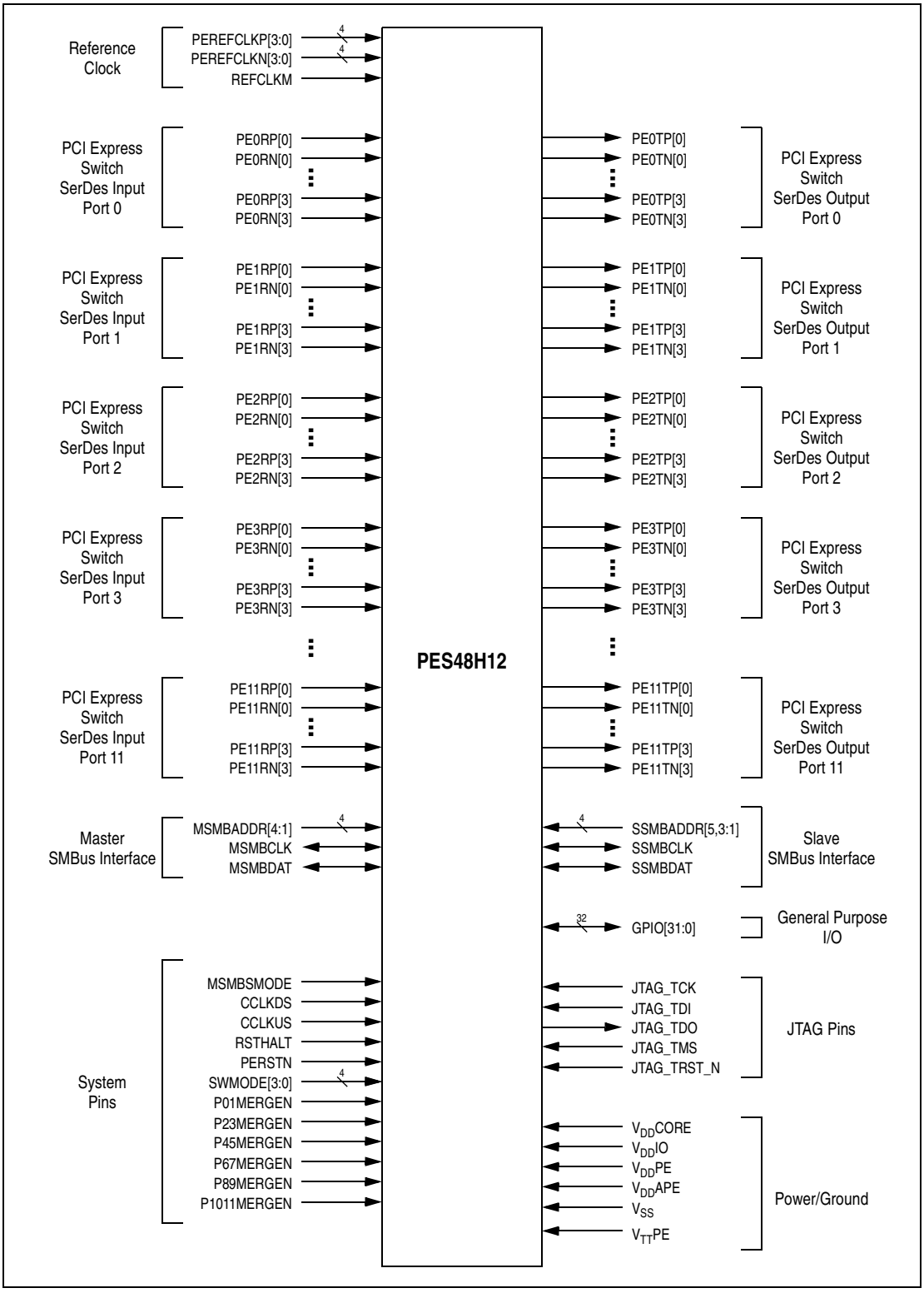


Figure 4 PES48H12 Logic Diagram

System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 13 and 15.

Parameter	Description	Min	Typical	Max	Unit
PEREFCLK					
$Refclk_{FREQ}$	Input reference clock frequency range	100		125[1]	MHz
$Refclk_{DC}$[2]	Duty cycle of input clock	40	50	60	%
T_R, T_F	Rise/Fall time of input clocks			0.2*RCUI	RCUI[3]
V_{SW}	Differential input voltage swing[4]	0.6		1.6	V
T_{jitter}	Input clock jitter (cycle-to-cycle)			125	ps
R_T	Termination Resistor		110		Ohms

Table 9 Input Clock Requirements

1. The input clock frequency will be either 100 or 125 MHz depending on signal REFCLKM.
2. ClkIn must be AC coupled. Use 0.01 — 0.1 µF ceramic capacitors.
3. RCUI (Reference Clock Unit Interval) refers to the reference clock period.
4. AC coupling required.

AC Timing Characteristics

Parameter	Description	Min[1]	Typical[1]	Max[1]	Units
PCIe Transmit					
UI	Unit Interval	399.88	400	400.12	ps
T_{TX-EYE}	Minimum Tx Eye Width	0.7	.9		UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.15	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+ / D- Tx output rise/fall time	50	90		ps
$T_{TX-IDLE-MIN}$	Minimum time in idle	50			UI
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Idle after sending an Idle ordered set			20	UI
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition from valid idle to diff data			20	UI
$T_{TX-SKEW}$	Transmitter data skew between any 2 lanes		500	1300	ps
PCIe Receive					
UI	Unit Interval	399.88	400	400.12	ps
T_{RX-EYE} (with jitter)	Minimum Receiver Eye Width (jitter tolerance)	0.4			UI
$T_{RX-EYE-MEDIUM TO MAX JITTER}$	Max time between jitter median & max deviation			0.3	UI
$T_{RX-IDLE-DET-DIFF-ENTER TIME}$	Unexpected Idle Enter Detect Threshold Integration Time			10	ms
$T_{RX-SKEW}$	Lane to lane input skew			20	ns

Table 10 PCIe AC Timing Characteristics

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.1

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[31:0][1]	Tpw_13b[2]	None	50	—	ns	See Figure 5.

Table 11 GPIO AC Timing Characteristics

1. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

2. The values for this symbol were determined by calculation, not by testing.

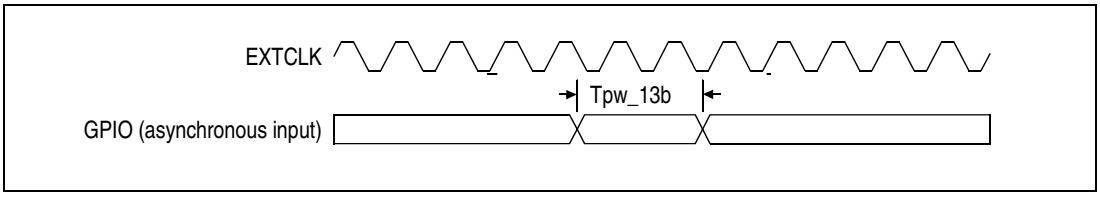


Figure 5 GPIO AC Timing Waveform

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	50.0	—	ns	See Figure 6.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	20	ns	
	Tdz_16c[2]		—	20	ns	
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	ns	

Table 12 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

2. The values for this symbol were determined by calculation, not by testing.

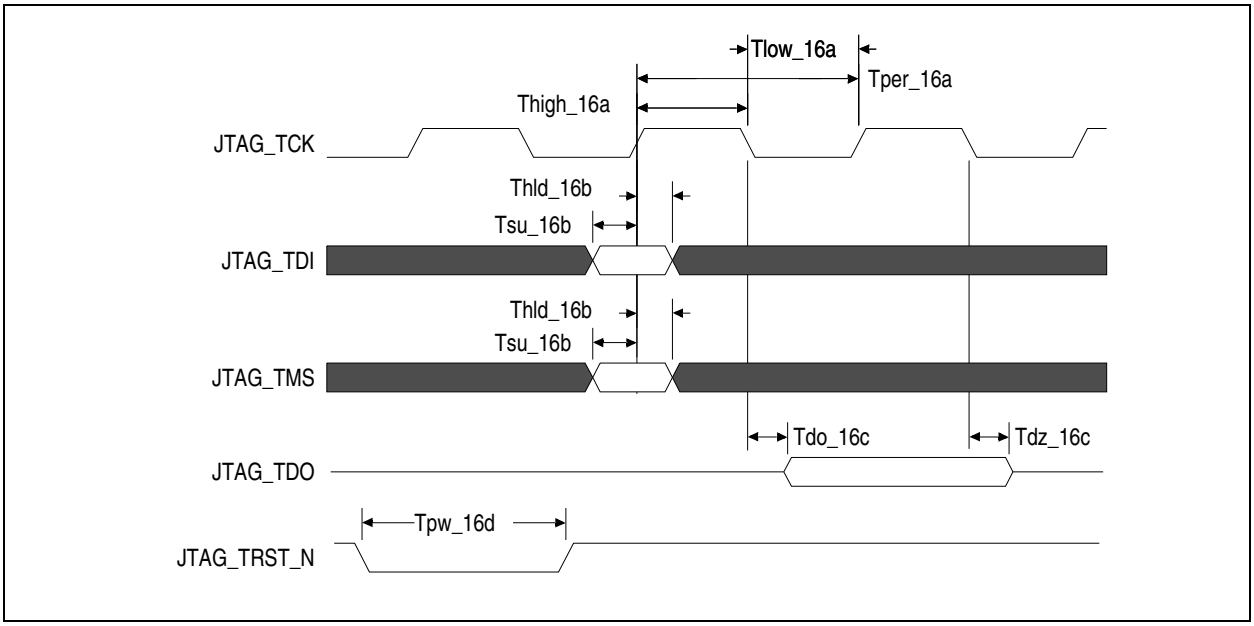


Figure 6 JTAG AC Timing Waveform

Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}CORE	Internal logic supply	0.9	1.0	1.1	V
V_{DD}I/O	I/O supply except for SerDes LVPECL/CML	3.0	3.3	3.6	V
V_{DD}PE	PCI Express Digital Power	0.9	1.0	1.1	V
V_{DD}APE	PCI Express Analog Power	0.9	1.0	1.1	V
V_{TT}PE	PCI Express Serial Data Transmit Termination Voltage	1.425	1.5	1.575	V
V_{SS}	Common ground	0	0	0	V

Table 13 PES48H12 Operating Voltages

Absolute Maximum Voltage Rating

V_{DD}Core	V_{DD}PE	V_{DD}APE	V_{TT}PE	V_{DD}I/O
1.5V	1.5V	1.5V	2.5V	5.0V

Table 14 PES48H12 Absolute Maximum Voltage Rating

Warning: For proper and reliable operation in adherence with this data sheet, the device should not exceed the recommended operating voltages in Table 13. The absolute maximum operating voltages in Table 14 are offered to provide guidelines for voltage excursions outside the recommended voltage ranges. Device functionality is not guaranteed at these conditions and sustained operation at these values or any exposure to voltages outside the maximum range may adversely affect device functionality and reliability.

Power-Up Sequence

This section describes the sequence in which various voltages must be applied to the part during power-up to ensure proper functionality. For the PES48H12, the power-up sequence must be as follows:

1. V_{DD}I/O — 3.3V
2. V_{DD}Core, V_{DD}PE, V_{DD}APE — 1.0V
3. V_{TT}PE — 1.5V

When powering up, each voltage level must ramp and stabilize prior to applying the next voltage in the sequence to ensure internal latch-up issues are avoided. There are no maximum time limitations in ramping to valid power levels. The power-down sequence must be in the reverse order of the power-up sequence.

Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 15 PES48H12 Operating Temperatures

Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 13 (and also listed below).

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 13 (and also listed below).

Number of active Lanes per Port		Core Supply		PCIe Digital Supply		PCIe Analog Supply		PCIe Termination Supply		I/O Supply		Total	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 1.5V	Max 1.575V	Typ 3.3V	Max 3.6V	Typ Power	Max Power
8/8/8/8/8/8	**mA**	2254	2774	2268	2797	966	1186	1133	1397	4	4		
	Watts	2.26	3.05	2.27	3.08	0.97	1.31	1.7	2.2	0.01	0.01	7.21W	9.65W

Table 16 PES48H12 Power Consumption

Thermal Considerations

This section describes thermal considerations for the PES48H12 (35mm^2 FCBGA1156 package). The data in Table 17 below contains information that is relevant to the thermal performance of the PES48H12 switch.

Symbol	Parameter	Value	Units	Conditions
$T_{J(max)}$	Junction Temperature	125	°C	Maximum
$T_{A(max)}$	Ambient Temperature	70	°C	Maximum for commercial-rated products
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	12.6	°C/W	Zero air flow
		6.4	°C/W	1 m/S air flow
		5.4	°C/W	2 m/S air flow
θ_{JB}	Thermal Resistance, Junction-to-Board	2.1	°C/W	
θ_{JC}	Thermal Resistance, Junction-to-Case	0.1	°C/W	
P	Power Dissipation of the Device	6.82	Watts	Maximum

Table 17 Thermal Specifications for PES48H12, 35x35mm FCBGA1156 Package

Note: It is important for the reliability of this device in any user environment that the junction temperature not exceed the $T_{J(max)}$ value specified in Table 17. Consequently, the effective junction to ambient thermal resistance (θ_{JA}) for the worst case scenario must be maintained below the value determined by the formula:

$$\theta_{JA} = (T_{J(max)} - T_{A(max)})/P$$

Given that the values of $T_{J(max)}$, $T_{A(max)}$, and P are known, the value of desired θ_{JA} becomes a known entity to the system designer. How to achieve the desired θ_{JA} is left up to the board or system designer, but in general, it can be achieved by adding the effects of θ_{JC} (value provided in Table 17), thermal resistance of the chosen adhesive (θ_{CS}), that of the heat sink (θ_{SA}), amount of airflow, and properties of the circuit board (number of layers and size of the board). As a general guideline, this device will not need a heat sink if the board has 10 or more layers AND the board size is larger than 4"x12" AND airflow in excess of 1 m/s is available. It is strongly recommended that users perform their own thermal analysis for their own board and system design scenarios.

DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 13.

Note: See Table 8, Pin Characteristics, for a complete I/O listing.

I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Serial Link	**PCIe Transmit**						
	$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	800		1200	mV	
	$V_{TX-DE-RATIO}$	De-emphasized differential output voltage	-3		-4	dB	
	$V_{TX-DC-CM}$	DC Common mode voltage	-0.1	1	3.7	V	
	$V_{TX-CM-ACP}$	RMS AC peak common mode output voltage			20	mV	
	$V_{TX-CM-DC-active-idle-delta}$	Abs delta of DC common mode voltage between L0 and idle			100	mV	
	$V_{TX-CM-DC-line-delta}$	Abs delta of DC common mode voltage between D+ and D-			25	mV	
	$V_{TX-Idle-DiffP}$	Electrical idle diff peak output			20	mV	
	$V_{TX-RCV-Detect}$	Voltage change during receiver detection			600	mV	
	$RL_{TX-DIFF}$	Transmitter Differential Return loss	12			dB	
	RL_{TX-CM}	Transmitter Common Mode Return loss	6			dB	
	$Z_{TX-DEFF-DC}$	DC Differential TX impedance	80	100	120	Ω	
	Z_{OSE}	Single ended TX Impedance	40	50	60	Ω	
	Transmitter Eye Diagram	TX Eye Height (De-emphasized bits)	505	650		mV	
	Transmitter Eye Diagram	TX Eye Height (Transition bits)	800	950		mV	
	PCIe Receive						
	$V_{RX-DIFFp-p}$	Differential input voltage (peak-to-peak)	175		1200	mV	
	$V_{RX-CM-AC}$	Receiver common-mode voltage for AC coupling			150	mV	
	$RL_{RX-DIFF}$	Receiver Differential Return Loss	15			dB	
	RL_{RX-CM}	Receiver Common Mode Return Loss	6			dB	
	$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	Ω	
	$Z_{RX-COMM-DC}$	Single-ended input impedance	40	50	60	Ω	
	$Z_{RX-COMM-HIGH-Z-DC}$	Powered down input common mode impedance (DC)	200k	350k		Ω	
	$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	mV	
PCIe REFCLK							
	C_{IN}	Input Capacitance	1.5	—		pF	

Table 18 DC Electrical Characteristics (Part 1 of 2)

I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Other I/Os							
LOW Drive Output	I_{OL}		—	2.5	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-5.5	—	mA	V_{OH} = 1.5V
High Drive Output	I_{OL}		—	12.0	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-20.0	—	mA	V_{OH} = 1.5V
Schmitt Trigger Input (STI)	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	$V_{DD}IO$ + 0.5	V	—
Input	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	$V_{DD}IO$ + 0.5	V	—
Capacitance	C_{IN}		—	—	8.5	pF	—
Leakage	Inputs		—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/downs		—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ WITH}$ Pull-ups/downs		—	—	± 80	µA	V_{DD}I/O (max)

Table 18 DC Electrical Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.0a.

Package Pinout — 1156-BGA Signal Pinout for PES48H12

The following table lists the pin numbers and signal names for the PES48H12 device.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	V_{SS}		B1	V_{SS}		C1	GPIO_29		D1	GPIO_28	
A2	V_{SS}		B2	$V_{DD}IO$		C2	GPIO_27		D2	GPIO_26	1
A3	GPIO_19		B3	GPIO_18		C3	GPIO_21	1	D3	$V_{DD}IO$	
A4	$V_{DD}IO$		B4	GPIO_17		C4	GPIO_16	1	D4	GPIO_23	1
A5	V_{SS}		B5	V_{SS}		C5	V_{SS}		D5	V_{SS}	
A6	PE9TP03		B6	PE9TN03		C6	V_{SS}		D6	PE9RP03	
A7	PE9TP02		B7	PE9TN02		C7	V_{SS}		D7	PE9RP02	
A8	V_{SS}		B8	V_{SS}		C8	V_{SS}		D8	V_{SS}	
A9	PE9TP01		B9	PE9TN01		C9	V_{SS}		D9	PE9RP01	
A10	PE9TP00		B10	PE9TN00		C10	V_{SS}		D10	PE9RP00	
A11	V_{SS}		B11	V_{SS}		C11	V_{SS}		D11	V_{SS}	
A12	PE8TP03		B12	PE8TN03		C12	V_{SS}		D12	PE8RP03	
A13	PE8TP02		B13	PE8TN02		C13	V_{SS}		D13	PE8RP02	
A14	V_{SS}		B14	V_{SS}		C14	V_{SS}		D14	V_{SS}	
A15	PE8TP01		B15	PE8TN01		C15	V_{SS}		D15	PE8RP01	
A16	PE8TP00		B16	PE8TN00		C16	V_{SS}		D16	PE8RP00	
A17	V_{SS}		B17	V_{SS}		C17	V_{SS}		D17	V_{SS}	
A18	PE3TP03		B18	PE3TN03		C18	V_{SS}		D18	PE3RP03	
A19	PE3TP02		B19	PE3TN02		C19	V_{SS}		D19	PE3RP02	
A20	V_{SS}		B20	V_{SS}		C20	V_{SS}		D20	V_{SS}	
A21	PE3TP01		B21	PE3TN01		C21	V_{SS}		D21	PE3RP01	
A22	PE3TP00		B22	PE3TN00		C22	V_{SS}		D22	PE3RP00	
A23	V_{SS}		B23	V_{SS}		C23	V_{SS}		D23	V_{SS}	
A24	PE2TP03		B24	PE2TN03		C24	V_{SS}		D24	PE2RP03	
A25	PE2TP02		B25	PE2TN02		C25	V_{SS}		D25	PE2RP02	
A26	V_{SS}		B26	V_{SS}		C26	V_{SS}		D26	V_{SS}	
A27	PE2TP01		B27	PE2TN01		C27	V_{SS}		D27	PE2RP01	
A28	PE2TP00		B28	PE2TN00		C28	V_{SS}		D28	PE2RP00	
A29	V_{SS}		B29	V_{SS}		C29	V_{SS}		D29	V_{SS}	
A30	$V_{DD}IO$		B30	MSMBADDR_3		C30	MSMBADDR_4		D30	JTAG_TMS	
A31	MSMBADDR_1		B31	MSMBADDR_2		C31	JTAG_TDI		D31	$V_{DD}IO$	
A32	MSMBSMODE		B32	PERSTN		C32	JTAG_TRST_N		D32	SSMBADDR_5	
A33	V_{SS}		B33	$V_{DD}IO$		C33	SSMBADDR_2		D33	SSMBADDR_3	
A34	V_{SS}		B34	V_{SS}		C34	SSMBADDR_1		D34	$V_{DD}IO$	

Table 19 PES48H12 1156-pin Signal Pin-Out (Part 1 of 9)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
E1	$V_{DD}IO$		F1	V_{SS}		G1	PE10TP00		H1	PE10TP01	
E2	GPIO_30		F2	V_{SS}		G2	PE10TN00		H2	PE10TN01	
E3	GPIO_31	1	F3	V_{SS}		G3	V_{SS}		H3	V_{SS}	
E4	GPIO_24	1	F4	V_{SS}		G4	PE10RP00		H4	PE10RP01	
E5	V_{SS}		F5	V_{SS}		G5	PE10RN00		H5	PE10RN01	
E6	PE9RN03		F6	V_{SS}		G6	V_{SS}		H6	V_{SS}	
E7	PE9RN02		F7	V_{SS}		G7	V_{SS}		H7	V_{SS}	
E8	V_{SS}		F8	V_{SS}		G8	V_{SS}		H8	GPIO_20	
E9	PE9RN01		F9	V_{SS}		G9	V_{SS}		H9	$V_{DD}IO$	
E10	PE9RN00		F10	V_{SS}		G10	V_{SS}		H10	V_{SS}	
E11	V_{SS}		F11	V_{SS}		G11	V_{SS}		H11	V_{SS}	
E12	PE8RN03		F12	V_{SS}		G12	V_{SS}		H12	V_{SS}	
E13	PE8RN02		F13	V_{SS}		G13	V_{SS}		H13	$V_{TT}PE$	
E14	V_{SS}		F14	V_{SS}		G14	V_{SS}		H14	V_{SS}	
E15	PE8RN01		F15	V_{SS}		G15	V_{SS}		H15	$V_{DD}APE$	
E16	PE8RN00		F16	V_{SS}		G16	V_{SS}		H16	V_{SS}	
E17	V_{SS}		F17	V_{SS}		G17	PEREFCLKP1		H17	V_{SS}	
E18	PE3RN03		F18	V_{SS}		G18	PEREFCLKN1		H18	V_{SS}	
E19	PE3RN02		F19	V_{SS}		G19	V_{SS}		H19	V_{SS}	
E20	V_{SS}		F20	V_{SS}		G20	V_{SS}		H20	$V_{DD}APE$	
E21	PE3RN01		F21	V_{SS}		G21	V_{SS}		H21	V_{SS}	
E22	PE3RN00		F22	V_{SS}		G22	V_{SS}		H22	$V_{TT}PE$	
E23	V_{SS}		F23	V_{SS}		G23	V_{SS}		H23	V_{SS}	
E24	PE2RN03		F24	V_{SS}		G24	V_{SS}		H24	V_{SS}	
E25	PE2RN02		F25	V_{SS}		G25	V_{SS}		H25	V_{SS}	
E26	V_{SS}		F26	V_{SS}		G26	V_{SS}		H26	MSMBDAT	
E27	PE2RN01		F27	V_{SS}		G27	MSMBCLK		H27	$V_{DD}IO$	
E28	PE2RN00		F28	V_{SS}		G28	V_{SS}		H28	SSMBCLK	
E29	V_{SS}		F29	V_{SS}		G29	V_{SS}		H29	V_{SS}	
E30	V_{SS}		F30	PE1RN03		G30	PE1RN02		H30	V_{SS}	
E31	V_{SS}		F31	PE1RP03		G31	PE1RP02		H31	V_{SS}	
E32	V_{SS}		F32	V_{SS}		G32	V_{SS}		H32	V_{SS}	
E33	V_{SS}		F33	PE1TN03		G33	PE1TN02		H33	V_{SS}	
E34	V_{SS}		F34	PE1TP03		G34	PE1TP02		H34	V_{SS}	

Table 19 PES48H12 1156-pin Signal Pin-Out (Part 2 of 9)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
J1	V_{SS}		K1	PE10TP02		L1	PE10TP03		M1	V_{SS}	
J2	V_{SS}		K2	PE10TN02		L2	PE10TN03		M2	V_{SS}	
J3	V_{SS}		K3	V_{SS}		L3	V_{SS}		M3	V_{SS}	
J4	V_{SS}		K4	PE10RP02		L4	PE10RP03		M4	V_{SS}	
J5	V_{SS}		K5	PE10RN02		L5	PE10RN03		M5	V_{SS}	
J6	V_{SS}		K6	V_{SS}		L6	V_{SS}		M6	V_{SS}	
J7	V_{SS}		K7	V_{SS}		L7	V_{SS}		M7	V_{SS}	
J8	V_{SS}		K8	V_{SS}		L8	V_{SS}		M8	V_{SS}	
J9	GPIO_25	1	K9	VDDIO		L9	V_{SS}		M9	V_{SS}	
J10	V_{SS}		K10	GPIO_22	1	L10	V_{SS}		M10	V_{SS}	
J11	V_{SS}		K11	V_{SS}		L11	V_{SS}		M11	V_{SS}	
J12	V_{SS}		K12	V_{SS}		L12	V_{SS}		M12	V_{SS}	
J13	V_{SS}		K13	V_{TT}PE		L13	V_{DD}PE		M13	V_{DD}PE	
J14	V_{DD}PE		K14	V_{SS}		L14	V_{DD}PE		M14	V_{SS}	
J15	V_{SS}		K15	V_{DD}APE		L15	V_{DD}PE		M15	V_{DD}PE	
J16	V_{SS}		K16	V_{SS}		L16	V_{SS}		M16	V_{SS}	
J17	V_{TT}PE		K17	V_{TT}PE		L17	V_{DD}PE		M17	V_{DD}PE	
J18	V_{TT}PE		K18	V_{TT}PE		L18	V_{DD}PE		M18	V_{DD}PE	
J19	V_{SS}		K19	V_{SS}		L19	V_{SS}		M19	V_{SS}	
J20	V_{SS}		K20	V_{DD}APE		L20	V_{DD}PE		M20	V_{DD}PE	
J21	V_{DD}PE		K21	V_{SS}		L21	V_{DD}PE		M21	V_{SS}	
J22	V_{SS}		K22	V_{TT}PE		L22	V_{DD}PE		M22	V_{DD}PE	
J23	V_{SS}		K23	V_{SS}		L23	V_{SS}		M23	V_{SS}	
J24	V_{SS}		K24	V_{SS}		L24	V_{SS}		M24	V_{SS}	
J25	JTAG_TDO		K25	CCLKDS		L25	V_{SS}		M25	V_{SS}	
J26	V_{DD}IO		K26	JTAG_TCK		L26	V_{SS}		M26	V_{SS}	
J27	SSMBDAT		K27	V_{SS}		L27	V_{SS}		M27	V_{SS}	
J28	V_{SS}		K28	V_{SS}		L28	V_{SS}		M28	V_{SS}	
J29	V_{SS}		K29	V_{SS}		L29	V_{SS}		M29	V_{SS}	
J30	PE1RN01		K30	PE1RN00		L30	V_{SS}		M30	PE0RN03	
J31	PE1RP01		K31	PE1RP00		L31	V_{SS}		M31	PE0RP03	
J32	V_{SS}		K32	V_{SS}		L32	V_{SS}		M32	V_{SS}	
J33	PE1TN01		K33	PE1TN00		L33	V_{SS}		M33	PE0TN03	
J34	PE1TP01		K34	PE1TP00		L34	V_{SS}		M34	PE0TP03	

Table 19 PES48H12 1156-pin Signal Pin-Out (Part 3 of 9)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
N1	PE11TP00		P1	PE11TP01		R1	V_{SS}		T1	PE11TP02	
N2	PE11TN00		P2	PE11TN01		R2	V_{SS}		T2	PE11TN02	
N3	V_{SS}		P3	V_{SS}		R3	V_{SS}		T3	V_{SS}	
N4	PE11RP00		P4	PE11RP01		R4	V_{SS}		T4	PE11RP02	
N5	PE11RN00		P5	PE11RN01		R5	V_{SS}		T5	PE11RN02	
N6	V_{SS}		P6	V_{SS}		R6	V_{SS}		T6	V_{SS}	
N7	V_{SS}		P7	V_{SS}		R7	V_{SS}		T7	V_{SS}	
N8	V_{TT}PE		P8	V_{SS}		R8	V_{DD}APE		T8	V_{SS}	
N9	V_{SS}		P9	V_{DD}PE		R9	V_{SS}		T9	V_{SS}	
N10	V_{TT}PE		P10	V_{SS}		R10	V_{DD}APE		T10	V_{SS}	
N11	V_{DD}PE		P11	V_{DD}PE		R11	V_{DD}PE		T11	V_{SS}	
N12	V_{DD}PE		P12	V_{SS}		R12	V_{DD}PE		T12	V_{SS}	
N13	V_{DD}CORE		P13	V_{DD}CORE		R13	V_{DD}CORE		T13	V_{SS}	
N14	V_{DD}CORE		P14	V_{SS}		R14	V_{DD}CORE		T14	V_{SS}	
N15	V_{DD}CORE		P15	V_{DD}CORE		R15	V_{SS}		T15	V_{DD}CORE	
N16	V_{SS}		P16	V_{SS}		R16	V_{DD}CORE		T16	V_{SS}	
N17	V_{DD}CORE		P17	V_{DD}CORE		R17	V_{SS}		T17	V_{DD}CORE	
N18	V_{SS}		P18	V_{SS}		R18	V_{DD}CORE		T18	V_{SS}	
N19	V_{DD}CORE		P19	V_{DD}CORE		R19	V_{SS}		T19	V_{DD}CORE	
N20	V_{DD}CORE		P20	V_{SS}		R20	V_{DD}CORE		T20	V_{SS}	
N21	V_{DD}CORE		P21	V_{DD}CORE		R21	V_{SS}		T21	V_{DD}CORE	
N22	V_{DD}CORE		P22	V_{DD}CORE		R22	V_{DD}CORE		T22	V_{DD}CORE	
N23	V_{DD}PE		P23	V_{SS}		R23	V_{DD}PE		T23	V_{SS}	
N24	V_{DD}PE		P24	V_{DD}PE		R24	V_{DD}PE		T24	V_{SS}	
N25	V_{TT}PE		P25	V_{SS}		R25	V_{DD}APE		T25	V_{SS}	
N26	V_{SS}		P26	V_{DD}PE		R26	V_{SS}		T26	V_{SS}	
N27	V_{TT}PE		P27	V_{SS}		R27	V_{DD}APE		T27	V_{SS}	
N28	V_{SS}		P28	V_{SS}		R28	V_{SS}		T28	V_{SS}	
N29	V_{SS}		P29	V_{SS}		R29	V_{SS}		T29	V_{SS}	
N30	PE0RN02		P30	V_{SS}		R30	PE0RN01		T30	PE0RN00	
N31	PE0RP02		P31	V_{SS}		R31	PE0RP01		T31	PE0RP00	
N32	V_{SS}		P32	V_{SS}		R32	V_{SS}		T32	V_{SS}	
N33	PE0TN02		P33	V_{SS}		R33	PE0TN01		T33	PE0TN00	
N34	PE0TP02		P34	V_{SS}		R34	PE0TP01		T34	PE0TP00	

Table 19 PES48H12 1156-pin Signal Pin-Out (Part 4 of 9)