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IDT™ 89HPES4T4
PCI Express® Switch

Preliminary User Manual

February 2011

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About this Manual

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Introduction

This user manual includes hardware and software information on the 89HPES4T4, a member of IDT's PRECISE™ family of PCI Express® switching solutions offering the next-generation I/O interconnect standard.

Finding Additional Information

Information not included in this manual such as mechanicals, package pin-outs, and electrical characteristics can be found in the data sheet for this device, which is available from the IDT website **(www.idt.com)** as well as through your local IDT sales representative.

Content Summary

Chapter 1, "PES4T4 Device Overview," provides a complete introduction to the performance capabilities of the 89HPES4T4. Included in this chapter is a summary of features for the device as well as a system block diagram and pin description.

Chapter 2, "Clocking, Reset, and Initialization," provides a description of the two differential reference clock inputs that are used internally to generate all of the clocks required by the internal switch logic and the SerDes.

Chapter 3, "Theory of Operation," describes the operation of the link feature including polarity inversion, link width negotiation, and lane reversal.

Chapter 4, "Link Operation," describes the operation of the link feature including polarity inversion, link width negotiation, and lane reversal.

Chapter 5, "General Purpose I/O," describes how the 16 General Purpose I/O (GPIO) pins may be individually configured as general purpose inputs, general purpose outputs, or alternate functions.

Chapter 6, "SMBus Interfaces," describes the operation of the SMBus master interface on the PES4T4.

Chapter 7, "Power Management," describes the power management capability structure located in the configuration space of each PCI-PCI bridge in the PES4T4.

Chapter 8, "Hot-Plug and Hot-Swap," describes the behavior of the hot-plug and hot-swap features in the PES4T4.

Chapter 9, "Configuration Registers," discusses the base addresses, PCI configuration space, and registers associated with the PES4T4.

Chapter 10, "JTAG Boundary Scan," discusses an enhanced JTAG interface, including a system logic TAP controller, signal definitions, a test data register, an instruction register, and usage considerations.

Signal Nomenclature

To avoid confusion when dealing with a mixture of "active-low" and "active-high" signals, the terms assertion and negation are used. The term assert or assertion is used to indicate that a signal is active or true, independent of whether that level is represented by a high or low voltage. The term negate or negation is used to indicate that a signal is inactive or false.

To define the active polarity of a signal, a suffix will be used. Signals ending with an 'N' should be interpreted as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses and select lines) will be interpreted as being active, or asserted when at a logic one (high) level.

Notes

To define buses, the most significant bit (MSB) will be on the left and least significant bit (LSB) will be on the right. No leading zeros will be included.

Throughout this manual, when describing signal transitions, the following terminology is used. Rising edge indicates a low-to-high (0 to 1) transition. Falling edge indicates a high-to-low (1 to 0) transition. These terms are illustrated in Figure 1.

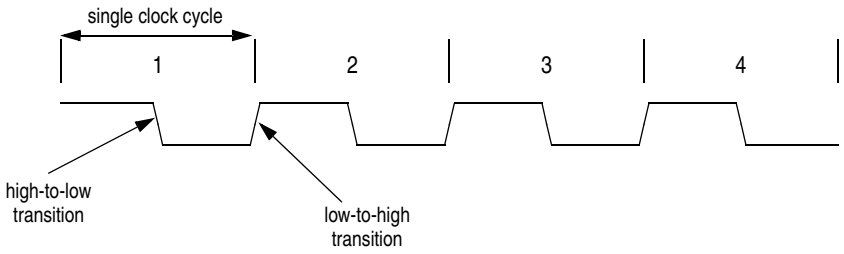

Figure 1 Signal Transitions

Numeric Representations

To represent numerical values, either decimal, binary, or hexadecimal formats will be used. The binary format is as follows: 0bDDD, where "D" represents either 0 or 1; the hexadecimal format is as follows: 0xDD, where "D" represents the hexadecimal digit(s); otherwise, it is decimal.

The compressed notation ABC[x|y|z]D refers to ABCxD, ABCyD, and ABCzD.

The compressed notation ABC[x:y]D refers to ABCxD, ABC(x+1)D, ABC(x+2)D,... ABCyD if x < y or to ABCxD, ABC(x-1)D, ABC(x-2)D,... ABCyD if x > y.

Data Units

The following data unit terminology is used in this document.

Term	Words	Bytes	Bits
Byte	1/2	1	8
Word	1	2	16
Doubleword (Dword)	2	4	32
Quadword (Qword)	4	8	64

Table 1 Data Unit Terminology

In quadwords, bit 63 is always the most significant bit and bit 0 is the least significant bit. In double-words, bit 31 is always the most significant bit and bit 0 is the least significant bit. In words, bit 15 is always the most significant bit and bit 0 is the least significant bit. In bytes, bit 7 is always the most significant bit and bit 0 is the least significant bit.

The ordering of bytes within words is referred to as either "big endian" or "little endian." Big endian systems label byte zero as the most significant (leftmost) byte of a word. Little endian systems label byte zero as the least significant (rightmost) byte of a word.

Notes

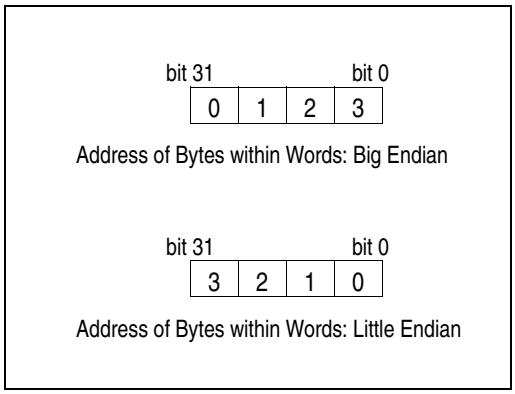

Table 2 Example of Byte Ordering for "Big Endian" or "Little Endian" System Definition

Register Terminology

Note: Software in the context of this register terminology refers to modifications made by PCIe root configuration writes to registers made through the serial EEPROM register initialization.

Type	Abbreviation	Description
Hardware Initialized	HWINIT	Register bits are initialized by firmware or hardware mechanisms such as pin strapping or serial EEPROM. (System firmware hardware initialization is only allowed for system integrated devices.) Bits are read-only after initialization and can only be reset (for write-once by firmware) with reset.
Read Only and Clear	RC	Software can read the register/bits with this attribute. Reading the value will automatically cause the register/bit to be reset to zero. Writing to a RC location has no effect.
Read Clear and Write	RCW	Software can read the register/bits with this attribute. Reading the value will automatically cause the register/bits to be reset to zero. Writes cause the register/bits to be modified.
Reserved	Reserved	The value read from a reserved register/bit is undefined. Thus, software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back.
Read Only	RO	Software can only read registers/bits with this attribute. Contents are hardwired to a constant value or are status bits that may be set and cleared by hardware. Writing to a RO location has no effect.
Read and Write	RW	Software can both read and write bits with this attribute.
Read and Write Clear	RW1C	Software can read and write to registers/bits with this attribute. However, writing a value of zero to a bit with this attribute has no effect. A RW1C bit can only be set to a value of 1 by a hardware event. To clear a RW1C bit (i.e., change its value to zero) a value of one must be written to the location. An RW1C bit is never cleared by hardware.

Table 3 Register Terminology (Sheet 1 of 2)

Notes

Type	Abbreviation	Description
Read and Write when Unlocked	RWL	Software can read the register/bits with this attribute. Writing to register/bits with this attribute will only cause the value to be modified if the REGUNLOCK bit in the SWCNTL register is set. When the REGUNLOCK bit is cleared, writes are ignored and the register/bits are effectively read-only. These registers are Sticky as they are preserved across a hot reset. These bits are not preserved during fundamental reset.
Read Only Sticky	ROS	Registers are read-only and cannot be altered by software. Registers are not initialized or modified by hot reset. When device consumes AUX power, some of these bits maintain their value across fundamental reset and are marked FRSticky.
Read and Write Sticky	RWS	Registers are read-write and may be either set or cleared by software to the desired state. Bits are not initialized or modified by hot reset. When device consumes AUX power, some of these bits maintain their value across fundamental reset and are marked FRSticky.
Read Write-1-to-Clear Sticky	RWICS	Registers indicate status when read, a set bit indicating a status event may be cleared by writing a 1. Writing a 0 to RW1CS bits has no effect. Bits are not initialized or modified by hot reset. When device consumes AUX power, some of these bits maintain their value across fundamental reset and are marked FRSticky.
Write Transient	WT	The zero is always read from a bit/field of this type. Writing of a one is used to qualify the writing of other bits/fields in the same register.
Zero	Zero	A zero register or bit must be written with a value of zero and returns a value of zero when read.

Table 3 Register Terminology (Sheet 2 of 2)

Use of Hypertext

In Chapter 9, Tables 9.2 and 9.3 contain register names and page numbers highlighted in blue under the Register Definition column. In pdf files, users can jump from this source table directly to the registers by clicking on the register name in the source table. Each register name in the table is linked directly to the appropriate register in the register section of the chapter. To return to the source table after having jumped to the register section, click on the same register name (in blue) in the register section.

Reference Documents

PCI Express Base Specification, Revision 1.1, PCI Special Interest Group.

PCI Power Management Interface Specification, Revision 1.2, PCI Special Interest Group.

PCI to PCI Bridge Architecture Specification, Revision 1.2, PCI Special Interest Group.

SMBus Specification, Revision 2.0.

Revision History

June 20, 2007: Initial Publication.

July 11, 2007: Corrected AERUCS to AERUES in AERCTL register, Chapter 8.

Notes

July 16, 2007: Made numerous minor edits throughout manual. Removed all references to slave SMBus.

June 6, 2008: In Chapter 1, updated the Features section to include 10x10mm 132-pin package option.

September 23, 2009: In Chapter 5, SMBus, added Note in I/O Expander section re setting of GPIOFUNC[4:2] bits. Made numerous changes in Chapter 6, Power.

September 24, 2009: In Chapter 3, change made to L2 description in Link States section. In Chapter 5, SMBus, added Note in I/O Expander section re setting of GPIOFUNC[4:2] bits. Made numerous changes in Chapter 6, Power. In Chapter 8, Registers, modified description of the LDIS bit in the PCI Express Link Control register and changed bit field for CTLPTOC in the Switch Time-Out Count register to [24:16].

November 10, 2009: Added a new Chapter 3 called Theory of Operations.

February 1, 2011: ZB silicon added to Table 1.9, Revision ID.

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PES4T4 Device Overview

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Introduction

The 89HPES4T4 is a member of IDT's PRECISE™ family of PCI Express switching solutions. The PES4T4 is a 4-lane, 4-port peripheral chip that performs PCI Express Base switching. It provides connectivity and switching functions between a PCI Express upstream port and up to four downstream ports and supports switching between downstream ports.

List of Features

- **High Performance PCI Express Switch**
  - *Four 2.5 Gbps PCI Express lanes*
  - *Four switch ports*
  - *x1 Upstream port*
  - *Three x1 Downstream ports*
  - *Low latency cut-through switch architecture*
  - *Support for Max payload sizes up to 256 bytes*
  - *One virtual channel*
  - *Eight traffic classes*
  - *PCI Express Base Specification Revision 1.1 compliant*
- **Flexible Architecture with Numerous Configuration Options**
  - *Automatic lane reversal on all ports*
  - *Automatic polarity inversion on all lanes*
  - *Ability to load device configuration from serial EEPROM*
- **Legacy Support**
  - *PCI compatible INTx emulation*
  - *Bus locking*
- **Highly Integrated Solution**
  - *Requires no external components*
  - *Incorporates on-chip internal memory for packet buffering and queueing*
  - *Integrates four 2.5 Gbps embedded SerDes with 8B/10B encoder/decoder (no separate transceivers needed)*
- **Reliability, Availability, and Serviceability (RAS) Features**
  - *Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)*
  - *Supports ECRC and Advanced Error Reporting*
  - *Supports PCI Express Native Hot-Plug, Hot-Swap capable I/O*
  - *Compatible with Hot-Plug I/O expanders used on PC motherboards*
- **Power Management**
  - *Utilizes advanced low-power design techniques to achieve low typical power consumption*
  - *Supports PCI Power Management Interface specification (PCI-PM 1.2)*
  - *Unused SerDes are disabled.*
  - *Supports Advanced Configuration and Power Interface Specification, Revision 2.0 (ACPI) supporting active link state*
- **Testability and Debug Features**
  - *Built in Pseudo-Random Bit Stream (PRBS) generator*
  - *Numerous SerDes test modes*
  - *Ability to bypass link training and force any link into any mode*
  - *Provides statistics and performance counters*

Notes

- **5 General Purpose Input/Output Pins**
  - *Each pin may be individually configured as an input or output*
  - *Each pin may be individually configured as an interrupt input*
  - *Each pin has a selectable alternate function*
- **Option A Package: 13mm x 13mm 144-ball BGA with 1mm ball spacing**
- **Option B Package: 10mm x 10mm 132-ball QFN with 1mm ball spacing**

System Diagrams

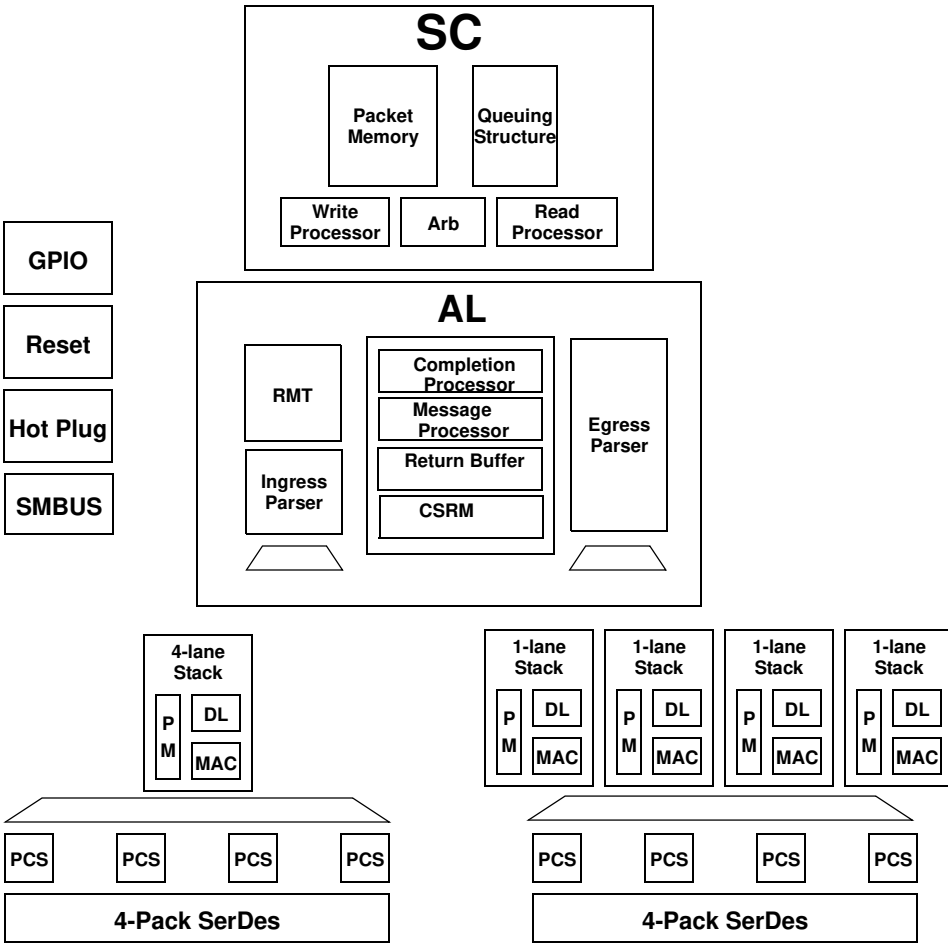

Figure 1.1 PES4T4 Architectural Block Diagram

Logic Diagram

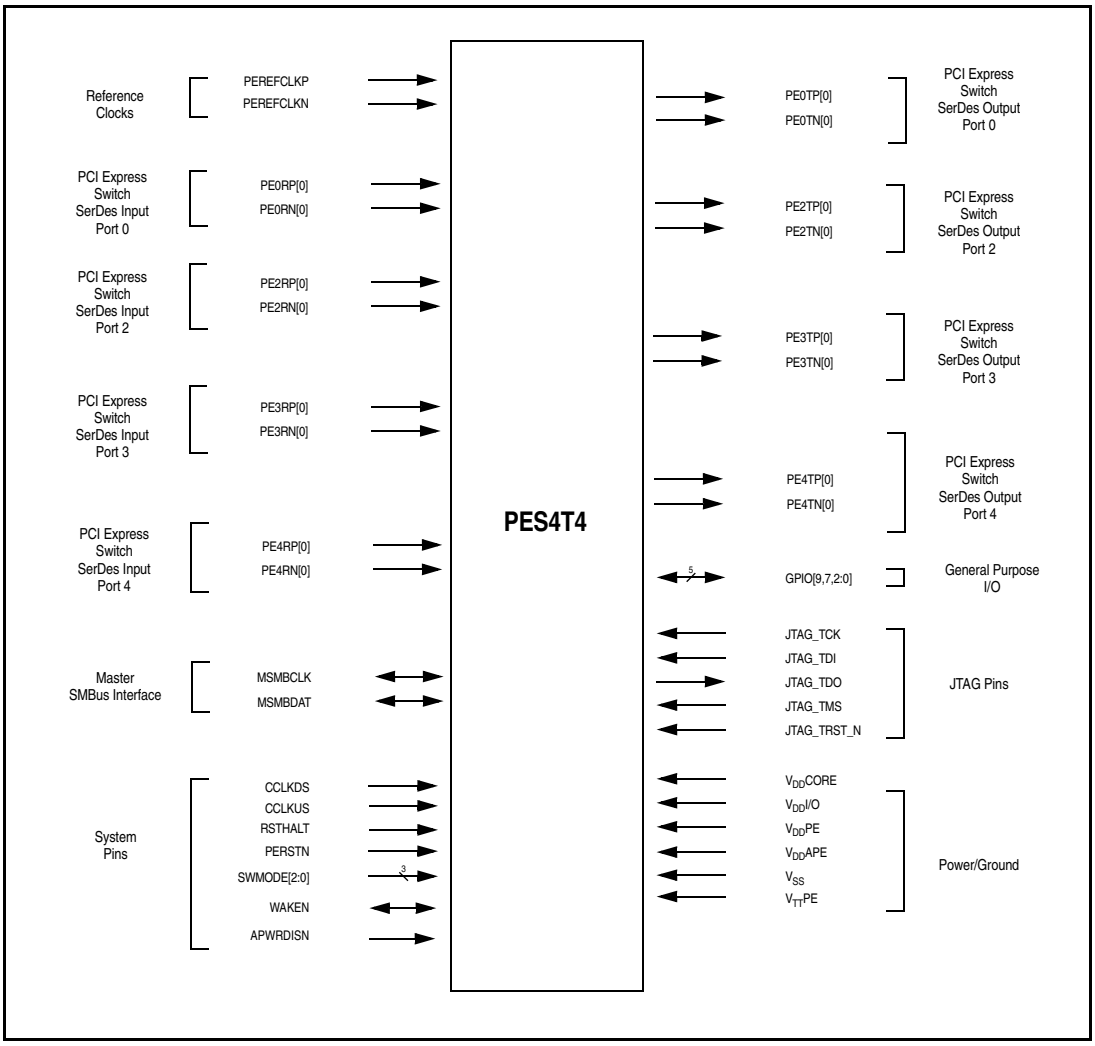

Figure 1.2 PES4T4 Logic Diagram

SSID/SSVID

The PES4T4 contains the mechanisms necessary to implement the PCI-to-PCI bridge Subsystem ID and Subsystem Vendor ID capability structure. However, in the default configuration the Subsystem ID and Subsystem Vendor ID capability structure is not enabled. To enable this capability, the SSID and SSVID fields in the Subsystem ID and Subsystem Vendor ID (SSIDSSVID) register must be initialized with the appropriate ID values. the Next Pointer (NXTPTR) field in one of the other enhanced capabilities should be initialized to point to this capability. Finally, the Next Pointer (NXTPTR) of this capability should be adjusted to point to the next capability if necessary.

Device Serial Number Enhanced Capability

The PES4T4 contains the mechanisms necessary to implement the PCI express device serial number enhanced capability. However, in the default configuration this capability structure is not enabled. To enable the device serial number enhanced capability, the Serial Number Lower Doubleword (SNUMLDW) and the Serial Number Upper Doubleword (SNUMUDW) registers should be initialized. The Next Pointer (NXTPTR) field in one of the other enhanced capabilities should be initialized to point to this capability. Finally, the Next Pointer (NXTPTR) of this capability should be adjusted to point to the next capability if necessary.

Notes

Pin Description

The following tables lists the functions of the pins provided on the PES4T4. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an "N" are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Signal	Type	Name/Description
PE0RP[0] PE0RN[0]	I	**PCI Express Port 0 Serial Data Receive.** Differential PCI Express receive pair for port 0.
PE0TP[0] PE0TN[0]	O	**PCI Express Port 0 Serial Data Transmit.** Differential PCI Express transmit pair for port 0.
PE2RP[0] PE2RN[0]	I	**PCI Express Port 2 Serial Data Receive.** Differential PCI Express receive pair for port 2.
PE2TP[0] PE2TN[0]	O	**PCI Express Port 2 Serial Data Transmit.** Differential PCI Express transmit pair for port 2.
PE3RP[0] PE3RN[0]	I	**PCI Express Port 3 Serial Data Receive.** Differential PCI Express receive pair for port 3.
PE3TP[0] PE3TN[0]	O	**PCI Express Port 3 Serial Data Transmit.** Differential PCI Express transmit pair for port 3.
PE4RP[0] PE4RN[0]	I	**PCI Express Port 4 Serial Data Receive.** Differential PCI Express receive pair for port 4.
PE4TP[0] PE4TN[0]	O	**PCI Express Port 4 Serial Data Transmit.** Differential PCI Express transmit pair for port 4.
PEREFCLKP PEREFCLKN	I	**PCI Express Reference Clock.** Differential reference clock pair input. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic and on-chip SerDes.

Table 1.1 PCI Express Interface Pins

Signal	Type	Name/Description
MSMBCLK	I/O	**Master SMBus Clock.** This bidirectional signal is used to synchronize transfers on the master SMBus.
MSMBDAT	I/O	**Master SMBus Data.** This bidirectional signal is used for data on the master SMBus.

Table 1.2 SMBus Interface Pins

Notes

Signal	Type	Name/Description
GPIO[0]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P2RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 2
GPIO[1]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P4RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 4
GPIO[2]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN0 Alternate function pin type: Input Alternate function: I/O Expander interrupt 0 input
GPIO[7]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: GPEN Alternate function pin type: Output Alternate function: General Purpose Event (GPE) output
GPIO[9]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P3RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 3

Table 1.3 General Purpose I/O Pins

Signal	Type	Name/Description
APWRDISN	I	**Auxiliary Power Disable Input.** When this pin is active, it disables the device from using auxiliary power supply.
CCLKDS	I	**Common Clock Downstream.** The assertion of this pin indicates that all downstream ports are using the same clock source as that provided to downstream devices.This bit is used as the initial value of the Slot Clock Configuration bit in all of the Link Status Registers for downstream ports. The value may be override by modifying the SCLK bit in the downstream port's PCIELSTS register.
CCLKUS	I	**Common Clock Upstream.** The assertion of this pin indicates that the upstream port is using the same clock source as the upstream device. This bit is used as the initial value of the Slot Clock Configuration bit in the Link Status Register for the upstream port. The value may be overridden by modifying the SCLK bit in the PA_PCIELSTS register.
PERSTN	I	**Fundamental Reset.** Assertion of this signal resets all logic inside the PES4T4 and initiates a PCI Express fundamental reset.

Table 1.4 System Pins (Part 1 of 2)