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Device Overview

The 89HPES22H16G2 is a member of the IDT PRECISE™ family of PCI Express® switching solutions. The PES22H16G2 is a 22-lane, 16-port system interconnect switch optimized for PCI Express Gen2 packet switching in high-performance applications, supporting multiple simultaneous peer-to-peer traffic flows. It provides connectivity and switching functions between a PCI Express upstream port and up to fifteen downstream ports and supports switching between downstream ports.

Features

◆ High Performance Non-Blocking Switch Architecture

- Sixteen maximum switch ports
 - *Two x4 ports*
 - *Fourteen x1 ports*
- Integrated SerDes supports 5.0 GT/s Gen2 and 2.5 GT/s Gen1 operation
- Delivers 22 GBps (176 Gbps) of aggregate switching capacity
- Supports up to 128 Bytes to 2 KB maximum payload size
- Low latency cut-through architecture
- Supports one virtual channel and eight traffic classes

◆ Standards and Compatibility

- PCI Express Base Specification 2.0 compliant
- Implements the following optional PCI Express features
 - *Advanced Error Reporting (AER) on all ports*
 - *End-to-End CRC (ECRC)*
 - *Access Control Services (ACS)*
 - *Power Budgeting Enhanced Capability*
 - *Device Serial Number Enhanced Capability*
 - *Sub-System ID and Sub-System Vendor ID Capability*
 - *Internal Error Reporting ECN*
 - *Multicast ECN*
 - *VGA and ISA enable*
 - *L0s and L1 ASPM*
 - *ARI ECN*

◆ Port Configurability

- x4, x2, and x1 ports
 - *Ability to merge adjacent x4 ports to create a x8 port*
- Automatic per port link width negotiation (x4 → x2 → x1)
- Crosslink support
- Automatic lane reversal
- Autonomous and software managed link width and speed control
- Per lane SerDes configuration
 - *De-emphasis*
 - *Receive equalization*

- *Drive strength*

◆ Switch Partitioning

- IDT proprietary feature that creates logically independent switches in the device
- Supports up to 16 fully independent switch partitions
- Configurable downstream port device numbering
- Supports dynamic reconfiguration of switch partitions
 - *Dynamic port reconfiguration — downstream, upstream*
 - *Dynamic migration of ports between partitions*
 - *Movable upstream port within and between switch partitions*

◆ Initialization / Configuration

- Supports Root (BIOS, OS, or driver), Serial EEPROM, or SMBus switch initialization
- Common switch configurations are supported with pin strapping (no external components)
- Supports in-system Serial EEPROM initialization/programming

◆ Quality of Service (QoS)

- Port arbitration
 - *Round robin*
- Request metering
 - *IDT proprietary feature that balances bandwidth among switch ports for maximum system throughput*
- High performance switch core architecture
 - *Combined Input Output Queued (CIOQ) switch architecture with large buffers*

◆ Multicast

- Compliant to the PCI-SIG multicast ECN
- Supports arbitrary multicasting of Posted transactions
- Supports 64 multicast groups
- Multicast overlay mechanism support
- ECRC regeneration support

◆ Clocking

- Supports 100 MHz and 125 MHz reference clock frequencies
- Flexible port clocking modes
 - *Common clock*
 - *Non-common clock*
 - *Local port clock with SSC and port reference clock input*

◆ Hot-Plug and Hot Swap

- Hot-plug controller on all ports
 - *Hot-plug supported on all downstream switch ports*
- All ports support hot-plug using low-cost external I²C I/O expanders
- Configurable presence detect supports card and cable applications

- GPE output pin for hot-plug event notification
 - *Enables SCI/SMI generation for legacy operating system support*
- Hot swap capable I/O
- ◆ **Power Management**
 - Supports D0, D3hot and D3 power management states
 - Active State Power Management (ASPM)
 - *Supports L0, L0s, L1, L2/L3 Ready and L3 link states*
 - *Configurable L0s and L1 entry timers allow performance/power-savings tuning*
 - Supports PCI Express Power Budgeting Capability
 - SerDes power savings
 - *Supports low swing / half-swing SerDes operation*
 - *SerDes optionally turned-off in D3hot*
 - *SerDes associated with unused ports are turned-off*
 - *SerDes associated with unused lanes are placed in a low power state*
- ◆ **54 General Purpose I/O**
- ◆ **Reliability, Availability and Serviceability (RAS)**
 - ECRC support
 - AER on all ports
 - SECCDED ECC protection on all internal RAMs
 - End-to-end data path parity protection
 - Checksum Serial EEPROM content protected
 - Autonomous link reliability (preserves system operation in the presence of faulty links)
 - Ability to generate an interrupt (INTx or MSI) on link up/down transitions
- ◆ **Test and Debug**
 - On-chip link activity and status outputs available for Port 0 (upstream port)
 - Per port link activity and status outputs available using external I²C I/O expander for all other ports
 - SerDes test modes
 - Supports IEEE 1149.6 AC JTAG and IEEE 1149.1 JTAG
- ◆ **Power Supplies**
 - Requires only two power supply voltages (1.0 V and 2.5 V). Note that a 3.3V is preferred for V_{DD}I/O
 - No power sequencing requirements
- ◆ **Packaged in a 35mm x 35mm 1156-ball Flip Chip BGA with 1mm ball spacing**

Product Description

Utilizing standard PCI Express interconnect, the PES22H16G2 provides the most efficient I/O connectivity for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides 176 Gbps of aggregated, full-duplex switching capacity through 22 integrated serial lanes, using proven and robust IDT technology. Each lane provides 5 GT/s of bandwidth in both directions and is fully compliant with PCI Express Base Specification, Revision 2.0.

The PES22H16G2 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 2.0. The PES22H16G2 can operate either as a store and forward switch. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to enable efficient switching and I/O connectivity.

The PES22H16G2 is a *partitionable* PCIe switch. This means that in addition to operating as a standard PCI express switch, the PES22H16G2 ports may be partitioned into groups that logically operate as completely independent PCIe switches. Figure 2 illustrates a three partition PES22H16G2 configuration.

Block Diagram

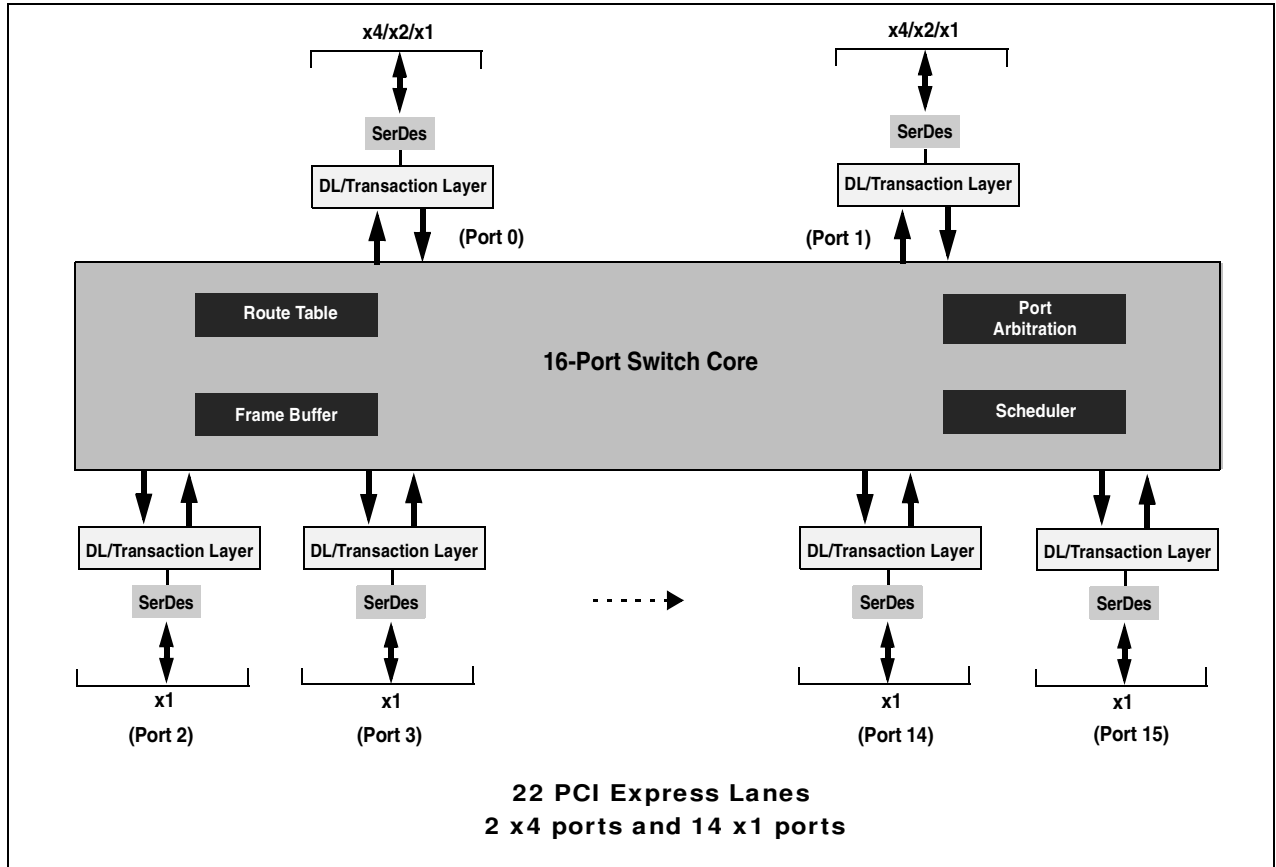


Figure 1 Internal Block Diagram

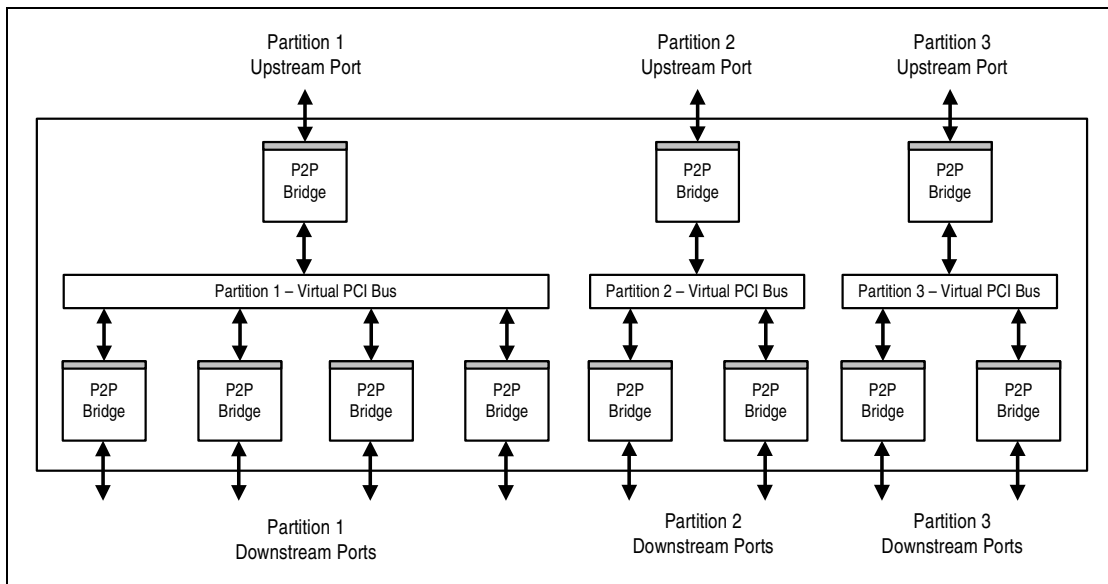


Figure 2 Example of Usage of Switch Partitioning

SMBus Interface

The PES22H16G2 contains two SMBus interfaces. The slave interface provides full access to the configuration registers in the PES22H16G2, allowing every configuration register in the device to be read or written by an external agent. The master interface allows the default configuration register values of the PES22H16G2 to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander.

Each of the two SMBus interfaces contain an SMBus clock pin and an SMBus data pin. In addition, the slave SMBus has SSMBADDR1 and SSMBADDR2 pins. As shown in Figure 3, the master and slave SMBuses may only be used in a split configuration.

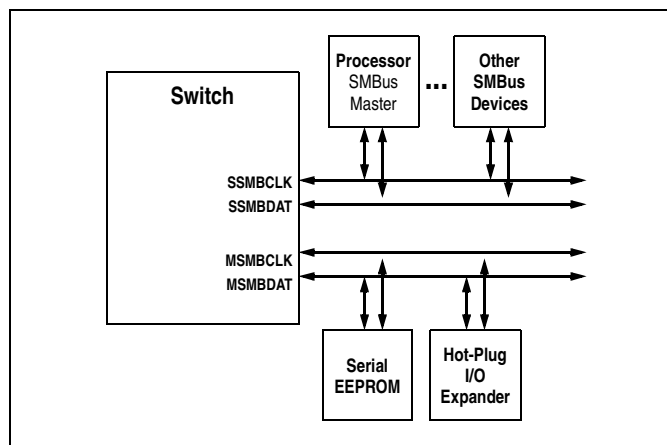


Figure 3 Split SMBus Interface Configuration

The switch's SMBus master interface does not support SMBus arbitration. As a result, the switch's SMBus master must be the only master in the SMBus lines that connect to the serial EEPROM and I/O expander slaves. In the split configuration, the master and slave SMBuses operate as two independent buses; thus, multi-master arbitration is not required.

Hot-Plug Interface

The PES22H16G2 supports PCI Express Hot-Plug on each downstream port (ports 1 through 15). To reduce the number of pins required on the device, the PES22H16G2 utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES22H16G2 generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES22H16G2. In response to an I/O expander interrupt, the PES22H16G2 generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

General Purpose Input/Output

The PES22H16G2 provides 54 General Purpose I/O (GPIO) pins that may be individually configured as general purpose inputs, general purpose outputs, or alternate functions. Some GPIO pins are shared with other on-chip functions. These alternate functions may be enabled via software, SMBus slave interface, or serial configuration EEPROM.

Pin Description

The following tables list the functions of the pins provided on the PES22H16G2. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an "N" are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level. Differential signals end with a suffix "N" or "P." The differential signal ending in "P" is the positive portion of the differential pair and the differential signal ending in "N" is the negative portion of the differential pair.

Signal	Type	Name/Description
PE00RP[3:0] PE00RN[3:0]	I	PCI Express Port 0 Serial Data Receive. Differential PCI Express receive pairs for port 0.
PE00TP[3:0] PE00TN[3:0]	O	PCI Express Port 0 Serial Data Transmit. Differential PCI Express transmit pairs for port 0.
PE01RP[3:0] PE01RN[3:0]	I	PCI Express Port 1 Serial Data Receive. Differential PCI Express receive pairs for port 1. When port 0 is merged with port 1, these signals become port 0 receive pairs for lanes 4 through 7.
PE01TP[3:0] PE01TN[3:0]	O	PCI Express Port 1 Serial Data Transmit. Differential PCI Express transmit pairs for port 1. When port 0 is merged with port 1, these signals become port 0 transmit pairs for lanes 4 through 7.
PE02RP[0] PE02RN[0]	I	PCI Express Port 2 Serial Data Receive. Differential PCI Express receive pair for port 2.
PE02TP[0] PE02TN[0]	O	PCI Express Port 2 Serial Data Transmit. Differential PCI Express transmit pair for port 2.
PE03RP[0] PE03RN[0]	I	PCI Express Port 3 Serial Data Receive. Differential PCI Express receive pair for port 3.
PE03TP[0] PE03TN[0]	O	PCI Express Port 3 Serial Data Transmit. Differential PCI Express transmit pair for port 3.
PE04RP[0] PE04RN[0]	I	PCI Express Port 4 Serial Data Receive. Differential PCI Express receive pair for port 4.
PE04TP[0] PE04TN[0]	O	PCI Express Port 4 Serial Data Transmit. Differential PCI Express transmit pair for port 4.
PE05RP[0] PE05RN[0]	I	PCI Express Port 5 Serial Data Receive. Differential PCI Express receive pair for port 5.
PE05TP[0] PE05TN[0]	O	PCI Express Port 5 Serial Data Transmit. Differential PCI Express transmit pair for port 5.
PE06RP[0] PE06RN[0]	I	PCI Express Port 6 Serial Data Receive. Differential PCI Express receive pair for port 6.
PE06TP[0] PE06TN[0]	O	PCI Express Port 6 Serial Data Transmit. Differential PCI Express transmit pair for port 6.
PE07RP[0] PE07RN[0]	I	PCI Express Port 7 Serial Data Receive. Differential PCI Express receive pair for port 7.
PE07TP[0] PE07TN[0]	O	PCI Express Port 7 Serial Data Transmit. Differential PCI Express transmit pair for port 7.
PE08RP[0] PE08RN[0]	I	PCI Express Port 8 Serial Data Receive. Differential PCI Express receive pair for port 8.
PE08TP[0] PE08TN[0]	O	PCI Express Port 8 Serial Data Transmit. Differential PCI Express transmit pair for port 8.
PE09RP[0] PE09RN[0]	I	PCI Express Port 9 Serial Data Receive. Differential PCI Express receive pair for port 9.
PE09TP[0] PE09TN[0]	O	PCI Express Port 9 Serial Data Transmit. Differential PCI Express transmit pair for port 9.
PE10RP[0] PE10RN[0]	I	PCI Express Port 10 Serial Data Receive. Differential PCI Express receive pair for port 10.

Table 1 PCI Express Interface Pins (Part 1 of 2)

Signal	Type	Name/Description
PE10TP[0] PE10TN[0]	O	PCI Express Port 10 Serial Data Transmit. Differential PCI Express transmit pair for port 10.
PE11RP[0] PE11RN[0]	I	PCI Express Port 11 Serial Data Receive. Differential PCI Express receive pair for port 11.
PE11TP[0] PE11TN[0]	O	PCI Express Port 11 Serial Data Transmit. Differential PCI Express transmit pair for port 11.
PE12RP[0] PE12RN[0]	I	PCI Express Port 12 Serial Data Receive. Differential PCI Express receive pair for port 12.
PE12TP[0] PE12TN[0]	O	PCI Express Port 12 Serial Data Transmit. Differential PCI Express transmit pair for port 12.
PE13RP[0] PE13RN[0]	I	PCI Express Port 13 Serial Data Receive. Differential PCI Express receive pair for port 13.
PE13TP[0] PE13TN[0]	O	PCI Express Port 13 Serial Data Transmit. Differential PCI Express transmit pair for port 13. W
PE14RP[0] PE14RN[0]	I	PCI Express Port 14 Serial Data Receive. Differential PCI Express receive pair for port 14.
PE14TP[0] PE14TN[0]	O	PCI Express Port 14 Serial Data Transmit. Differential PCI Express transmit pair for port 14.
PE15RP[0] PE15RN[0]	I	PCI Express Port 15 Serial Data Receive. Differential PCI Express receive pair for port 15.
PE15TP[0] PE15TN[0]	O	PCI Express Port 15 Serial Data Transmit. Differential PCI Express transmit pair for port 15.

Table 1 PCI Express Interface Pins (Part 2 of 2)

Signal	Type	Name/Description
GCLKN[1:0] GCLKP[1:0]	I	Global Reference Clock. Differential reference clock input pair. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic. The frequency of the differential reference clock is determined by the GCLKFSEL signal.
P[15:0]CLKN P[15:0]CLKP	I	Port Reference Clock. Differential reference clock pair associated with ports 0 through 15. ¹

Table 2 Reference Clock Pins

¹. Unused port clock pins should be connected to Vss on the board.

Signal	Type	Name/Description
MSMBADDR[4:1]	I	Master SMBus Address. These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded.
MSMBCLK	I/O	Master SMBus Clock. This bidirectional signal is used to synchronize transfers on the master SMBus. It is active and generating the clock only when the EEPROM or I/O Expanders are being accessed.
MSMBDAT	I/O	Master SMBus Data. This bidirectional signal is used for data on the master SMBus.

Table 3 SMBus Interface Pins (Part 1 of 2)

Signal	Type	Name/Description
SSMBADDR[5,3:1]	I	Slave SMBus Address. These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	Slave SMBus Clock. This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	Slave SMBus Data. This bidirectional signal is used for data on the slave SMBus.

Table 3 SMBus Interface Pins (Part 2 of 2)

Signal	Type	Name/Description
GPIO[0]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART0PERSTN Alternate function pin type: Input Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[1]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART1PERSTN Alternate function pin type: Input Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[2]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART2PERSTN Alternate function pin type: Input Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[3]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART3PERSTN Alternate function pin type: Input Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[4]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function — Reserved 2nd Alternate function pin name: P0LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 0 Link Up Status output.
GPIO[5]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: GPEN 1st Alternate function pin type: Output 1st Alternate function: Hot-plug general purpose even output. 2nd Alternate function pin name: P0ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 0 Link Active Status Output.
GPIO[6]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[7]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.

Table 4 General Purpose I/O Pins (Part 1 of 8)

Signal	Type	Name/Description
GPIO[8]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN Alternate function pin type: Input Alternate function: IO expander interrupt.
GPIO[9]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0APN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 0 Attention Push Button Input.
GPIO[10]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0PDN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 0 Presence Detect Input.
GPIO[11]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0PFN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 0 Power Fault Input.
GPIO[12]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0PWRGDN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 0 Power Good Input.
GPIO[13]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0MRLN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 0 Manually Operated Retention Latch Input.
GPIO[14]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0AIN Alternate function pin type: Output Alternate function: Hot Plug Signal Group 0 Attention Indicator Output.
GPIO[15]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0PIN Alternate function pin type: Output Alternate function: Hot Plug Signal Group 0 Power Indicator Output.
GPIO[16]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0PEP Alternate function pin type: Output Alternate function: Hot Plug Signal Group 0 Power Enable Output.
GPIO[17]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0RSTN Alternate function pin type: Output Alternate function: Hot Plug Signal Group 0 Reset Output.
GPIO[18]	I/O	General Purpose I/O. Alternate function pin name: HP1APN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 1 Attention Push Button Input.

Table 4 General Purpose I/O Pins (Part 2 of 8)

Signal	Type	Name/Description
GPIO[19]	I/O	General Purpose I/O. Alternate function pin name: HP1PDN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 1 Presence Detect Input.
GPIO[20]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP1PFN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 1 Power Fault Input.
GPIO[21]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP1PWRGDN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 1 Power Enable Input.
GPIO[22]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP1MRLN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 1 Manually Operated Retention Latch Input. 2nd Alternate function pin name: P1LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 1 Link Up Status Output.
GPIO[23]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP1AIN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 1 Attention Indicator Output. 2nd Alternate function pin name: P1ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 1 Link Active Status Output.
GPIO[24]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP1PIN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 1 Power Indicator Output. 2nd Alternate function pin name: P2LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 2 Link Up Status Output.
GPIO[25]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP1PEP 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 1 Power Enable Output. 2nd Alternate function pin name: P2ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 2 Link Active Status Output.
GPIO[26]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP1RSTN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 1 Reset Output. 2nd Alternate function pin name: P3LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 3 Link Up Status Output.

Table 4 General Purpose I/O Pins (Part 3 of 8)

Signal	Type	Name/Description
GPIO[27]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2APN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 2 Attention Push Button Input. 2nd Alternate function pin name: P3ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 3 Link Active Status Output.
GPIO[28]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2PDN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 2 Presence Detect Input. 2nd Alternate function pin name: P4LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 4 Link Up Status Output.
GPIO[29]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2PFN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 2 Power Fault Input. 2nd Alternate function pin name: P4ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 4 Link Active Status Output.
GPIO[30]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2PWRGDN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 2 Power Good Input. 2nd Alternate function pin name: P5LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 5 Link Up Status Output.
GPIO[31]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2MRLN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 2 Manually Operated Retention Latch Input. 2nd Alternate function pin name: P5ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 5 Link Active Status Output.
GPIO[32]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2AIN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 2 Attention Indicator Output. 2nd Alternate function pin name: P6LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 6 Link Up Status Output.

Table 4 General Purpose I/O Pins (Part 4 of 8)

Signal	Type	Name/Description
GPIO[33]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2PIN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 2 Power Indicator Output. 2nd Alternate function pin name: P6ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 6 Link Active Status Output.
GPIO[34]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2PEP 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 2 Power Enable Output. 2nd Alternate function pin name: P7LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 7 Link Up Status Output.
GPIO[35]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2RSTN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 2 Reset Output. 2nd Alternate function pin name: P7ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 7 Link Active Status Output.
GPIO[36]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP3APN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 3 Attention Push Button Input. 2nd Alternate function pin name: P8LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 8 Link Up Status Output.
GPIO[37]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP3PDN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 3 Presence Detect Input. 2nd Alternate function pin name: P8ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 8 Link Active Status Output.
GPIO[38]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP3PFN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 3 Power Fault Input. 2nd Alternate function pin name: P9LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 9 Link Up Status Output.
GPIO[39]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP3PWRGDN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 3 Power Good Input. 2nd Alternate function pin name: P9ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 9 Link Active Status Output.

Table 4 General Purpose I/O Pins (Part 5 of 8)

Signal	Type	Name/Description
GPIO[40]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP3MRLN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 3 Manually Operated Retention Latch Input. 2nd Alternate function pin name: P10LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 10 Link Up Status Output.
GPIO[41]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP3AIN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 3 Attention Indicator Output. 2nd Alternate function pin name: P10ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 10 Link Active Status Output.
GPIO[42]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP3PIN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 3 Power Indicator Output. 2nd Alternate function pin name: P11LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 11 Link Up Status Output.
GPIO[43]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP3PEP 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 3 Power Enable Output. 2nd Alternate function pin name: P11ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 11 Link Active Status Output.
GPIO[44]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP3RSTN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 3 Reset Output. 2nd Alternate function pin name: P12LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 12 Link Up Status Output.
GPIO[45]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP4APN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 4 Attention Push Button Input. 2nd Alternate function pin name: P12ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 12 Link Active Status Output.

Table 4 General Purpose I/O Pins (Part 6 of 8)

Signal	Type	Name/Description
GPIO[46]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP4PDN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 4 Presence Detect Input. 2nd Alternate function pin name: P13LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 13 Link Up Status Output.
GPIO[47]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP4PFN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 4 Power Fault Input. 2nd Alternate function pin name: P13ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 13 Link Active Status Output.
GPIO[48]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP4PWRGDN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 4 Power Good Input. 2nd Alternate function pin name: P14LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 14 Link Up Status Output.
GPIO[49]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP4MRLN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 4 Manually Operated Retention Latch Input. 2nd Alternate function pin name: P14ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 14 Link Active Status Output.
GPIO[50]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP4AIN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 4 Attention Indicator Output. 2nd Alternate function pin name: P15LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 15 Link Up Status Output.

Table 4 General Purpose I/O Pins (Part 7 of 8)

Signal	Type	Name/Description
GPIO[51]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP4PIN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 4 Power Indicator Output. 2nd Alternate function pin name: P15ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 15 Link Active Status Output.
GPIO[52]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP4PEP Alternate function pin type: Output Alternate function: Hot Plug Signal Group 4 Power Enable Output.
GPIO[53]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP4RSTN Alternate function pin type: Output Alternate function: Hot Plug Signal Group 4 Reset Output.

Table 4 General Purpose I/O Pins (Part 8 of 8)

Signal	Type	Name/Description
CLKMODE[2:0]		Clock Mode. These signals determine the port clocking mode used by ports of the device.
GCLKFSEL	I	Global Clock Frequency Select. These signals select the frequency of the GCLKP and GCLKN signals. 0x0 100 MHz 0x1 125 MHz
MSMBSMODE	I	Master SMBus Slow Mode. The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 KHz. This value may not be overridden.
P01MERGEN	I	Port 0 and 1 Merge. P01MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 0 is merged with port 1 to form a single x8 port. The Serdes lanes associated with port 1 become lanes 4 through 7 of port 0. When this pin is high, port 0 and port 1 are not merged, and each operates as a single x4 port.
PERSTN	I	Global Reset. Assertion of this signal resets all logic inside PES22H16G2.
RSTHALT	I	Reset Halt. When this signal is asserted during a PCI Express fundamental reset, PES22H16G2 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the SWCTL register by an SMBus master.

Table 5 System Pins (Part 1 of 2)

Signal	Type	Name/Description
SWMODE[3:0]	I	<p>Switch Mode. These configuration pins determine the PES22H16G2 switch operating mode. Note: These pins should be static and not change following the negation of PERSTN.</p> <p>0x0 - Single partition 0x1 - Single partition with Serial EEPROM initialization 0x2 through 0x7 - Reserved 0x8 - Single partition with port 0 selected as the upstream port (port 2 disabled) 0x9 - Single partition with port 2 selected as the upstream port (port 0 disabled) 0xA - Single partition with Serial EEPROM initialization and port 0 selected as the upstream port (port 2 disabled) 0xB - Single partition with Serial EEPROM initialization and port 2 selected as the upstream port (port 0 disabled) 0xC - Multi-partition 0xD - Multi-partition with Serial EEPROM initialization 0xE - Reserved 0xF - Reserved</p>

Table 5 System Pins (Part 2 of 2)

Signal	Type	Name/Description
JTAG_TCK	I	JTAG Clock. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	JTAG Data Input. This is the serial data input to the boundary scan logic or JTAG Controller.
JTAG_TDO	O	JTAG Data Output. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	JTAG Mode. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	<p>JTAG Reset. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur:</p> <ol style="list-style-type: none"> 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 6 Test Pins

Signal	Type	Name/Description
REFRES00	I/O	External Reference Resistor. Provides a reference for the SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES01	I/O	External Reference Resistor. Provides a reference for the SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES02	I/O	External Reference Resistor. Provides a reference for the SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.

Table 7 Power, Ground, and SerDes Resistor Pins (Part 1 of 3)

Signal	Type	Name/Description
REFRES03	I/O	External Reference Resistor. Provides a reference for the SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES04	I/O	External Reference Resistor. Provides a reference for the SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES05	I/O	External Reference Resistor. Provides a reference for the SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES06	I/O	External Reference Resistor. Provides a reference for the SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES07	I/O	External Reference Resistor. Provides a reference for the SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES08	I/O	Port 8 External Reference Resistor. Provides a reference for the Port 8 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES09	I/O	Port 9 External Reference Resistor. Provides a reference for the Port 9 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES10	I/O	Port 10 External Reference Resistor. Provides a reference for the Port 10 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES11	I/O	Port 11 External Reference Resistor. Provides a reference for the Port 11 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES12	I/O	Port 12 External Reference Resistor. Provides a reference for the Port 12 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES13	I/O	Port 13 External Reference Resistor. Provides a reference for the Port 13 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES14	I/O	Port 14 External Reference Resistor. Provides a reference for the Port 14 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES15	I/O	Port 15 External Reference Resistor. Provides a reference for the Port 15 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRESPLL	I/O	PLL External Reference Resistor. Provides a reference for the PLL bias currents and PLL calibration circuitry. A 3K Ohm +/- 1% resistor should be connected from this pin to ground.
V _{DD} CORE	I	Core V_{DD}. Power supply for core logic (1.0V).
V _{DD} I/O	I	I/O V_{DD}. LVTTTL I/O buffer power supply (2.5V or preferred 3.3V).
V _{DD} PEA	I	PCI Express Analog Power. Serdes analog power supply (1.0V).

Table 7 Power, Ground, and SerDes Resistor Pins (Part 2 of 3)

Signal	Type	Name/Description
V _{DD} PEHA	I	PCI Express Analog High Power. Serdes analog power supply (2.5V).
V _{DD} PETA	I	PCI Express Transmitter Analog Voltage. Serdes transmitter analog power supply (1.0V).
V _{SS}	I	Ground.

Table 7 Power, Ground, and SerDes Resistor Pins (Part 3 of 3)

Pin Characteristics

Note: Some input pads of the switch do not contain internal pull-ups or pull-downs. Unused SMBus and System inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, floating pins can cause a slight increase in power consumption. Unused Serdes (Rx and Tx) pins should be left floating. Finally, No Connection pins should not be connected.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor ¹	Notes
PCI Express Interface	PE00RN[3:0]	I	PCIe differential ²	Serial Link		
	PE00RP[3:0]	I				
	PE00TN[3:0]	O				
	PE00TP[3:0]	O				
	PE01RN[3:0]	I				
	PE01RP[3:0]	I				
	PE01TN[3:0]	O				
	PE01TP[3:0]	O				
	PE02RN[0]	I				
	PE02RP[0]	I				
	PE02TN[0]	O				
	PE02TP[0]	O				
	PE03RN[0]	I				
	PE03RP[0]	I				
	PE03TN[0]	O				
	PE03TP[0]	O				
	PE04RN[0]	I				
	PE04RP[0]	I				
	PE04TN[0]	O				
	PE04TP[0]	O				
	PE05RN[0]	I				
	PE05RP[0]	I				
	PE05TN[0]	O				
	PE05TP[0]	O				
	PE06RN[0]	I				
	PE06RP[0]	I				
	PE06TN[0]	O				
	PE06TP[0]	O				
	PE07RN[0]	I				
	PE07RP[0]	I				
	PE07TN[0]	O				
	PE07TP[0]	O				
PE08RN[0]	I					

Table 8 Pin Characteristics (Part 1 of 3)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor ¹	Notes
PCI Express Interface (cont.)	PE08RP[0]	I	PCIe differential	Serial Link		
	PE08TN[0]	O				
	PE08TP[0]	O				
	PE09RN[0]	I				
	PE09RP[0]	I				
	PE09TN[0]	O				
	PE09TP[0]	O				
	PE10RN[0]	I				
	PE10RP[0]	I				
	PE10TN[0]	O				
	PE10TP[0]	O				
	PE11RN[0]	I				
	PE11RP[0]	I				
	PE11TN[0]	O				
	PE11TP[0]	O				
	PE12RN[0]	I				
	PE12RP[0]	I				
	PE12TN[0]	O				
	PE12TP[0]	O				
	PE13RN[0]	I				
	PE13RP[0]	I				
	PE13TN[0]	O				
	PE13TP[0]	O				
	PE14RN[0]	I				
	PE14RP[0]	I				
	PE14TN[0]	O				
	PE14TP[0]	O				
	PE15RN[0]	I				
	PE15RP[0]	I				
	PE15TN[0]	O				
	PE15TP[0]	O				
		GCLKN[1:0]			I	HCSL
	GCLKP[1:0]	I				
	P[15:0]CLKN	I				
	P[15:0]CLKP	I				

Table 8 Pin Characteristics (Part 2 of 3)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor ¹	Notes
SMBus	MSMBADDR[4:1]	I	LVTTTL	Input	pull-down	
	MSMBCLK	I/O		STI ³		
	MSMBDAT	I/O		STI		
	SSMBADDR[5,3:1]	I		Input	pull-up	
	SSMBCLK	I/O		STI		
	SSMBDAT	I/O		STI		
General Purpose I/O	GPIO[53:0]	I/O	LVTTTL		pull-up	
System Pins	CLKMODE[1:0]	I	LVTTTL	Input	pull-up	
	CLKMODE[2]	I			pull-down	
	GCLKFSEL	I			pull-down	
	MSMBSMODE	I			pull-down	
	P01MERGEN	I			pull-down	
	PERSTN	I		STI		
	RSTHALT	I		Input	pull-down	
	SWMODE[3:0]	I			pull-down	
EJTAG / JTAG	JTAG_TCK	I	LVTTTL	STI	pull-up	
	JTAG_TDI	I		STI	pull-up	
	JTAG_TDO	O				
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I		STI	pull-up	External pull-down
SerDes Reference Resistors	REFRES[15:0]	I/O	Analog			
	REFRESPLL	I/O				

Table 8 Pin Characteristics (Part 3 of 3)

¹. Internal resistor values under typical operating conditions are 92K Ω for pull-up and 91K Ω for pull-down.

². All receiver pins set the DC common mode voltage to ground. All transmitters must be AC coupled to the media.

³. Schmitt Trigger Input (STI).

Logic Diagram — PES22H16G2

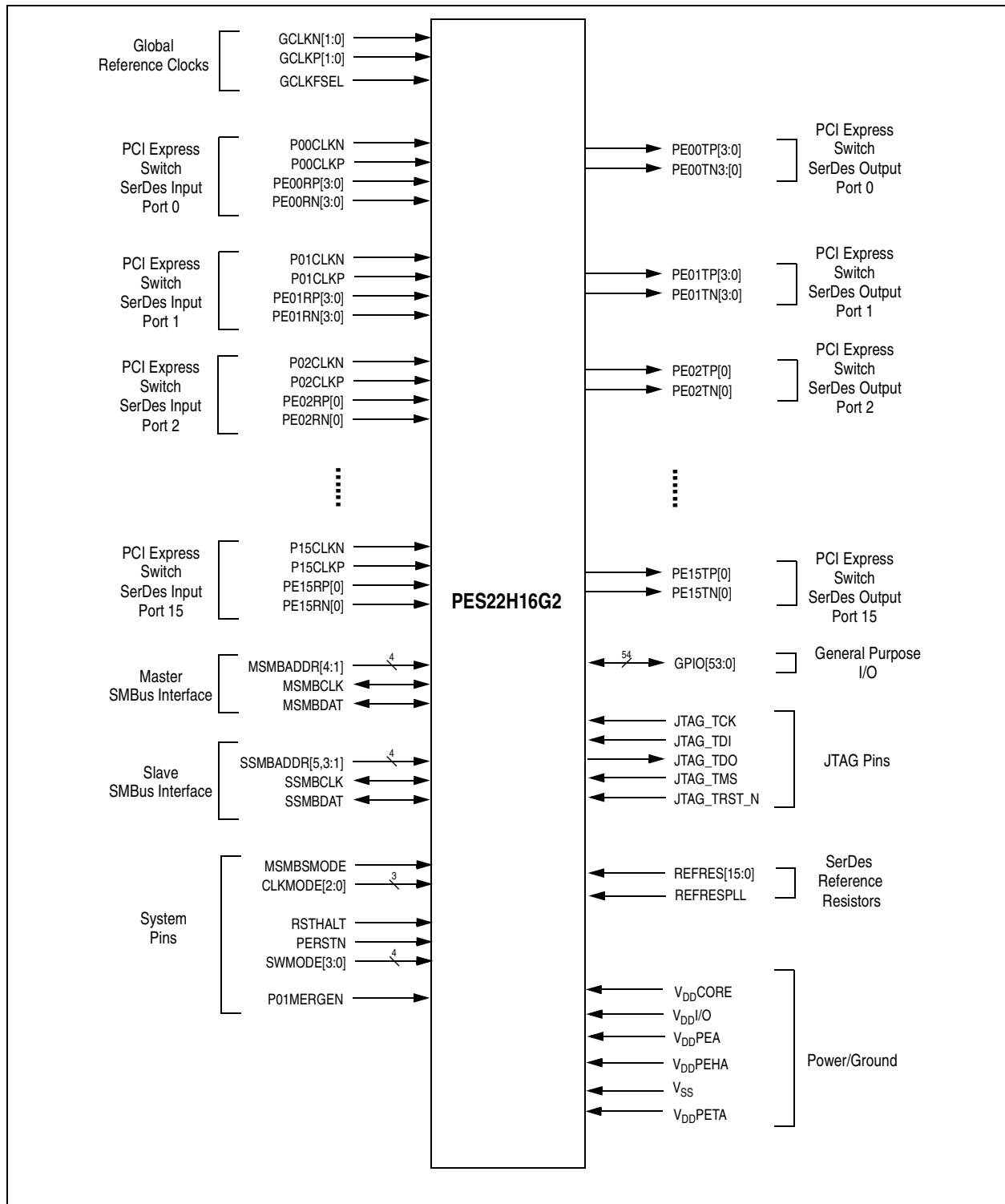


Figure 4 PES22H16G2 Logic Diagram

System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 13 and 14.

Parameter	Description	Condition	Min	Typical	Max	Unit
Refclk _{FREQ}	Input reference clock frequency range		100		125 ¹	MHz
T _{C-RISE}	Rising edge rate	Differential	0.6		4	V/ns
T _{C-FALL}	Falling edge rate	Differential	0.6		4	V/ns
V _{IH}	Differential input high voltage	Differential	+150			mV
V _{IL}	Differential input low voltage	Differential			-150	mV
V _{CROSS}	Absolute single-ended crossing point voltage	Single-ended	+250		+550	mV
V _{CROSS-DELTA}	Variation of V _{CROSS} over all rising clock edges	Single-ended			+140	mV
V _{RB}	Ring back voltage margin	Differential	-100		+100	mV
T _{STABLE}	Time before V _{RB} is allowed	Differential	500			ps
T _{PERIOD-AVG}	Average clock period accuracy		-300		2800	ppm
T _{PERIOD-ABS}	Absolute period, including spread-spectrum and jitter		9.847		10.203	ns
T _{CC-JITTER}	Cycle to cycle jitter				150	ps
V _{MAX}	Absolute maximum input voltage				+1.15	V
V _{MIN}	Absolute minimum input voltage		-0.3			V
Duty Cycle	Duty cycle		40		60	%
Rise/Fall Matching	Single ended rising Refclk edge rate versus falling Refclk edge rate			20		%
Z _{C-DC}	Clock source output DC impedance		40		60	Ω

Table 9 Input Clock Requirements

¹The input clock frequency will be either 100 or 125 MHz depending on signal GCLKFSEL.

AC Timing Characteristics

Parameter	Description	Gen 1			Gen 2			Units
		Min ¹	Typ ¹	Max ¹	Min ¹	Typ ¹	Max ¹	
PCIe Transmit								
UI	Unit Interval	399.88	400	400.12	199.94	200	200.06	ps
T _{TX-EYE}	Minimum Tx Eye Width	0.75			0.75			UI
T _{TX-EYE-MEDIAN-to-MAX-JITTER}	Maximum time between the jitter median and maximum deviation from the median			0.125				UI
T _{TX-RISE} ; T _{TX-FALL}	TX Rise/Fall Time: 20% - 80%	0.125			0.15			UI
T _{TX-IDLE-MIN}	Minimum time in idle	20			20			UI
T _{TX-IDLE-SET-TO-IDLE}	Maximum time to transition to a valid Idle after sending an Idle ordered set			8			8	ns

Table 10 PCIe AC Timing Characteristics (Part 1 of 2)

Parameter	Description	Gen 1			Gen 2			Units
		Min ¹	Typ ¹	Max ¹	Min ¹	Typ ¹	Max ¹	
T _{TX-IDLE-TO-DIFF-DATA}	Maximum time to transition from valid idle to diff data			8			8	ns
T _{TX-SKEW}	Transmitter data skew between any 2 lanes			1.3			1.3	ns
T _{MIN-PULSED}	Minimum Instantaneous Lone Pulse Width	NA			0.9			UI
T _{TX-HF-DJ-DD}	Transmitter Deterministic Jitter > 1.5MHz Bandwidth	NA					0.15	UI
T _{RF-MISMATCH}	Rise/Fall Time Differential Mismatch	NA					0.1	UI
PCIe Receive								
UI	Unit Interval	399.88	400	400.12	199.94		200.06	ps
T _{RX-EYE (with jitter)}	Minimum Receiver Eye Width (jitter tolerance)	0.4			0.4			UI
T _{RX-EYE-MEDIUM TO MAX JITTER}	Max time between jitter median & max deviation			0.3				UI
T _{RX-SKEW}	Lane to lane input skew			20			8	ns
T _{RX-HF-RMS}	1.5 — 100 MHz RMS jitter (common clock)	NA					3.4	ps
T _{RX-HF-DJ-DD}	Maximum tolerable DJ by the receiver (common clock)	NA					88	ps
T _{RX-LF-RMS}	10 KHz to 1.5 MHz RMS jitter (common clock)	NA					4.2	ps
T _{RX-MIN-PULSE}	Minimum receiver instantaneous eye width	NA			0.6			UI

Table 10 PCIe AC Timing Characteristics (Part 2 of 2)

¹. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 2.0

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[53:0] ¹	Tpw_13b ²	None	50	—	ns	See Figure 5.

Table 11 GPIO AC Timing Characteristics

¹. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

². The values for this symbol were determined by calculation, not by testing.

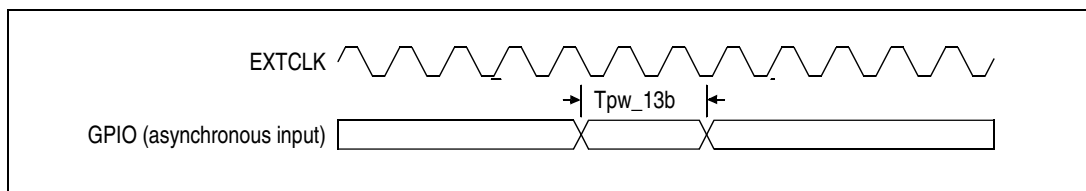


Figure 5 GPIO AC Timing Waveform

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	50.0	—	ns	See Figure 6.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS ¹ , JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	20	ns	
	Tdz_16c ²		—	20	ns	
JTAG_TRST_N	Tpw_16d ²	none	25.0	—	ns	

Table 12 JTAG AC Timing Characteristics

¹ The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

² The values for this symbol were determined by calculation, not by testing.

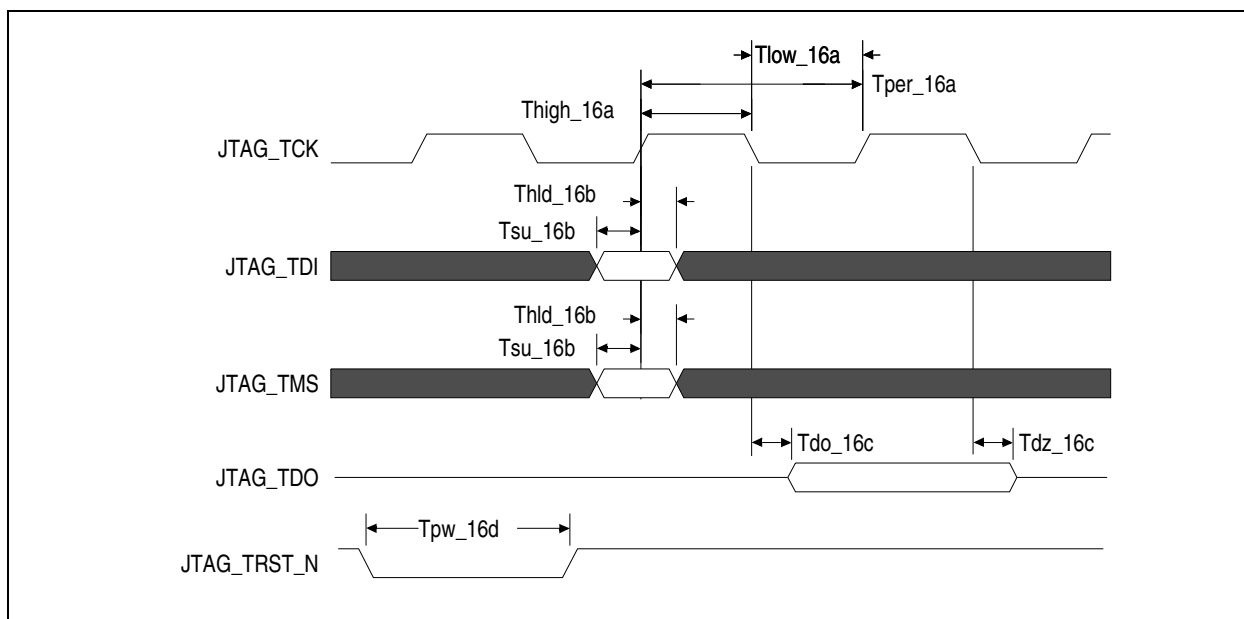


Figure 6 JTAG AC Timing Waveform

Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V _{DD} CORE	Internal logic supply	0.9	1.0	1.1	V
V _{DD} I/O	I/O supply except for SerDes	2.25	2.5	2.75	V
		3.125	3.3	3.465	V
V _{DD} PEA ¹	PCI Express Analog Power	0.95	1.0	1.1	V
V _{DD} PEHA ²	PCI Express Analog High Power	2.25	2.5	2.75	V
V _{DD} PETA ¹	PCI Express Transmitter Analog Voltage	0.95	1.0	1.1	V
V _{SS}	Common ground	0	0	0	V

Table 13 PES22H16G2 Operating Voltages

¹ V_{DD}PEA and V_{DD}PETA should have no more than 25mV_{peak-peak} AC power supply noise superimposed on the 1.0V nominal DC value.

² V_{DD}PEHA should have no more than 50mV_{peak-peak} AC power supply noise superimposed on the 2.5V nominal DC value.

Power-Up Sequence

During power supply ramp-up, V_{DD}CORE must remain at least 1.0V below V_{DD}I/O at all times. There are no other power-up sequence requirements for the various operating supply voltages.

The power-down sequence can occur in any order.

Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 14 PES22H16G2 Operating Temperatures