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General Description

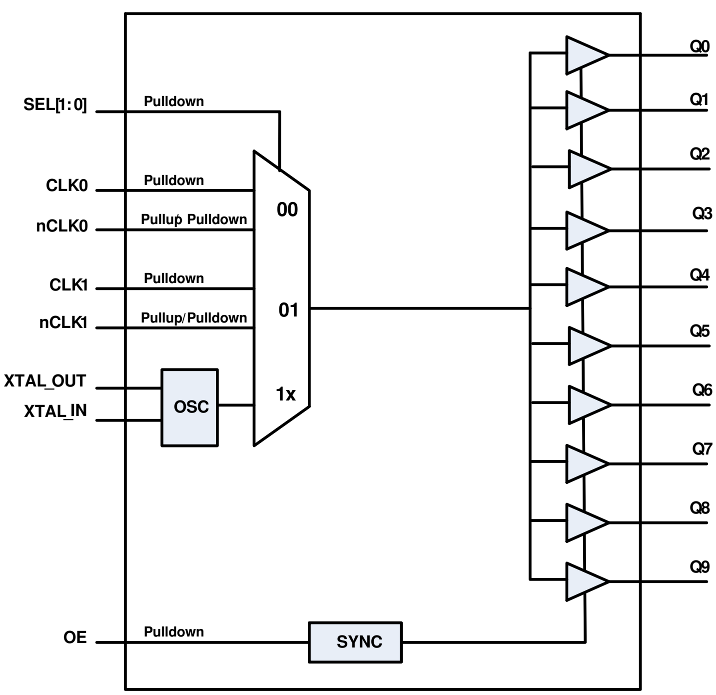
The 8L30110 is a low skew, 1-to-10 LVCMOS / LVTTL Fanout Buffer. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines.

The 8L30110 is characterized at full 3.3V and 2.5V, mixed 3.3V/2.5V, 3.3V/1.8V, 3.3V/1.5V, 2.5V/1.8V and 2.5V/1.5V output operating supply modes. The input clock is selected from two differential clock inputs or a crystal input. The differential input can be wired to accept a single-ended input. The internal oscillator circuit is automatically disabled if the crystal input is not selected.

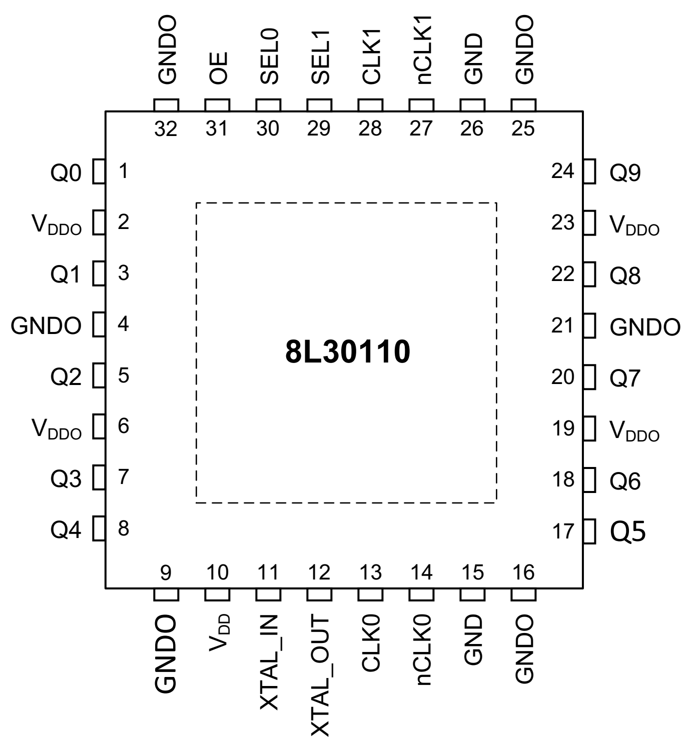
Features

- Ten LVCMOS / LVTTL outputs up to 200MHz
- Differential input pair can accept the following differential input levels: LVPECL, LVDS, HCSL
- Crystal Oscillator Interface
- Crystal input frequency range: 8MHz to 50MHz
- Output skew: 63ps (typical)
- Additive RMS phase jitter: 22fs (typical)
- Power supply modes:
  Core / Output
  3.3V / 3.3V
  3.3V / 2.5V
  3.3V / 1.8V
  3.3V / 1.5V
  2.5V / 2.5V
  2.5V / 1.8V
  2.5V / 1.5V
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

Block Diagram



Pin Assignment



32-pin, 5mm x 5mm VFQFN Package

Pin Descriptions and Characteristics

Table 1. Pin Descriptions[1]

Number	Name	Type		Description
1	Q0	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
2	V_{DDO}	Power		Output supply.
3	Q1	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
4	GNDO	Power		Power supply output ground.
5	Q2	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
6	V_{DDO}	Power		Output supply.
7	Q3	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
8	Q4	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
9	GNDO	Power		Power supply output ground.
10	V_{DD}	Power		Power supply.
11	XTAL_IN	Input		Crystal input.
12	XTAL_OUT	Output		Crystal output.
13	CLK0	Input	Pulldown	Non-inverting differential clock.
14	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock. Internal resistor bias to $V_{DD}/2$.
15	GND	Power		Power supply core ground.
16	GNDO	Power		Power supply output ground.
17	Q5	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
18	Q6	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
19	V_{DDO}	Power		Output supply.
20	Q7	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
21	GNDO	Power		Power supply output ground.
22	Q8	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
23	V_{DDO}	Power		Output supply.
24	Q9	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
25	GNDO	Power		Power supply output ground.
26	GND	Power		Power supply core ground.
27	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock. Internal resistor bias to $V_{DD}/2$.
28	CLK1	Input	Pulldown	Non-inverting differential clock.
29	SEL1	Input	Pulldown	Input clock selection. LVCMOS/LVTTL interface levels. See Table 3A.
30	SEL0	Input	Pulldown	Input clock selection. LVCMOS/LVTTL interface levels. See Table 3A.
31	OE	Input	Pulldown	Output enable. LVCMOS/LVTTL interface levels. See Table 3B.
32	GNDO	Power		Power supply output ground.
ePad	GND_EP	Power		Exposed pad of package. Connect to ground.

NOTE 1. *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics[1]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	SEL[1:0], OE CLK0, nCLK0, CLK1, nCLK1			2		pF
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{PULLUP}	Input Pullup Resistor				51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)		V_{DDO} = 3.465V, f = 100MHz			9.5	pF
			V_{DDO} = 2.625V, f = 100MHz			7.4	pF
			V_{DDO} = 2V, f = 100MHz			7.2	pF
			V_{DDO} = 1.65V, f = 100MHz			6.9	pF
R_{OUT}	Output Impedance		V_{DDO} = 3.3V		15		Ω
			V_{DDO} = 2.5V		18		Ω
			V_{DDO} = 1.8V		25		Ω
			V_{DDO} = 1.5V		30		Ω

NOTE 1. Measured at ambient temperature (unless otherwise noted.)

Function Tables

Table 3A. SELx Function Table

Control Input	
SEL[1:0]	**Selected Input Clock**
00 (default)	CLK0, nCLK0
01	CLK1, nCLK1
11 or 10	XTAL

Table 3B. OE Function Table

Control Input	Function
OE	**Q[0:9]**
0 (default)	High-Impedance
1	Enabled

Table 3C. Input/Output Operation Table[1]

Input State	Output State
CLK0, CLK1 = HIGH nCLK0, nCLK1 = LOW	Logic HIGH
CLK0, CLK1 = LOW nCLK0, nCLK1 = HIGH	Logic LOW
CLK0, nCLK0, CLK1, nCLK1 open	Logic LOW

NOTE 1. Device must have switching edge to obtain output states.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}/V_{DDO}	3.6V
Inputs, V_I CLK_X, $nCLK_X$, XTAL_IN Other Inputs	 3.6V 2V 3.6V
Outputs, V_O	3.6V
T_J (Junction Temperature)	125°C
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics,
V_{DD} = 3.3V±5%, V_{DDO} = 3.3V±5% or 2.5V±5% or 1.8V±0.2V or 1.5V±0.15V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
			1.6	1.8	2	V
			1.35	1.5	1.65	V
I_{DD}	Static Supply Current	SEL[1:0] = 00 or 01, Outputs Unloaded		19	22	mA
		SEL[1:0] = 10 or 11, Outputs Unloaded		18	22	mA

Table 4B. Power Supply DC Characteristics,
V_{DD} = 2.5V±5%, V_{DDO} = 2.5V±5% or 1.8V±0.2V or 1.5V±0.15V,T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Current		2.375	2.5	2.625	V
			1.6	1.8	2	V
			1.35	1.5	1.65	V
I_{DD}	Static Supply Current	SEL[1:0] = 00 or 01, Outputs Unloaded		18	22	mA
		SEL[1:0] = 10 or 11, Outputs Unloaded		17	22	mA

:

Table 4C. LVCMOS/LVTTL DC Characteristics,
V_{DD} = 3.3V±5% or 2.5V±5%, V_{DDO} (≤V_{DD}) = 3.3V±5% or 2.5V±5% or 1.8V±0.2V or 1.5V±0.15V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V±5%	2			V
			V_{DD} = 2.5V±5%	1.7			V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V±5%			0.8	V
			V_{DD} = 2.5V±5%			0.7	V
I_{IH}	Input High Current	OE, SEL[1:0]	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	OE, SEL[1:0]	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage		V_{DDO} = 3.3V±5%, I_{OH} = -12mA	2.6			V
			V_{DDO} = 2.5V±5%, I_{OH} = -8mA	1.8			V
			V_{DDO} = 1.8V±0.2V, I_{OH} = -2mA	1.2			V
			V_{DDO} = 1.5V±0.15V, I_{OH} = -2mA	0.95			V
V_{OL}	Output Low Voltage		V_{DDO} = 3.3V±5%, I_{OL} = 12mA			0.5	V
			V_{DDO} = 2.5V±5%, I_{OL} = 8mA			0.5	V
			V_{DDO} = 1.8V±0.2V, I_{OL} = 2mA			0.4	V
			V_{DDO} = 1.5V±0.15V, I_{OL} = 2mA			0.35	V

Table 4D. Differential DC Characteristics,
V_{DD} = 3.3V±5% or 2.5V±5%, V_{DDO} (≤V_{DD}) = 3.3V±5% or 2.5V±5% or 1.8V±0.2V or 1.5V±0.15V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK[0:1], nCLK[0:1]	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	CLK[0:1]	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
		nCLK[0:1]	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage[1]			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage [1, 2]			0.5		V_{DD} – 0.85	V

NOTE 1. V_{IL} should not be less than -0.3V and V_{IH} should not be greater than V_{DD}.
NOTE 2. Common mode voltage is defined at the crosspoint.

Table 5. Crystal Characteristics[1]

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		8		50	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Load Capacitance (CL)			12	18	pF

NOTE 1. To insure crystal accuracy, the use of external tuning capacitors is required.

AC Electrical Characteristics

Table 6. AC Characteristics,
V_{DD} = 3.3V±5% or 2.5V±5%, V_{DDO} (≤V_{DD}) = 3.3V±5% or 2.5V±5% or 1.8V±0.2V or 1.5V±0.15V, T_A = -40°C to 85°C[1, 2]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	Using External Crystal		8		50	MHz
		Using External Clock Source				200	MHz
ΔV/ΔT	Input Edge Rate	Input Clock from CLK0, nCLK0, CLK1, nCLK1	20% – 80%		2		V/ns
t_{PD}	Propagation Delay[3]		V_{DDO} = 3.3V ± 5%	1.5		2.5	ns
			V_{DDO} = 2.5V ± 5%	1.8		2.7	ns
			V_{DDO} = 1.8V ± 0.2V	1.8		3.8	ns
			V_{DDO} = 1.5V ± 0.15V	2.5		4.6	ns
*t*sk(o)	Output Skew[4, 5]		V_{DDO} = 3.3V ± 5%		40	70	ps
			V_{DDO} = 2.5V ± 5%		45	85	ps
			V_{DDO} = 1.8V ± 0.2V		55	110	ps
			V_{DDO} = 1.5V ± 0.15V		63	120	ps
tjit	Buffer Additive Phase Jitter[6] refer to Additive Phase Jitter Section; f_{OUT} = 156.25MHz, Integration Range: 12kHz - 20MHz	Input Clock from CLK0, nCLK0 or CLK1, nCLK1	V_{DDO} = 3.3V ± 5%		22		fs
			V_{DDO} = 2.5V ± 5%		17		fs
			V_{DDO} = 1.8V ± 0.2V		55		fs
			V_{DDO} = 1.5V ± 0.15V		103		fs
NF	Noise Floor[7]	Input Clock from CLK0, nCLK0, CLK1, nCLK1 @125MHz	10kHz Offset		-129		dBC/Hz
			100kHz Offset		-142		dBC/Hz
			1MHz Offset		-158		dBC/Hz
			10MHz Offset		-160		dBC/Hz
			20MHz Offset		-160		dBC/Hz
tjit(Ø)	RMS Phase Jitter	Input Clock from Crystal 25MHz; 12kHz - 5MHz	V_{DDO} = 3.3V ± 5%		138		fs
			V_{DDO} = 2.5V ± 5%		134		fs
			V_{DDO} = 1.8V ± 0.2V		140		fs
			V_{DDO} = 1.5V ± 0.15V		157		fs
NF	Noise Floor	Input Clock from Crystal 25MHz	100Hz Offset		-113		dBC/Hz
			1kHz Offset		-143		dBC/Hz
			10kHz Offset		-157		dBC/Hz
			100kHz Offset		-162		dBC/Hz
			1MHz Offset		-163		dBC/Hz
			5MHz Offset		-163		dBC/Hz

Table 6. AC Characteristics,
V_{DD} = 3.3V±5% or 2.5V±5%, V_{DDO} (≤V_{DD}) = 3.3V±5% or 2.5V±5% or 1.8V±0.2V or 1.5V±0.15V, T_A = -40°C to 85°C[1, 2]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
t_R / t_F	Output Rise/Fall Time	V_{DDO} = 3.3V ± 5%	20% to 80%			700	ps
		V_{DDO} = 2.5V ± 5%	20% to 80%			650	ps
		V_{DDO} = 1.8V ± 0.2V	20% to 80%			605	ps
		V_{DDO} = 1.5V ± 0.15V	20% to 80%			675	ps
odc	Output Duty Cycle		50% input Duty Cycle @ 125MHz	45		55	%
t_{EN}	Output Enable Time[8]	OE			2 - 3		cycles
t_{DIS}	Output Disable Time[8]	OE			2 - 3		cycles
$MUX_{\_ISOLATION}$	MUX Isolation[8]		@ 125MHz		90		dB

NOTE 1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 2. All parameters measured at $f \leq f_{OUT}$ unless noted otherwise.

NOTE 3. Measured from the differential input crossing point to V_{DDO} /2 of the output.

NOTE 4. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO} /2.

NOTE 5. This parameter is defined in accordance with JEDEC Standard 65.

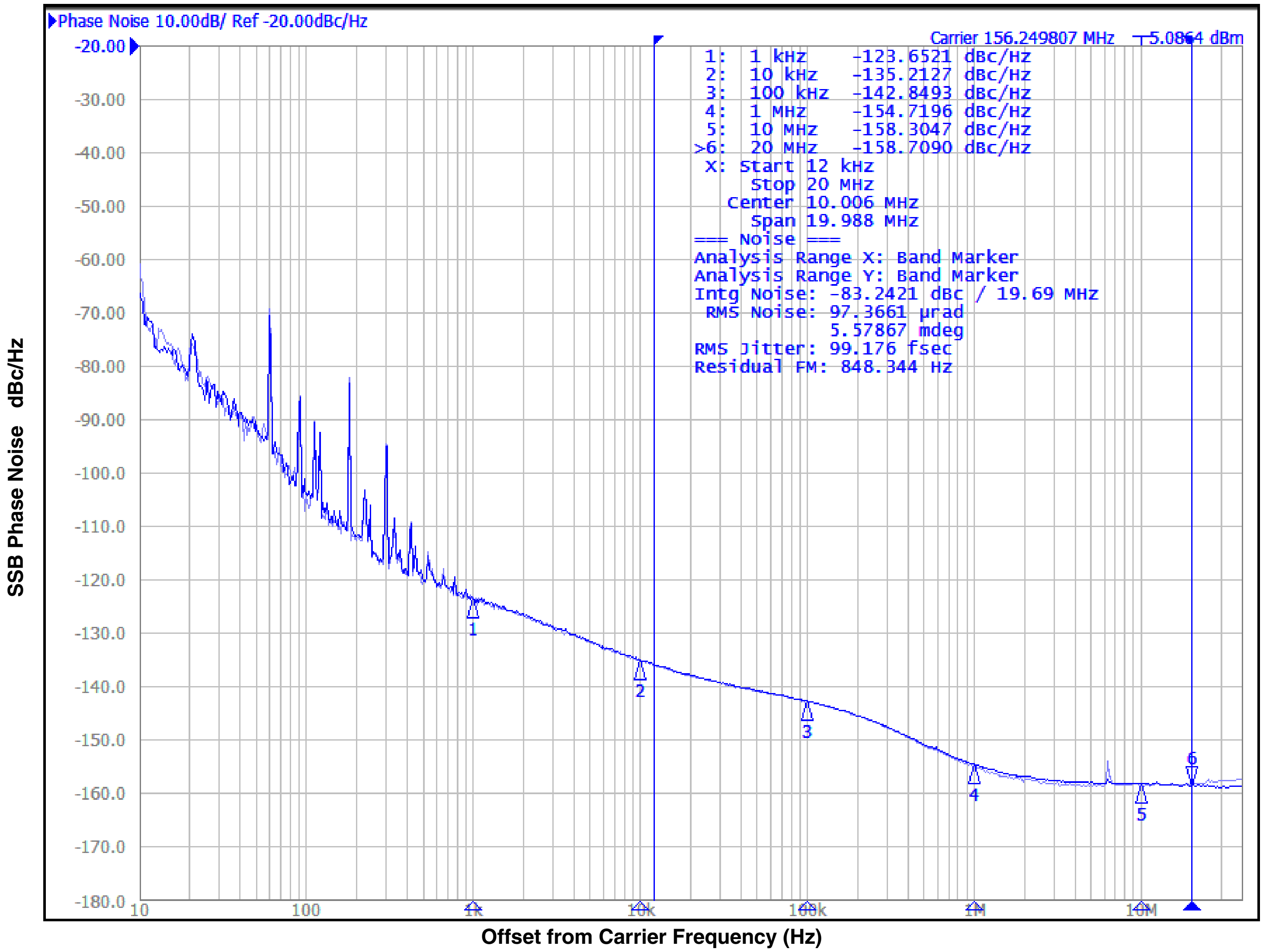
NOTE 6. Input source is IDT 8T49NS010.

NOTE 7. f_{IN} = f_{OUT} = 125MHz, V_{DD} = V_{DDO} = 3.3V.

NOTE 8. These parameters are guaranteed by characterization. Not tested in production.

Additive Phase Jitter

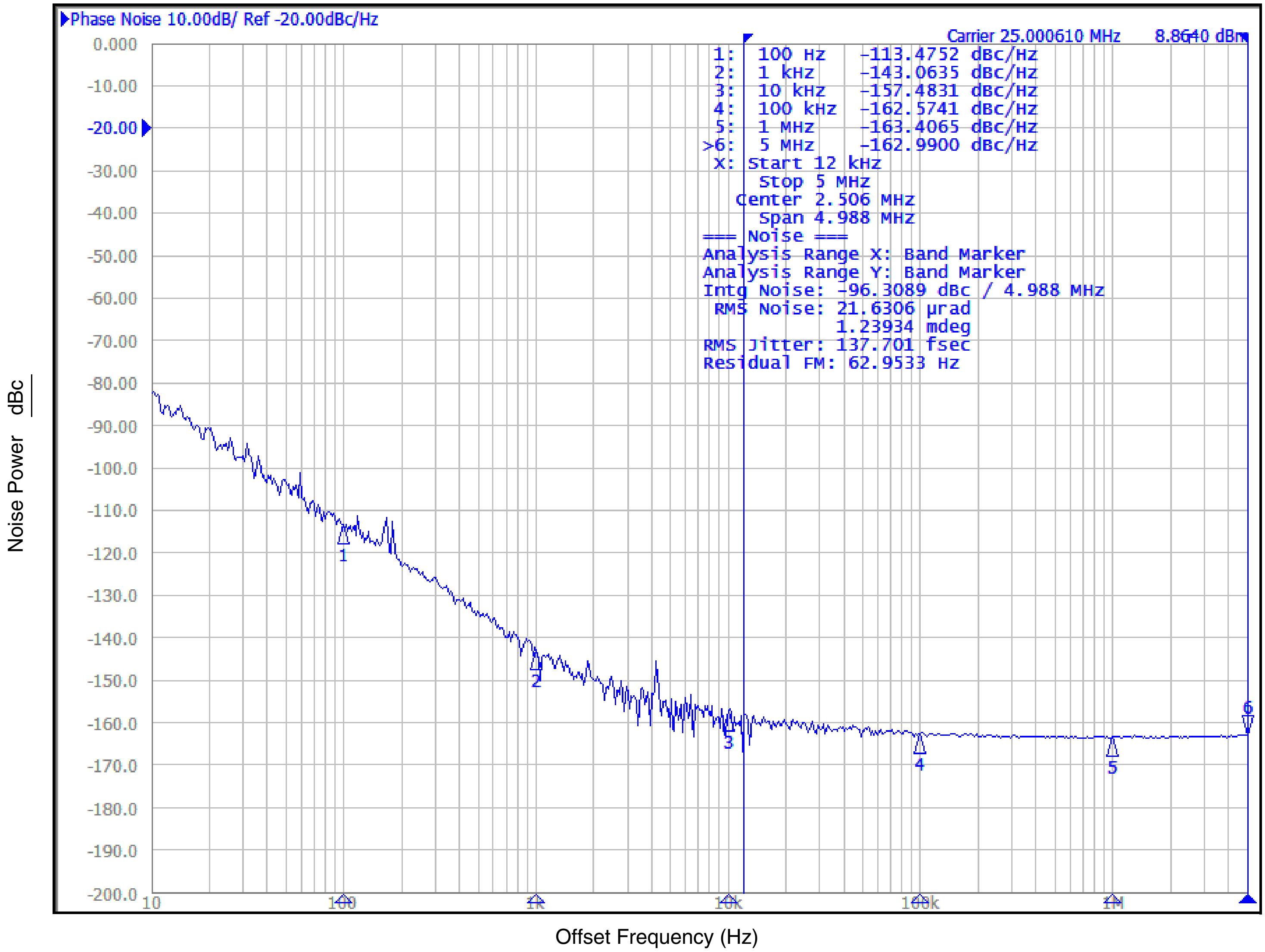
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

The additive phase jitter for this device was measured using an IDT Clock Driver 8T49NS010 as an input source and Agilent E5052 phase noise analyzer.

Typical Phase Noise at 25MHz (3.3V) with 25MHz Crystal Input



Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS outputs can be left floating We recommend that there is no trace attached.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock is driven from a single-ended 2.5V LVCMOS driver and the DC offset (or swing center) of this signal is 1.25V, the R1 and R2 values should be adjusted to set the V1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced while maintaining an edge rate faster than 1V/ns. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

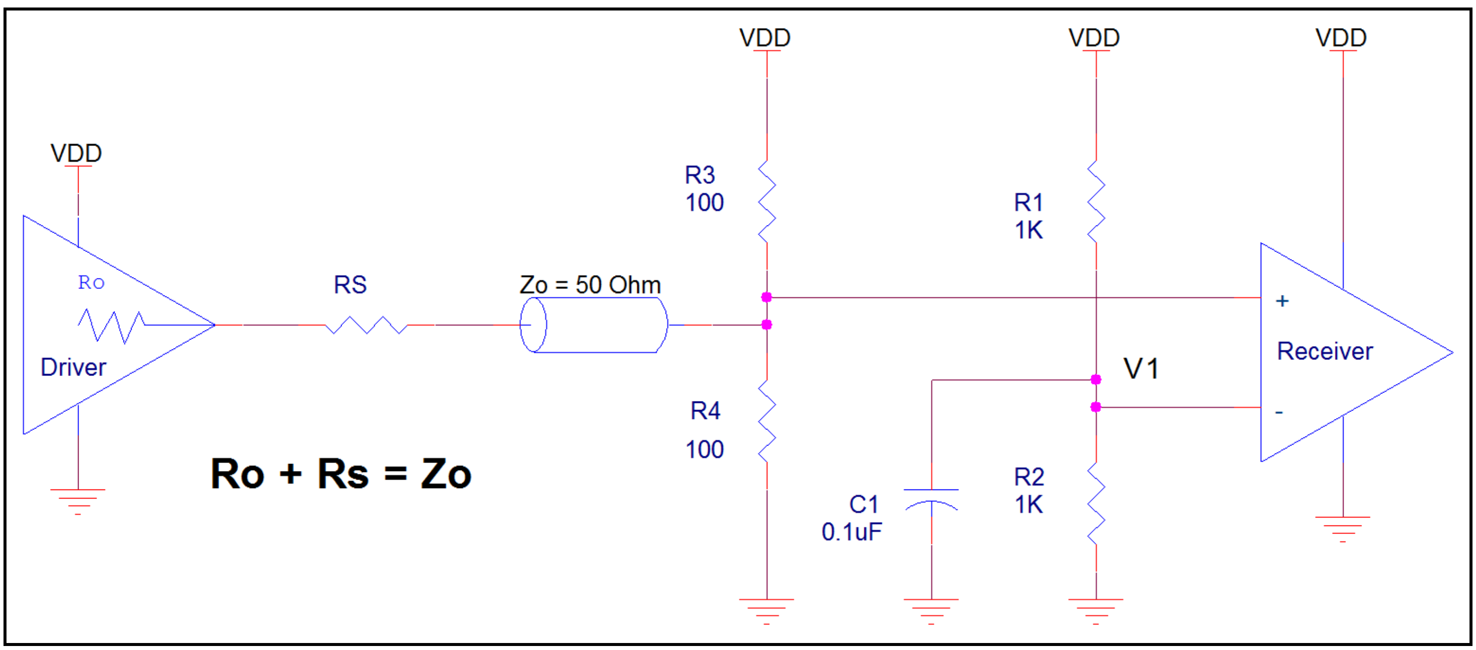


Figure 2. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Crystal Input Interface

The 8L30110 has been characterized with 12pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 3* below were determined using an 12pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

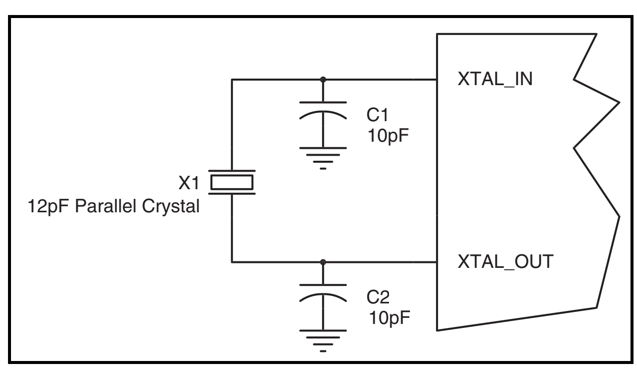


Figure 3. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 4A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 4B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

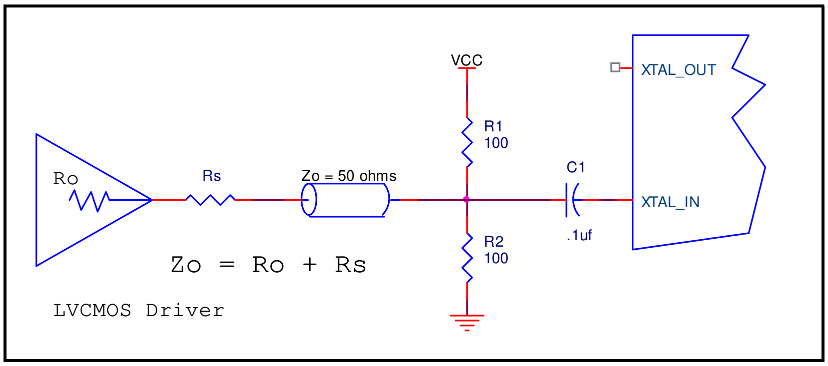


Figure 4A. General Diagram for LVCMOS Driver to XTAL Input Interface

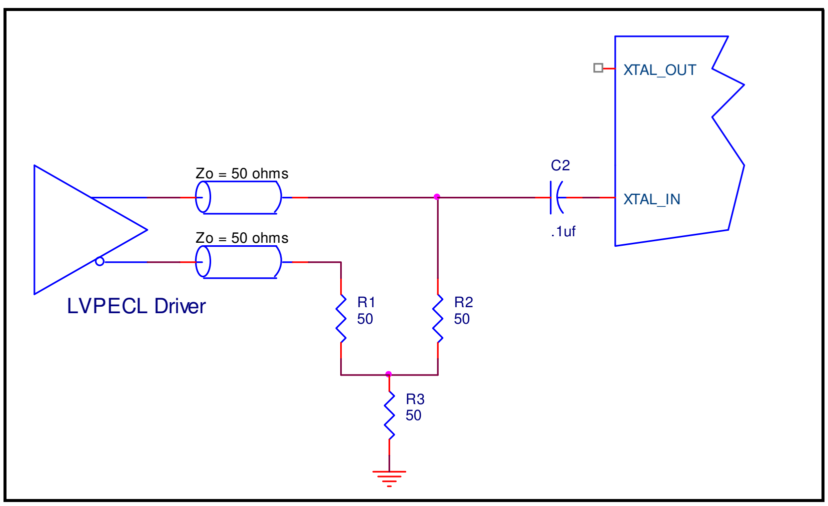


Figure 4B. General Diagram for LVPECL Driver to XTAL Input Interface

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 5A to 5D* show interface examples for the CLK /nCLK input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

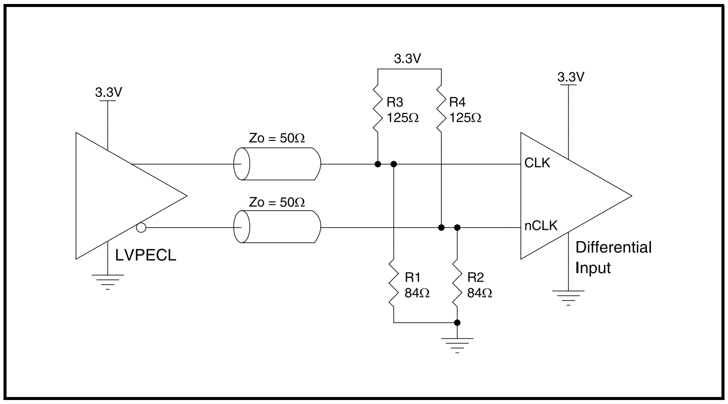


Figure 5A. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

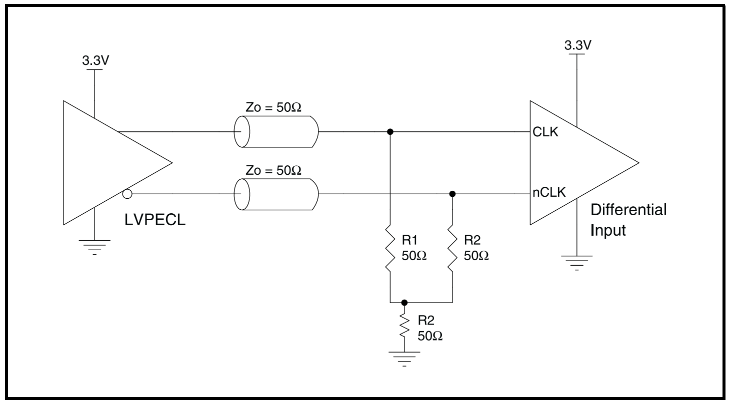


Figure 5B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

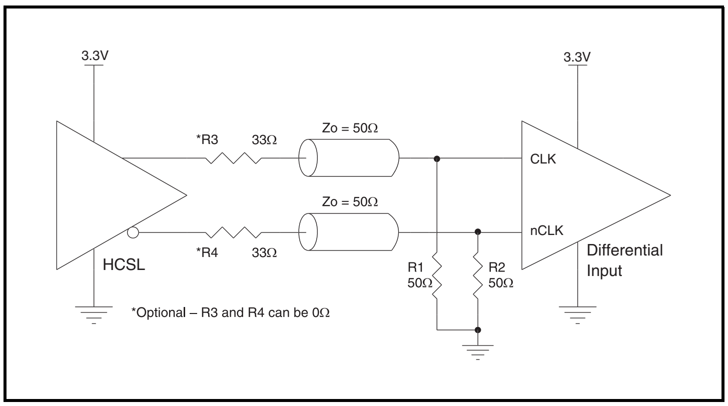


Figure 5C. CLK/nCLK Input Driven by a 3.3V HCSL Driver

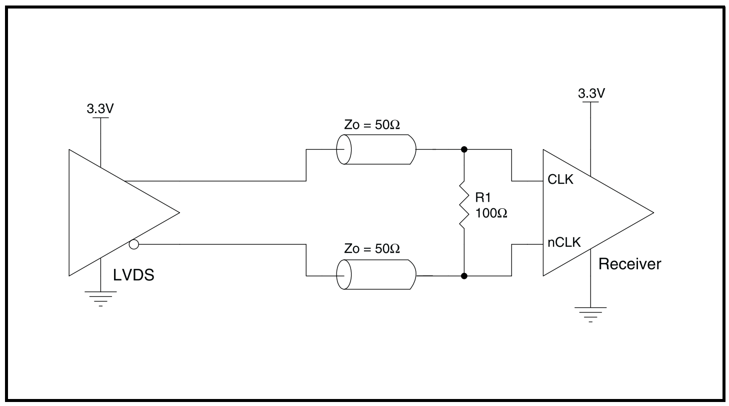


Figure 5D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

2.5V Differential Clock Input Interface

CLKx/nCLKx accepts LVDS, LVPECL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figure to Figure* show interface examples for the CLKx/nCLKx input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure , the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

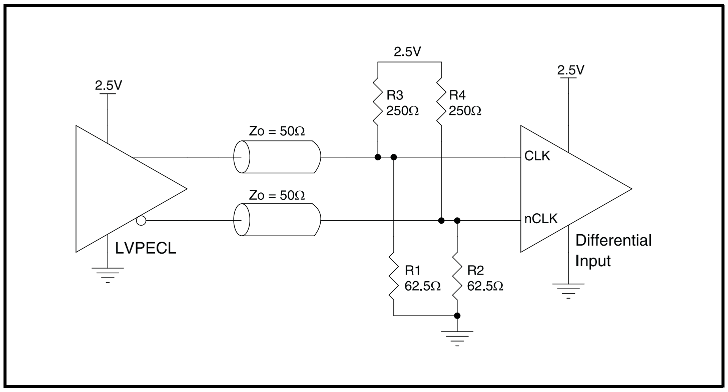


Figure 6A. CLKx/nCLKx Input Driven by a 2.5V LVPECL Driver

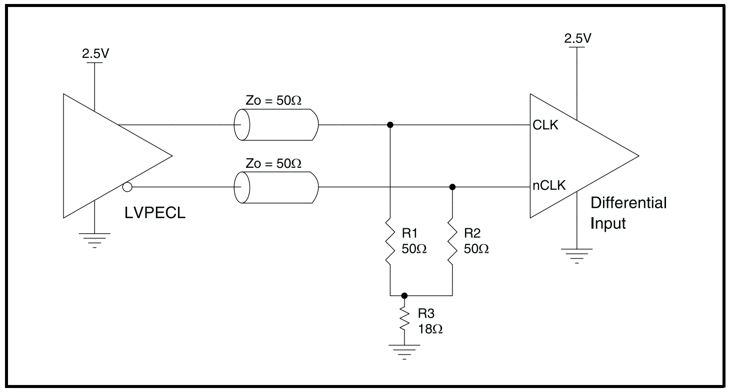


Figure 6B. CLKx/nCLKx Input Driven by a 2.5V LVPECL Driver

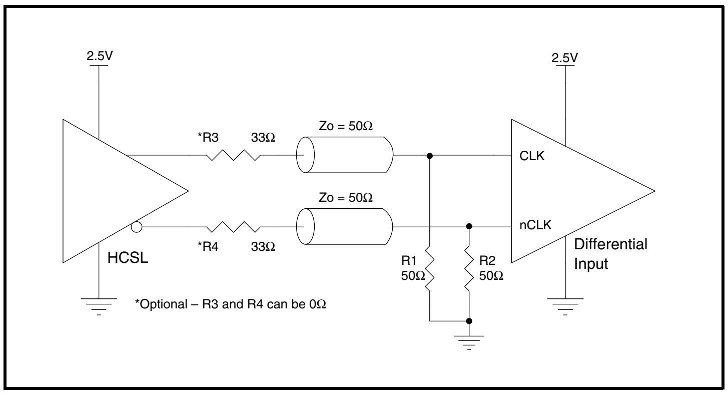


Figure 6C. CLKx/nCLKx Input Driven by a 2.5V HCSL Driver

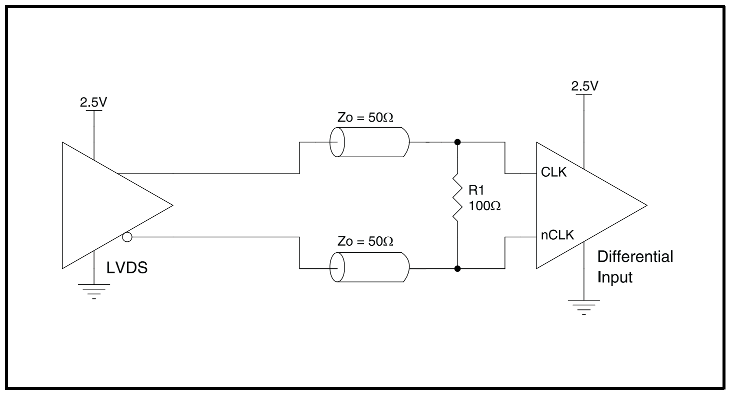


Figure 6D. CLKx/nCLKx Input Driven by a 2.5V LVDS Driver

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

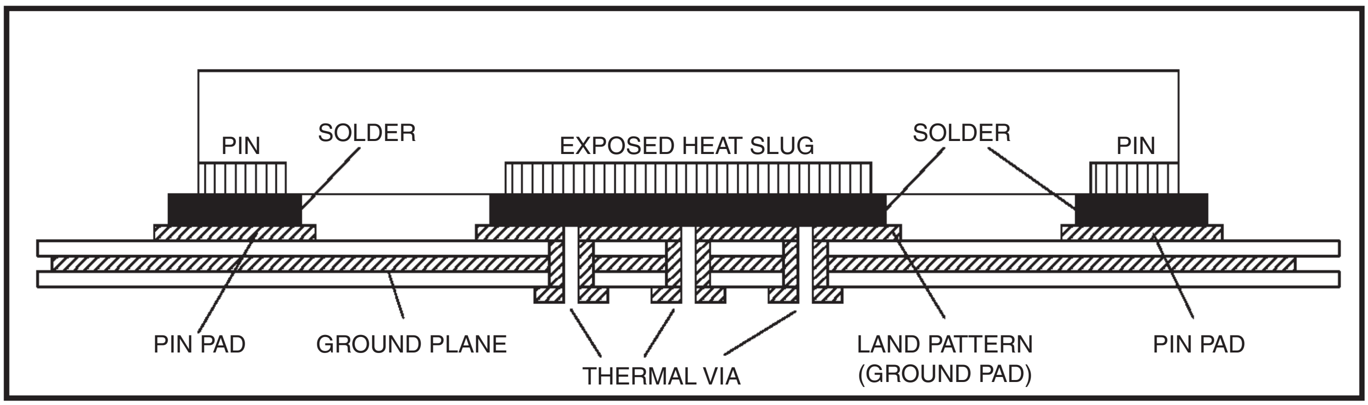


Figure 6. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the 8L30110.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8L30110 is the sum of the core power plus the power dissipation in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

Total Static Power:

Power $(core)_{MAX}$ = V_{DD_MAX} * I_{DD} = 3.465V * 22mA = **76.23mW**

Dynamic Power Dissipation at F_{OUT} (200MHz)

Total Power (F_{OUT_MAX}) = [(C_{PD} * N) * Frequency * $(V_{DDO})^2$**]** = [(9.5pF *10) * 200MHz * $(3.465V)^2$] = **228mW**
N = number of outputs

Total Power
= Static Power + Dynamic Power Dissipation
= 76.23mW + 228mW
= 304.23mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 35.23°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.304 * 35.23°C/W = 95.7°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	35.23°C/W	31.6°C/W	30.0°C/W

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 32-Lead VFQFN

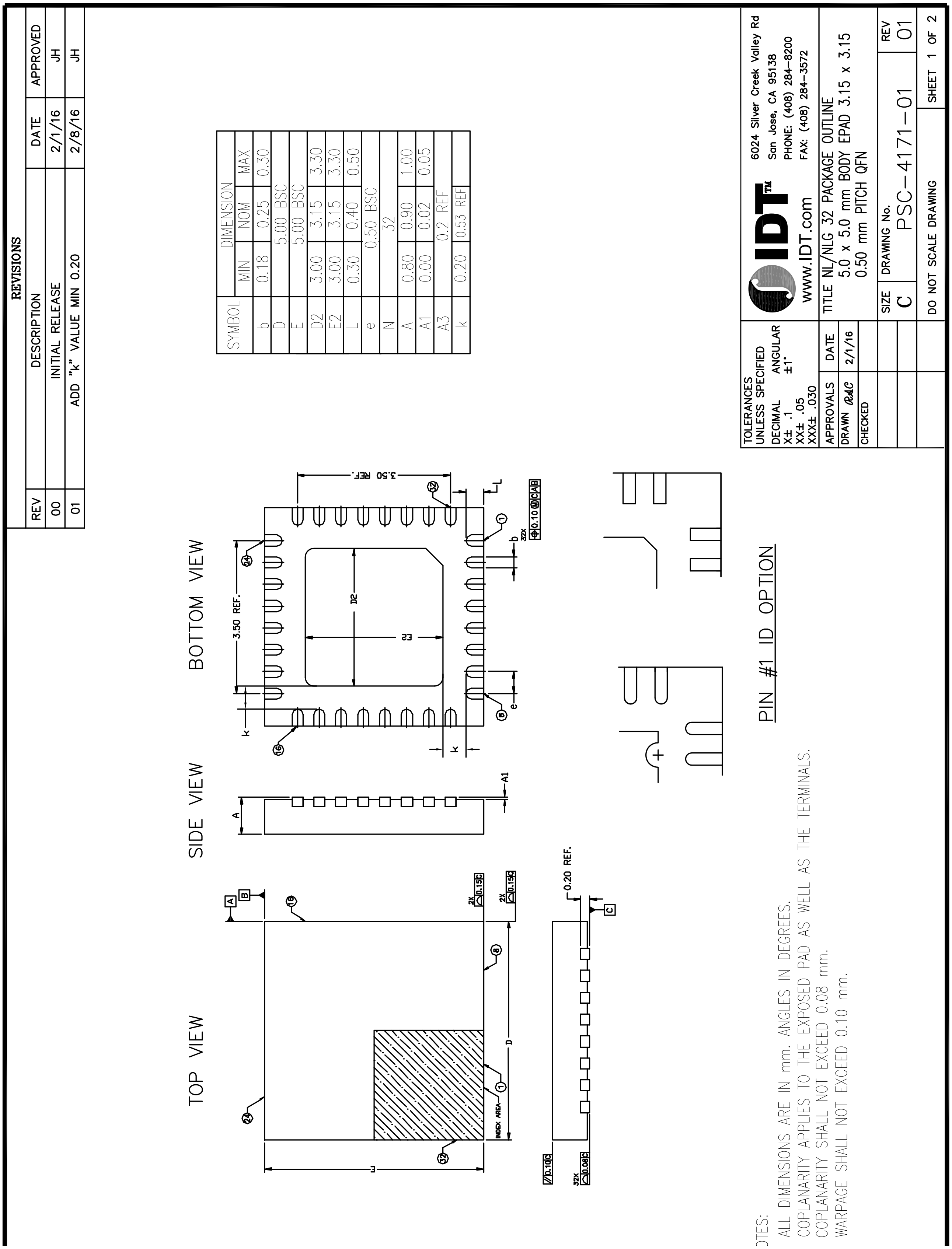
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	35.23°C/W	31.6°C/W	30.0°C/W

Transistor Count

The transistor count for 8L30110 is: 1628

32 Lead VFQFN NL Package Outline and Package Dimensions

Package Outline - NL Suffix for 32 Lead VFQFN

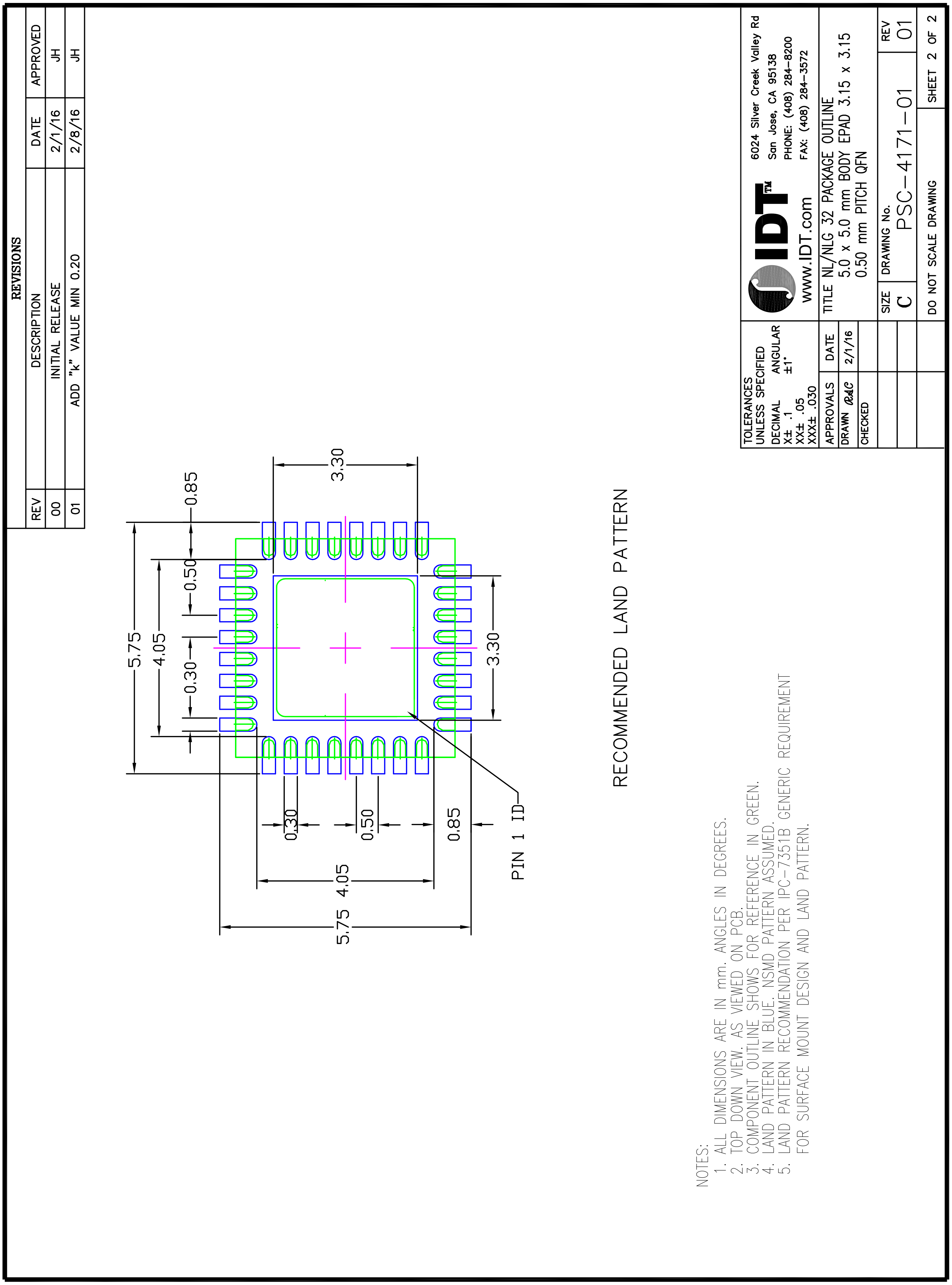


REVISIONS

REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	2/1/16	JH
01	ADD "k" VALUE MIN 0.20	2/8/16	JH

SYMBOL	DIMENSION MIN	NOM	MAX
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
D2	3.00	3.15	3.30
E2	3.00	3.15	3.30
L	0.30	0.40	0.50
e		0.50 BSC	
N		32	
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.2 REF	
k	0.20	0.53 REF	

Package Outline - NL Suffix for 32 Lead VFQFN, continued



Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8L30110NLGI	IDT8L30110NLGI	Lead-Free, 32-Lead VFQFN	Tray	-40°C to 85°C
8L30110NLGI8	IDT8L30110NLGI	Lead-Free, 32-Lead VFQFN	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
2		18-19	Updated Package Outline Updated datasheet header/footer.	2/3/16
3		18-19	Updated Package Outline	2/18/16

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