



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



General Description

8P391208 is intended to take 1 or 2 reference clocks, select between them, using a pin selection and generate up to 8 outputs that are the same as the reference frequency.

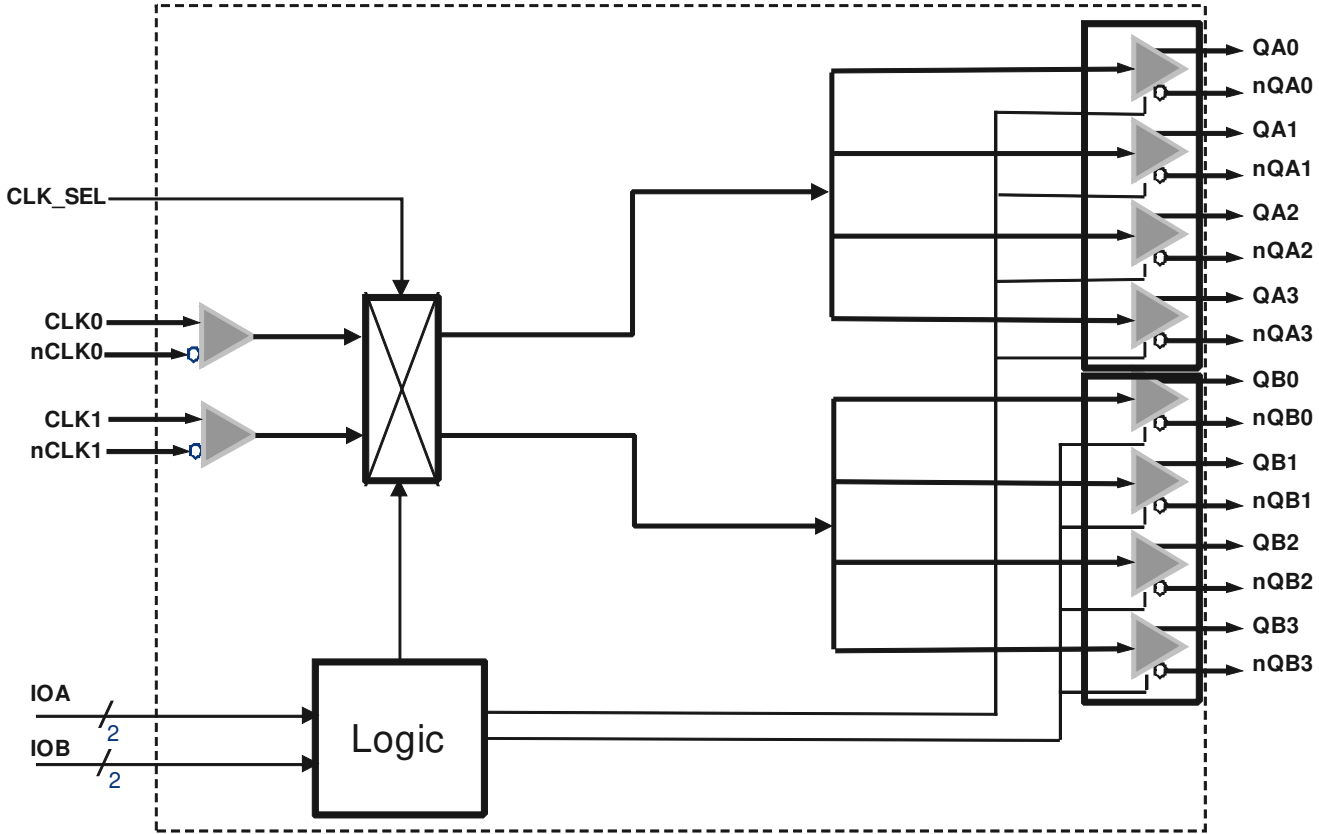
8P391208 supports two output banks, each with its own power supply. All outputs in one bank would generate the same output frequency, and each bank can be individually controlled for output type or output enable.

The device can operate over the -40°C to +85°C temperature range.

Features

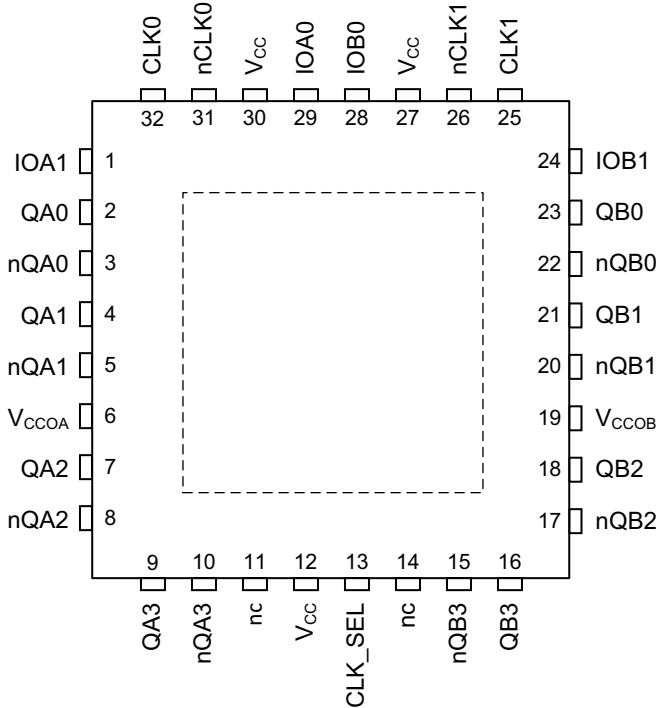
- Two differential inputs support LVPECL, LVDS, HCSL or LVCMOS reference clocks
- Accepts input frequencies ranging from 1PPS (1Hz) to 700MHz (up to 1GHz when configured into HCSL output mode at 3.3V)
- Select which of the two input clocks is to be used as the reference clock for which bank via pin selection
- Generates 8 differential outputs
- Differential outputs selectable as LVPECL, LVDS, CML or HCSL
- CML mode supports two different voltage swings
- Differential outputs support frequencies from 1PPS to 700MHz (up to 1GHz when configured into HCSL output mode at 3.3V)
- Outputs arranged in 2 banks of 4 outputs each
- Each bank supports a separate power supply of 3.3V, 2.5V or 1.8V
- Controlled by 3-level input pins
- Input mux selection control pin
- Control inputs are 3.3V-tolerant for all core voltages
- Output noise floor of -153dBc/Hz @ 156.25MHz
- Core voltage supply of 3.3V, 2.5V or 1.8V
- -40°C to +85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

8P391208 Block Diagram



Pin Assignment

Figure 1: 8P391208 Pin Assignment for 5mm x 5mm 32-pin VFQFN Package



Pin Description and Characteristic Tables

Table 1: Pin Description

Number	Name	Type ^[1]		Description
1	IOA1	Input	Pullup / Pulldown	Controls output functions for Bank A. 3-level input.
2	QA0	Output		Positive differential clock output. Included in Bank A. Refer to Output Drivers section for more details.
3	nQA0	Output		Negative differential clock output. Included in Bank A. Refer to Output Drivers section for more details.
4	QA1	Output		Positive differential clock output. Included in Bank A. Refer to Output Drivers section for more details.
5	nQA1	Output		Negative differential clock output. Included in Bank A. Refer to Output Drivers section for more details.
6	V _{CCOA}	Power		Output voltage supply for Output Bank A.
7	QA2	Output		Positive differential clock output. Included in Bank A. Refer to Output Drivers section for more details.
8	nQA2	Output		Negative differential clock output. Included in Bank A. Refer to Output Drivers section for more details.
9	QA3	Output		Positive differential clock output. Included in Bank A. Refer to Output Drivers section for more details.
10	nQA3	Output		Negative differential clock output. Included in Bank A. Refer to Output Drivers section for more details.
11	nc	Unused		Unused. Do not connect.
12	V _{CC}	Power		Core Logic voltage supply.
13	CLK_SEL	Input	Pullup / Pulldown	Input Clock Selection Control pin. 3-level input. This pin's function is described in the Input Selection section.
14	nc	Unused		Unused. Do not connect.
15	nQB3	Output		Negative differential clock output. Included in Bank B. Refer to Output Drivers section for more details.
16	QB3	Output		Positive differential clock output. Included in Bank B. Refer to Output Drivers section for more details.
17	nQB2	Output		Negative differential clock output. Included in Bank B. Refer to Output Drivers section for more details.
18	QB2	Output		Positive differential clock output. Included in Bank B. Refer to Output Drivers section for more details.
19	V _{CCOB}	Power		Output voltage supply for Output Bank B.
20	nQB1	Output		Negative differential clock output. Included in Bank B. Refer to Output Drivers section for more details.
21	QB1	Output		Positive differential clock output. Included in Bank B. Refer to Output Drivers section for more details.

Table 1: Pin Description (Continued)

22	nQB0	Output		Negative differential clock output. Included in Bank B. Refer to Output Drivers section for more details.
23	QB0	Output		Positive differential clock output. Included in Bank B. Refer to Output Drivers section for more details.
24	IOB1	Input	Pullup / Pulldown	Controls output functions for Bank B. 3-level input.
25	CLK1	Input	Pulldown	Non-inverting differential clock input.
26	nCLK1	Input	Pullup / Pulldown	Inverting differential clock input. $V_{CC}/2$ when left floating (set by the internal pullup and pulldown resistors).
27	V_{CC}	Power		Core Logic voltage supply.
28	IOB0	Input	Pullup / Pulldown	Controls output functions for Bank B. 3-level input.
29	IOA0	Input	Pullup / Pulldown	Controls output functions for Bank A. 3-level input.
30	V_{CC}	Power		Core Logic voltage supply.
31	nCLK0	Input	Pullup / Pulldown	Inverting differential clock input. $V_{CC}/2$ when left floating (set by the internal pullup and pulldown resistors).
32	CLK0	Input	Pulldown	Non-inverting differential clock input.
EP	V_{EE}	Ground		Exposed pad must be connected to GND.

1. *Pullup* and *Pulldown* refer to internal input resistors. See [Table 2, Pin Characteristics](#), for typical values.

Table 2: Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
C_{PD}	Power Dissipation Capacitance (per output pair)	LVPECL	$V_{CCOx}^{[1]} = 3.465V$ or $2.625V$	2.0		pF
		LVDS				pF
		CML, 400mV				pF
		CML, 800mV				pF
	QA[0:3], nQA[0:3]; QB[0:3], nQB[0:3]	LVPECL	$V_{CCOx}^{[1]} = 1.89V$	2.5		pF
		LVDS				pF
		CML, 400mV				pF
		CML, 800mV				pF
R_{PULLUP}	Input Pullup Resistor			51		k Ω
$R_{PULLDOWN}$	Input Pulldown Resistor			51		k Ω

1. V_{CCOx} refers to V_{CCOA} for QA[3:0], nQA[3:0] or V_{CCOB} for QB[3:0], nQB[3:0].

Principles of Operation

Input Selection

The 8P391208 supports two input references: CLK0 and CLK1 that may be driven with differential or single-ended clock signals. Either may be used as the source frequency for either or both output banks under control of the CLK_SEL input pin.

Table 3: Input Selection Control

CLK_SEL	Description
High	Banks A & B Both Driven from CLK1
Middle ^[1]	Bank A Driven from CLK0 & Bank B Driven from CLK1
Low	Banks A & B Both Driven from CLK0

1. A 'middle' voltage level is defined in [Table 10](#). Leaving the input pin open will also generate this level via a weak internal resistor network.

Output Drivers

The QA[0:3] and QB[0:3] clock outputs are provided with pin-controlled output drivers. The following table shows how each bank can be controlled. Each bank is separately controlled and all outputs within a single bank will behave the same way.

Table 4: Output Mode and Enable Control

IOx[1]	IOx[0]	Output Bank Function
High	High	All outputs in the bank are high-impedance
High	Middle	All outputs in the bank are LVPECL
High	Low	All outputs in the bank are LVDS
Middle	High	All outputs in the bank are CML (400mV)
Middle	Middle	All outputs in the bank are high-impedance
Middle	Low	All outputs in the bank are HCSL
Low	High	All outputs in the bank are CML (800mV)
Low	Middle	All outputs in the bank are LVPECL
Low	Low	All outputs in the bank are high-impedance

CML operation supports both a 400mV (pk-pk) swing and an 800mV (pk-pk) swing selection.

The operating voltage ranges of each output is determined by its independent output power pin (V_{CCOA} or V_{CCOB}) and thus each can have different output voltage levels. Output voltage levels of 1.8V, 2.5V or 3.3V are supported for differential operation.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under **Absolute Maximum Ratings** may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the **DC Characteristics or AC Characteristics** is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 5: Absolute Maximum Ratings

Item	Rating
Supply Voltage, $V_{CCX}^{[1]}$ to GND	3.6V
Inputs IOA[1:0], IOB[1:0], CLK_SEL, CLK0, nCLK0, CLK1, nCLK1	-0.5V to 3.6V
Outputs, I _O QA[0:3], nQA[0:3]; QB[0:3], nQB[0:3] Continuous Current Surge Current	40mA 60mA
Outputs, V _O QA[0:3], nQA[0:3]; QB[0:3], nQB[0:3]	-0.5V to 3.6V
Operating Junction Temperature	125°C
Storage Temperature, T _{STG}	-65°C to 150°C
Lead Temperature (Soldering, 10s)	+260°C

1. V_{CCX} denotes V_{CC} , V_{CCOA} , or V_{CCOB} .

Supply Voltage Characteristics

Table 6: Power Supply Characteristics, $V_{CC} = V_{CCOX}^{[1]} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $+85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCOX}	Output Supply Voltage		3.135	3.3	3.465	V
I_{CC}	Core Supply Current	All Outputs Configured for LVDS Logic Levels; Outputs Unloaded		22	25	mA
I_{CCOX}	Output Supply Current ^[2]	All Outputs Configured for LVDS Logic Levels; Outputs Unloaded		139	157	mA

1. NOTE 1. V_{CCOX} denotes V_{CCOA} , V_{CCOB} .

2. Internal dynamic switching current at maximum f_{OUT} is included.

Table 7: Power Supply Characteristics, $V_{CC} = V_{CCOX}^{[1]} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $+85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	2.5	2.625	V
V_{CCOX}	Output Supply Voltage		2.375	2.5	2.625	V
I_{CC}	Core Supply Current	All Outputs Configured for LVDS Logic Levels; Outputs Unloaded		19	22	mA
I_{CCOX}	Output Supply Current ^[2]	All Outputs Configured for LVDS Logic Levels; Outputs Unloaded		137	154	mA

1. NOTE 1. V_{CCOX} denotes V_{CCOA} , V_{CCOB} .

2. Internal dynamic switching current at maximum f_{OUT} is included.

Table 8: Power Supply Characteristics, $V_{CC} = V_{CCOx}^{[1]} = 1.8V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $+85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		1.71	1.8	1.89	V
V_{CCOx}	Output Supply Voltage		1.71	1.8	1.89	V
I_{CC}	Core Supply Current	All Outputs Configured for LVDS Logic Levels; Outputs Unloaded		15	17	mA
I_{CCOx}	Output Supply Current ^[2]	All Outputs Configured for LVDS Logic Levels; Outputs Unloaded		125	141	mA

- NOTE 1. V_{CCOx} denotes V_{CCOA} , V_{CCOB} .
- Internal dynamic switching current at maximum f_{OUT} is included.

Table 9: Typical Output Supply Current, $V_{CC} = 3.3V$, $2.5V$ or $1.8V$, $V_{EE} = 0V$, $T_A = 25^\circ C$

Symbol	Parameter ^[1]	Test Conditions	$V_{CCOx}^{[2]} = 3.3V$					$V_{CCOx}^{[2]} = 2.5V$					$V_{CCOx}^{[2]} = 1.8V$					Units
			LVPECL	LVDS	HCSL	CML (400mV)	CML (800mV)	LVPECL	LVDS	HCSL	CML (400mV)	CML (800mV)	LVPECL	LVDS	HCSL	CML (400mV)	CML (800mV)	
I_{CCOA}	Bank A Output Supply Current	Outputs Unloaded	50	66	41	33	33	49	65	37	31	31	43	28	31	27	27	mA
I_{CCOB}	Bank B Output Supply Current	Outputs Unloaded	50	66	41	33	33	49	65	37	31	31	43	28	31	27	27	mA

- Internal dynamic switching current at maximum f_{OUT} is included.
- V_{CCOx} denotes V_{CCOA} , or V_{CCOB} .

DC Electrical Characteristics

Table 10: LVC MOS/LVTTL Control / Status Signals DC Characteristics for 3-Level Pins, $V_{EE} = 0V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$

	Parameter	Signals	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK_SEL, IOA[1:0], IOB[1:0]	$V_{CC} = 3.3V$	$0.85 \cdot V_{CC}$		3.465	V
			$V_{CC} = 2.5V$	$0.85 \cdot V_{CC}$		2.625	V
			$V_{CC} = 1.8V$	$0.85 \cdot V_{CC}$		1.89	V
V_{IM}	Input Middle Voltage ^[1]	CLK_SEL, IOA[1:0], IOB[1:0]	$V_{CC} = 3.3V$	$0.45 \cdot V_{CC}$		$0.55 \cdot V_{CC}$	V
			$V_{CC} = 2.5V$	$0.45 \cdot V_{CC}$		$0.55 \cdot V_{CC}$	V
			$V_{CC} = 1.8V$	$0.45 \cdot V_{CC}$		$0.55 \cdot V_{CC}$	V
V_{IL}	Input Low Voltage	CLK_SEL, IOA[1:0], IOB[1:0],	$V_{CC} = 3.3V$	-0.3		$0.15 \cdot V_{CC}$	V
			$V_{CC} = 2.5V$	-0.3		$0.15 \cdot V_{CC}$	V
			$V_{CC} = 1.8V$	-0.3		$0.15 \cdot V_{CC}$	V
I_{IH}	Input High Current	CLK_SEL, IOA[1:0], IOB[1:0]	$V_{CC} = V_{IN} = 3.465V$ or $2.625V$ or $1.89V$			150	μA
I_{IM}	Input Middle Current	CLK_SEL, IOA[1:0], IOB[1:0]	$V_{CC} = 3.465V$ or $2.625V$ or $1.89V$, $V_{IN} = V_{CC} / 2$	-10		10	μA
I_{IL}	Input Low Current	CLK_SEL, IOA[1:0], IOB[1:0],	$V_{CC} = 3.465V$ or $2.625V$ or $1.89V$, $V_{IN} = 0V$	-150			μA

1. For 3-level input pins, a mid-level voltage is used to select the 3rd state. This voltage will be maintained by a weak internal pull-up / pull-down network for each pin to select this state if the pin is left open. It is recommended that any external resistor networks used to select a middle-level input voltage be terminated to the device's core V_{CC} voltage level.

Table 11: Differential Input DC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $2.5V \pm 5\%$ or $1.8V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLKx, nCLKx ^[1]	$V_{CC} = V_{IN} = 3.465V$ or $2.625V$		150	μA
I_{IL}	Input Low Current	CLKx ^[1]	$V_{CC} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-5		μA
		nCLKx ^[1]	$V_{CC} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-150		μA
V_{PP}	Peak-to-Peak Voltage ^[2]		0.2		1.3	V
V_{CMR}	Common Mode Input Voltage ^{[2], [3]}		V_{EE}		$V_{CC} - 1.2$	V

1. CLKx denotes CLK0, CLK1. nCLKx denotes nCLK0, nCLK1.
 2. V_{IL} should not be less than -0.3V. V_{IH} should not be higher than V_{CC} .
 3. Common mode voltage is defined as the cross-point.

Table 12: LVPECL DC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $2.5V \pm 5\%$ or $1.8V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $+85^\circ C$

Symbol	Parameter		$V_{CCOx}^{[1]} = 3.3V \pm 5\%$			$V_{CCOx}^{[1]} = 2.5V \pm 5\%$			$V_{CCOx}^{[1]} = 1.8V \pm 5\%$			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage ^[2]	$Qx, nQx^{[3]}$	$V_{CCOx} - 1.3$		$V_{CCOx} - 0.8$	$V_{CCOx} - 1.35$		$V_{CCOx} - 0.9$	$V_{CCOx} - 1.50$		$V_{CCOx} - 0.9$	V
V_{OL}	Output Low Voltage ^[2]	$Qx, nQx^{[2]}$	$V_{CCOx} - 2$		$V_{CCOx} - 1.75$	$V_{CCOx} - 2$		$V_{CCOx} - 1.75$	V_{EE}		0.25	V

- V_{CCOx} denotes V_{CCOA} , V_{CCOB} .
- Outputs terminated with 50Ω to $V_{CCOx} - 2V$ when $V_{CCOx} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$. Outputs terminated with 50Ω to ground when $V_{CCOx} = 1.8V \pm 5\%$.
- Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3. nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

Table 13: LVDS DC Characteristics, $V_{CCOx}^{[1]} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $+85^\circ C^{[1]}$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage	$Qx, nQx^{[2]}$	Terminated 100Ω across Qx and nQx	195		480	mV
ΔV_{OD}	V_{OD} Magnitude Change	$Qx, nQx^{[2]}$				50	mV
V_{OS}	Offset Voltage	$Qx, nQx^{[2]}$		1.1		1.375	V
ΔV_{OS}	V_{OS} Magnitude Change	$Qx, nQx^{[2]}$				50	mV

- V_{CCOx} denotes V_{CCOA} , V_{CCOB} .
- Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3.
 nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

Table 14: LVDS DC Characteristics, $V_{CCOx}^{[1]} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $+85^\circ C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage	$Qx, nQx^{[2]}$	Terminated 100Ω across Qx and nQx	195		470	mV
ΔV_{OD}	V_{OD} Magnitude Change	$Qx, nQx^{[2]}$				50	mV
V_{OS}	Offset Voltage	$Qx, nQx^{[2]}$		1.1		1.375	V
ΔV_{OS}	V_{OS} Magnitude Change	$Qx, nQx^{[2]}$				50	mV

- V_{CCOx} denotes V_{CCOA} , V_{CCOB} .
- Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3.
 nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

Table 15: LVDS DC Characteristics, $V_{CCOx}^{[1]} = 1.8V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $+85^\circ C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage	Qx, nQx ^[2]	Terminated 100Ω across Qx and nQx	195		454	mV
ΔV_{OD}	V_{OD} Magnitude Change	Qx, nQx ^[2]				50	mV
V_{OS}	Offset Voltage	Qx, nQx ^[2]		1.1		1.375	V
ΔV_{OS}	V_{OS} Magnitude Change	Qx, nQx ^[2]				50	mV

- V_{CCOx} denotes V_{CCOA} , V_{CCOB} .
- Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3.
nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

Table 16: CML (400mV Swing) DC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $2.5V \pm 5\%$ or $1.8V \pm 5\%$, $V_{CCOx}^{[1]} = 3.3V \pm 5\%$, $2.5V \pm 5\%$ or $1.8V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $+85^\circ C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage	Qx, nQx ^[2]	Terminated with 50Ω to V_{CCOx}	$V_{CCOx} - 0.1$		V_{CCOx}	V
V_{OL}	Output Low Voltage	Qx, nQx ^[2]		$V_{CCOx} - 0.5$		$V_{CCOx} - 0.3$	V
V_{OUT}	Output Voltage Swing	Qx, nQx ^[2]		300		500	mV

- V_{CCOx} denotes V_{CCOA} , V_{CCOB} .
- Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3.
nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

Table 17: CML (800mV Swing) DC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $2.5V \pm 5\%$ or $1.8V \pm 5\%$, $V_{CCOx}^{[1]} = 3.3V \pm 5\%$, $2.5V \pm 5\%$ or $1.8V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $+85^\circ C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage	Qx, nQx ^[2]	Terminated with 50Ω to V_{CCOx}	$V_{CCOx} - 0.1$		V_{CCOx}	V
V_{OL}	Output Low Voltage	Qx, nQx ^[2]		$V_{CCOx} - 0.95$		$V_{CCOx} - 0.7$	V
V_{OUT}	Output Voltage Swing	Qx, nQx ^[2]		575		1000	mV

- V_{CCOx} denotes V_{CCOA} , V_{CCOB} .
- Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3.
nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

Table 18: HCSL DC Characteristics, $V_{CC} = V_{CCOA} = V_{CCOB} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 25^\circ C^{[1], [2]}$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage	Qx, nQx		475		900	mV
V_{OL}	Output Low Voltage	Qx, nQx		-100			mV
V_{OUT}	Output Voltage Swing	Qx, nQx		475		900	mV

- Guaranteed by design and Characterization, not 100% tested in production.
- $C_L = 2\text{pf}$, $R_S = 33.2\Omega$, $R_P = 49.9\Omega$

Table 19: Input Frequency Characteristics, $V_{CC} = 3.3V \pm 5\%$, $2.5V \pm 5\%$ or $1.8V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $+85^\circ C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	CLKx, nCLKx ^{[1], [2]}		1Hz		700MHz	
idc	Input Duty Cycle ^[3]				50		%

1. CLKx denotes CLK0, CLK1. nCLKx denotes nCLK0, nCLK1.
2. Input frequency is up to 1GHz when $V_{CC}/V_{CCOx} = 3.3V \pm 5\%$ for HCSL output mode.
3. Any deviation from a 50% duty cycle on the input may be reflected in the output duty cycle.

AC Electrical Characteristics

Table 20: LVDS, LVPECL, CML AC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $2.5V \pm 5\%$ or $1.8V \pm 5\%$, $V_{CCOx}^{[1]} = 3.3V \pm 5\%$, $2.5V \pm 5\%$ or $1.8V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $+85^\circ C$

Symbol	Parameter ^[2]		Test Conditions ^[3]	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	LVDS, LVPECL, CML		1PPS		700	MHz
t_R / t_F	Output Rise and Fall Times	LVPECL	20% to 80%	100		705	ps
		LVDS	20% to 80%, $V_{CCOx} = 3.3V$	150		530	ps
			20% to 80%, $V_{CCOx} = 2.5V$	165		530	ps
			20% to 80%, $V_{CCOx} = 1.8V$	200		565	ps
		CML 400mV	20% to 80%	100		625	ps
CML 800mV	20% to 80%	150		580	ps		
$t_{sk(b)}$	Bank Skew ^{[4], [5], [6]}	LVPECL ^[7]				55	ps
		LVDS ^[7]				55	ps
		CML 400mV ^[7]				55	ps
		CML 800mV ^[7]				55	ps
odc	Output Duty Cycle ^[8]			45	50	55	%
MUX_{ISOL}	Mux Isolation				70		dB
$t_{startup}$	Startup Time				25		ms

- V_{CCOx} denotes V_{CCOA} , V_{CCOB} .
- Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
- Tested for the following out frequencies: 100MHz, 156.25MHz, 312.5MHz, 700MHz.
- This parameter is guaranteed by characterization. Not tested in production.
- This parameter is defined in accordance with JEDEC Standard 65.
- Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.
- Measured at the output differential crosspoint.
- Measured using 50% duty cycle on input reference.

Table 21: HCSL AC Characteristics, $f_{OUT} = 100\text{MHz}$, $V_{CC} = 3.3\text{V} \pm 5\%$, $2.5\text{V} \pm 5\%$ or $1.8\text{V} \pm 5\%$, $V_{CCOX}^{[1]} = 3.3\text{V} \pm 5\%$, $2.5\text{V} \pm 5\%$ or $1.8\text{V} \pm 5\%$, $V_{EE} = 0\text{V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

Symbol	Parameter ^[2]	Test Conditions	Minimum	Typical	Maximum	Units
V_{RB}	Ring-back Voltage Margin ^{[3], [4]}		-100		100	mV
t_{STABLE}	Time before V_{RB} is allowed ^{[3], [4]}		500			ps
V_{MAX}	Absolute Max. Output Voltage ^{[5], [6]}				1150	mV
V_{MIN}	Absolute Min. Output Voltage ^{[5], [7]}		-300			mV
V_{CROSS}	Absolute Crossing Voltage ^{[8], [9], [5]}		200		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edge ^{[8], [10], [5]}				140	mV

1. V_{CCOX} denotes V_{CCOA} , V_{CCOB} .
2. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
3. Measurement taken from differential waveform.
4. t_{STABLE} is the time the differential clock must maintain a minimum $\pm 150\text{mV}$ differential voltage after rising/falling edges before it is allowed to drop back into the $V_{RB} \pm 100\text{mV}$ differential range.
5. Measurement taken from single ended waveform.
6. Defined as the maximum instantaneous voltage including overshoot.
7. Defined as the minimum instantaneous voltage including undershoot.
8. Measured at crossing point where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx.
9. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
10. Defined as the total variation of all crossing voltages of rising Qx and falling nQx, This is the maximum allowed variance in V_{CROSS} for any particular system.

Table 22: HCSL Electrical Characteristics, Current Mode Differential Pair, $V_{CC} = V_{CCOA} = V_{CCOB} = 3.3V \pm 5\%$, $2.5V \pm 5\%$ or $1.8V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $+85^\circ C$ ^{[1], [2]}

Symbol	Parameter	Test Conditions ^{[3], [4]}	Minimum	Typical	Maximum	Units
V_{OH}	Output Voltage High	Statistical Measurement on Single-ended Signal using Oscilloscope Math Function	300		950	mV
V_{OL}	Output Voltage Low		-100			mV
V_{MAX}	Absolute Max. Output Voltage ^{[5], [6]}				1150	mV
V_{MIN}	Absolute Min. Output Voltage ^{[5], [7]}		-300			mV
V_{CROSS}	Absolute Crossing Voltage ^{[5], [8], [9]}		150		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all Edges ^{[5], [8], [10]}				140	mV
Edge Rate Rise	Rising Edge Rate ^{[11], [12]}		0.3		4.5	V/ns
Edge Rate Fall	Falling Edge Rate ^{[11], [12]}		0.3		4.5	V/ns

- Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
- Guaranteed by design and Characterization, not 100% tested in production.
- Test configuration: $C_L = 2pF$, $R_S = 33.2\Omega$, $R_P = 49.9\Omega$.
- Tested for the following out frequencies: 156.25MHz, 245.76MHz, 312.5MHz, and 625MHz. For other frequencies, contact IDT Marketing.
- Measurement taken from a single-ended waveform.
- Defined as the maximum instantaneous voltage including overshoot.
- Defined as the minimum instantaneous voltage including undershoot.
- Measured at crossing point where the instantaneous voltage value of the rising edge of CLK+ equals the falling edge of CLK-.
- Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
- Defined as the total variation of all crossing voltages of rising CLK+ and falling CLK-. this is the maximum allowed variance in VCROSS for any particular system.
- Measurement taken from a differential waveform.
- Measured from -150mV on the differential waveform (derived from Q minus nQ). the signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

Table 23: Typical Additive Jitter, $V_{CC} = 3.3V \pm 5\%$, $2.5V \pm 5\%$ or $1.8V \pm 5\%$, $V_{CCOx}^{[1]} = 3.3V \pm 5\%$, $2.5V \pm 5\%$, $1.8V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $+85^\circ C$

Symbol	Parameter	Test Conditions ^[2]	Minimum	Typical	Maximum	Units	
$t_{jit}(f)$	RMS Additive Jitter (Random)	LVPECL	$f_{OUT} = 156.25MHz$, Integration Range: 12kHz - 20MHz		62		fs
		LVDS			82		fs
		HCSL			74		fs
		CML, 400mV			68		fs
		CML, 400mV			65		fs

- V_{CCOx} denotes V_{CCOA} , V_{CCOB} .
- All outputs configured for the specific output type, as shown in the table.

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from CLK to ground.

LVC MOS LV TTL Level Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1k Ω resistor can be used.

LVC MOS 3-Level I/O Control Pins

These pins are 3-level pins and if left unconnected this is interpreted as a valid input selection option (Middle).

Outputs:

Differential Outputs

All unused Differential outputs can be left floating. It is recommended that there is no trace attached.

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

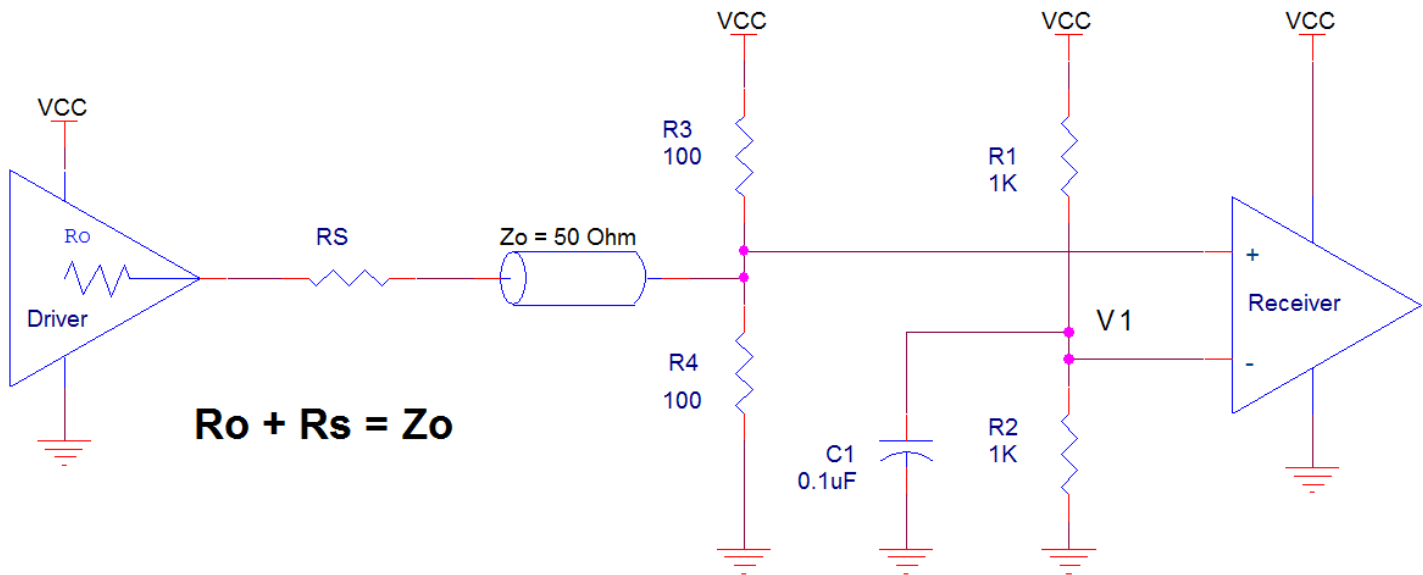
LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100 Ω across. If they are left floating, there should be no trace attached.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and $V_{CC} = 3.3V$, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (R_o) and the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced while maintaining an edge rate faster than 1V/ns. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than $V_{CC} + 0.3V$. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

Figure 2: Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels



3.3V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figure 3 to Figure 7* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in *Figure 3*, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

Figure 3: CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

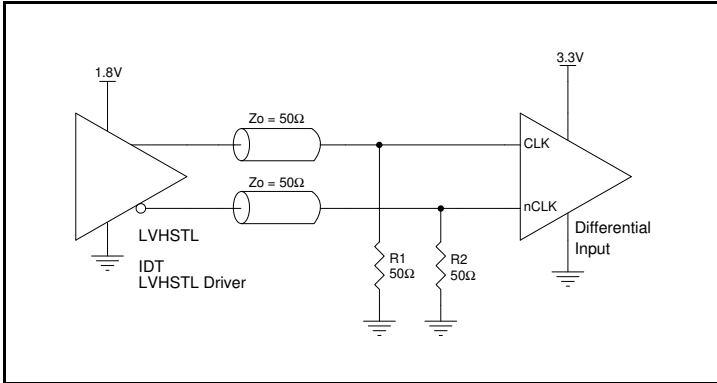


Figure 6: CLK/nCLK Input Driven by a 3.3V LVPECL Driver

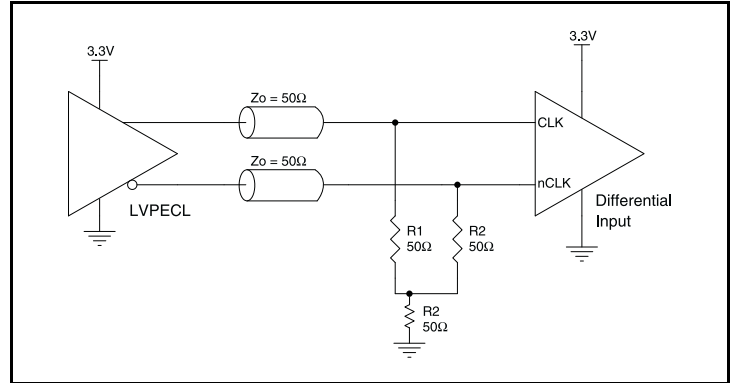


Figure 4: CLK/nCLK Input Driven by a 3.3V LVPECL Driver

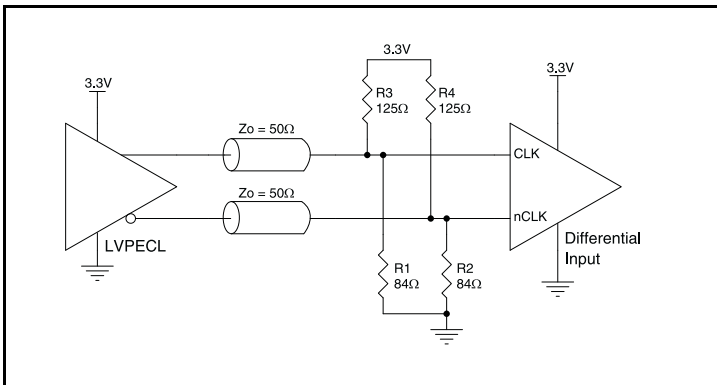


Figure 7: CLK/nCLK Input Driven by a 3.3V HCSL Driver

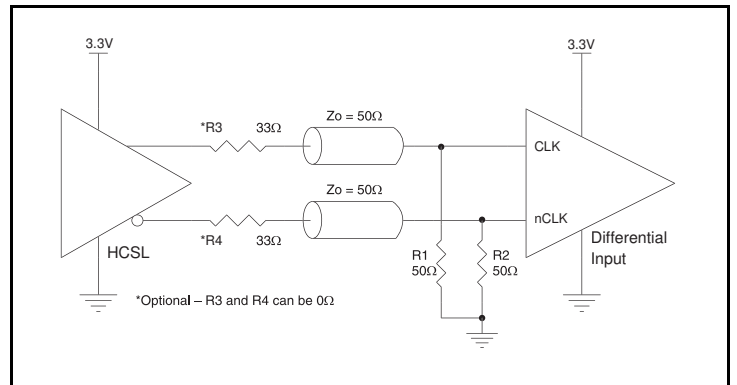
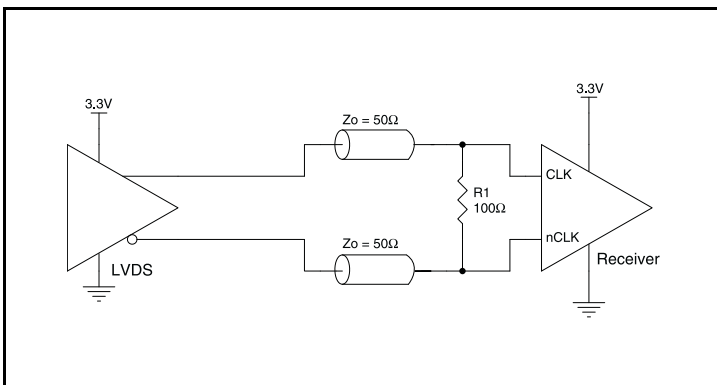


Figure 5: CLK/nCLK Input Driven by a 3.3V LVDS Driver



2.5V Differential Clock Input Interface

CLKx/nCLKx accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figure 8 to Figure 12* show interface examples for the CLKx/nCLKx input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in *Figure 8*, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

Figure 8: CLKx/nCLKx Input Driven by an IDT Open Emitter LVHSTL Driver

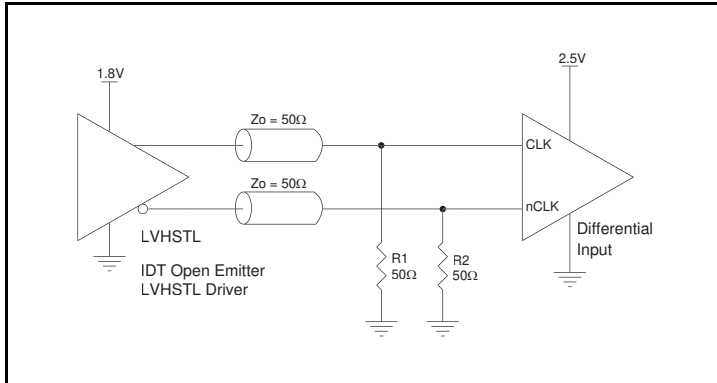


Figure 11: CLKx/nCLKx Input Driven by a 2.5V LVPECL Driver

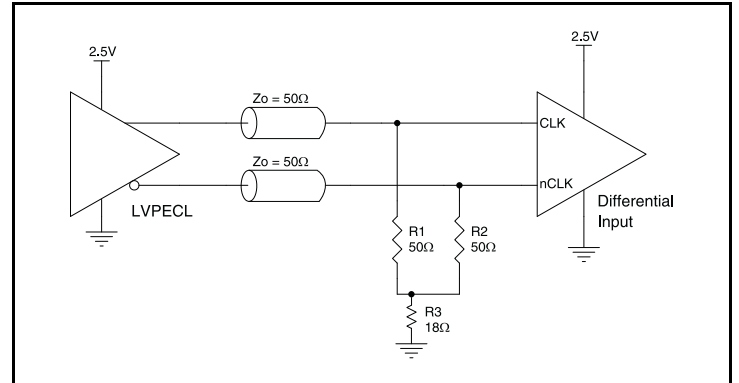


Figure 9: CLKx/nCLKx Input Driven by a 2.5V LVPECL Driver

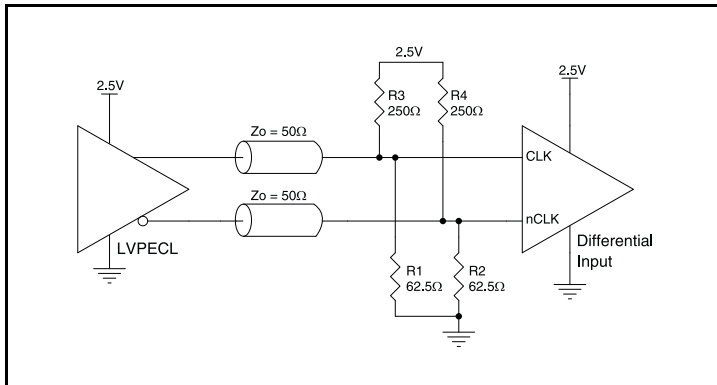


Figure 12: CLKx/nCLKx Input Driven by a 2.5V LVDS Driver

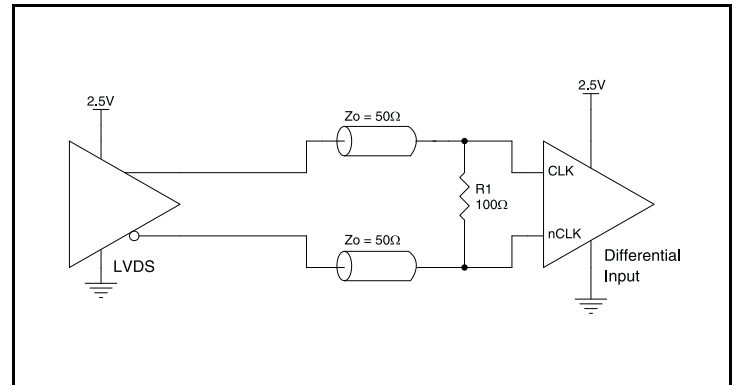
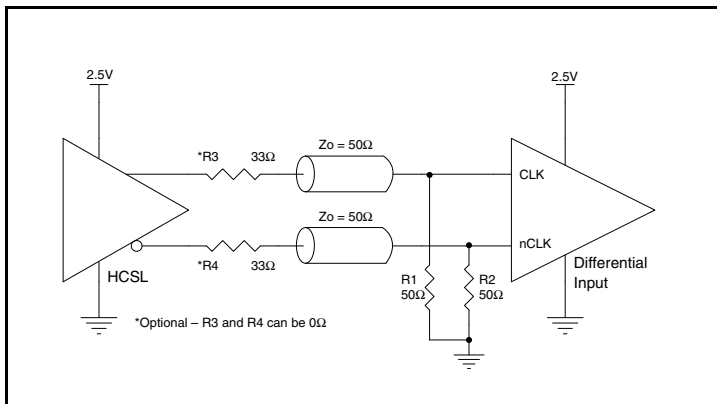


Figure 10: CLKx/nCLKx Input Driven by a 2.5V HCSL Driver



LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω . The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in [Figure 13](#) can be used with either type of output structure. [Figure 14](#), which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF . If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

Figure 13: Standard LVDS Termination

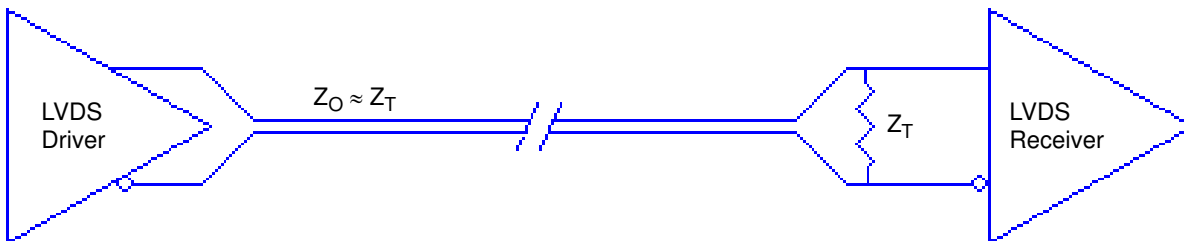
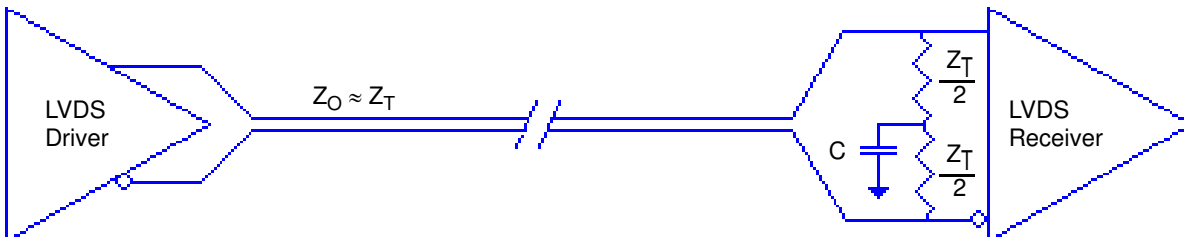


Figure 14: Optional LVDS Termination



Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential output is a low impedance follower output that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. [Figure 15](#) and [Figure 16](#) show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

Figure 15: 3.3V LVPECL Output Termination

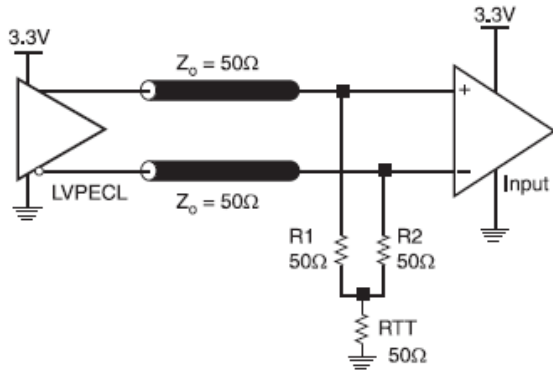
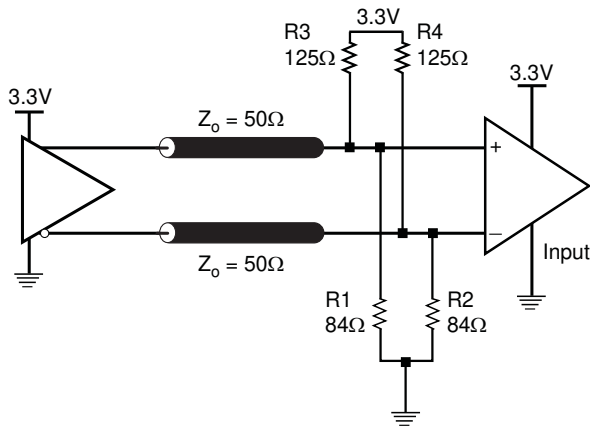


Figure 16: 3.3V LVPECL Output Termination



Termination for 2.5V LVPECL Outputs

Figure 17 and Figure 18 show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{CC0} - 2V$. For $V_{CC0} = 2.5V$, the $V_{CC0} - 2V$ is very close to ground level. The R3 in Figure 18 can be eliminated and the termination is shown in Figure 19.

Figure 17: 2.5V LVPECL Driver Termination Example

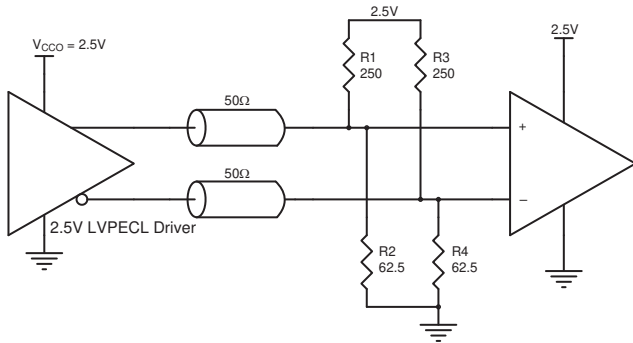


Figure 18: 2.5V LVPECL Driver Termination Example

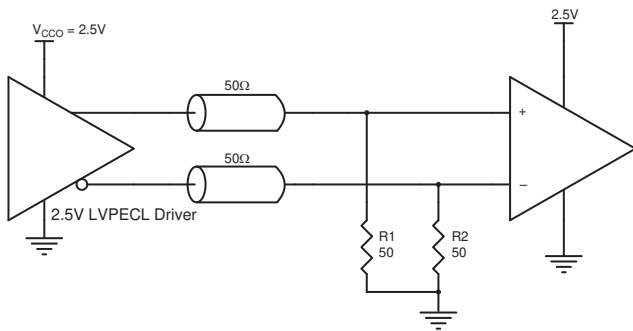
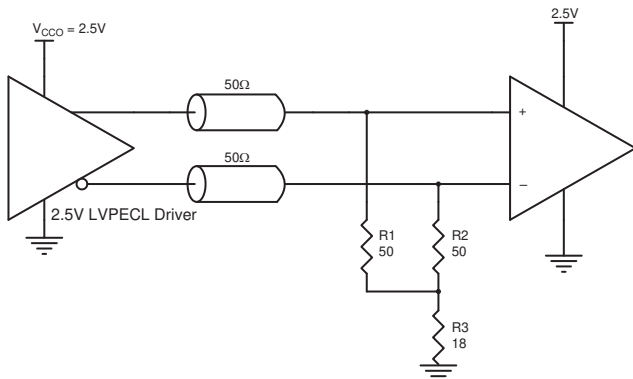


Figure 19: 2.5V LVPECL Driver Termination Example



Recommended Termination for HCSL Outputs

Figure 20 is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output types. All traces should be 50Ω impedance single-ended or 100Ω differential.

Figure 21 is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor (R_s) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

Figure 20: Recommended Source Termination (where the driver and receiver will be on separate PCBs)

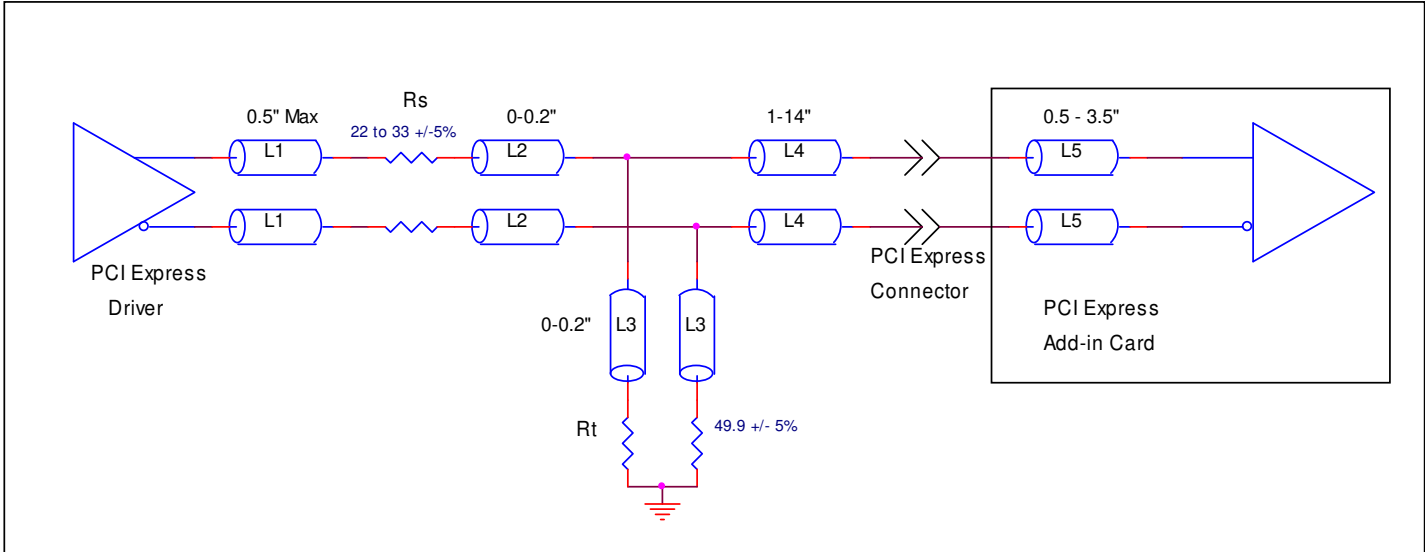
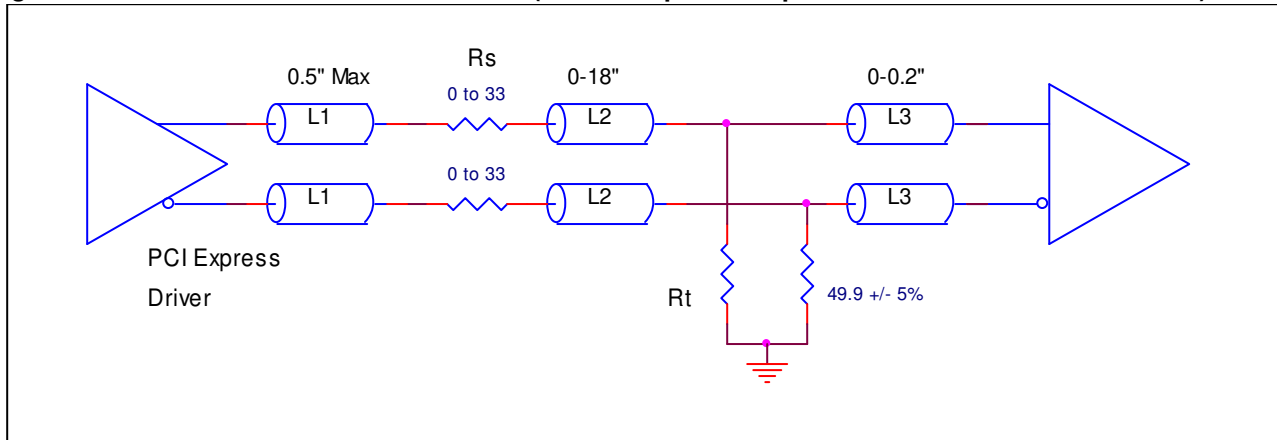


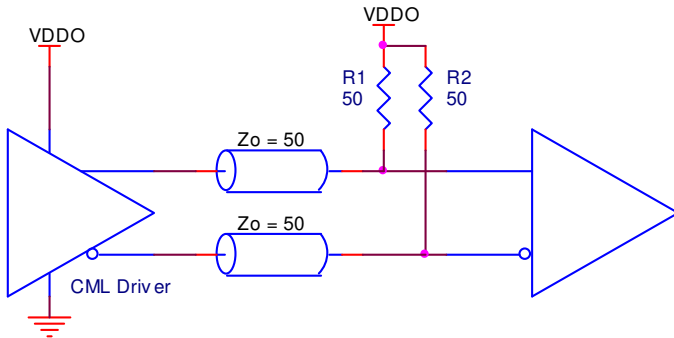
Figure 21: Recommended Termination (where a point-to-point connection can be used)



CML Termination

Figure 22 shows an example of the termination for a CML driver. In this example, the transmission line characteristic impedance is 50Ω . The R1 and R2 50Ω matched load terminations are pulled up to V_{DDO} . The matched loads are located close to the receiver.

Figure 22: CML Termination Example



Power Dissipation and Thermal Considerations

The 8P391208 is a multi-functional, high speed device that targets a wide variety of clock frequencies and applications. Since this device is highly programmable with a broad range of features and functionality, the power consumption will vary as each of these features and functions is enabled.

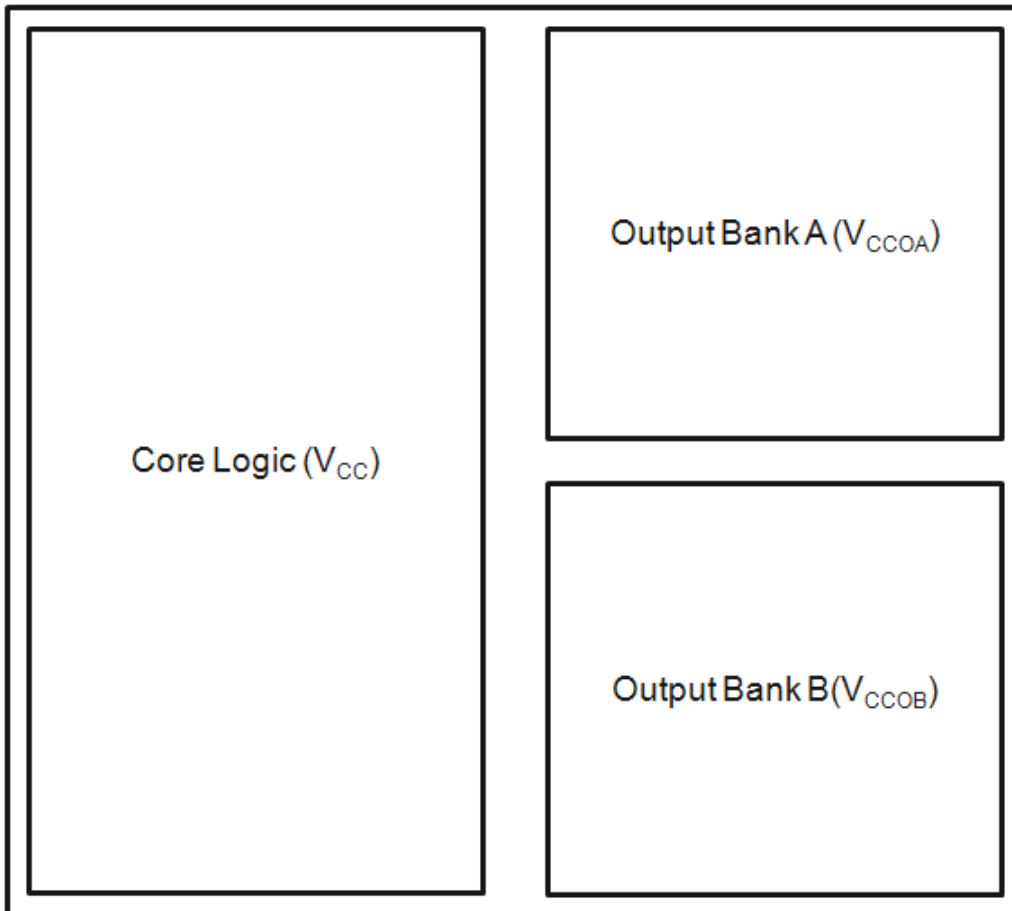
The 8P391208 device was designed and characterized to operate within the ambient industrial temperature range of $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$. The ambient temperature represents the temperature around the device, not the junction temperature. When using the device in extreme cases, such as maximum operating frequency and high ambient temperature, external air flow may be required in order to ensure a safe and reliable junction temperature. Extreme care must be taken to avoid exceeding 125°C junction temperature.

The power calculation examples below were generated using a maximum ambient temperature and supply voltage. For many applications, the power consumption will be much lower. Please contact IDT technical support for any concerns on calculating the power dissipation for your own specific configuration.

Power Domains

The 8P391208 device has a number of separate power domains that can be independently enabled and disabled via register accesses (all power supply pins must still be connected to a valid supply voltage). [Figure 23](#) below indicates the individual domains and the associated power pins.

Figure 23: 8P391208 Power Domains



Power Consumption Calculation

Determining total power consumption involves several steps:

1. Determine the power consumption using maximum current values for core voltage from [Table 6](#), [Table 7](#), [Table 8](#) and [Table 9, Page 7](#) for the appropriate case of how many banks or outputs are enabled.
2. Determine the nominal power consumption of each enabled output path.
 - a. This consists of a base amount of power that is independent of operating frequency, as shown in [Table 25](#) through [Table 36](#) (depending on the chosen output protocol).
 - b. Then there is a variable amount of power that is related to the output frequency. This can be determined by multiplying the output frequency by the FQ_Factor shown in [Table 25](#) through [Table 36](#).
3. All of the above totals are then summed.

Thermal Considerations

Once the total power consumption has been determined, it is necessary to calculate the maximum operating junction temperature for the device under the environmental conditions it will operate in. Thermal conduction paths, air flow rate and ambient air temperature are factors that can affect this. The thermal conduction path refers to whether heat is to be conducted away via a heat-sink, via airflow or via conduction into the PCB through the device pads (including the ePAD). Thermal conduction data is provided for typical scenarios in [Table 42, Page 36](#). Please contact IDT for assistance in calculating results under other scenarios.

Table 24: θ_{JA} vs. Air Flow Table for a 32-lead 5mm x 5mm VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	35.23°C/W	31.6°C/W	30.0°C/W